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Research Article

A Floating CCCII and DDCC Based Memcapacitor Circuit With Electronically Controllable Behavior

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Abstract
In this paper, a simple floating memcapacitor emulator circuit is developed using two active circuit elements. The proposed circuit is having not only a simple structure but also electronically controllable property. The operating frequency of the proposed circuit can be tuned by changing only one voltage source. Some analyses such as different frequencies, voltages, and temperatures are presented to show the proposed circuit performance. Also, to demonstrate the floating feature, the electrical responses of the serial and parallel-connected memcapacitors are given. All simulation results show good agreement with theoretical analyses.

Keywords: memcapacitor, active circuit elements, DDCC, CCCII, electronically controllable.

Elektronik Olarak Kontrol Edilebilir Özelliğe Sahip CCCII ve DDCC Tabanlı Yüzen Memkapasitör Devresi

Öz

Bu çalışmada, iki aktif devre elemanı kullanılarak basit bir yüzen memkapasitör devresi tasarlanmıştır. Hazırlanan devre hem elektronik olarak kontrol edilebilirlik özelliğine hem de basit bir yapıya sahiptir. Hazırlanan devrenin çalışma frekansı, kutuplama gerilim değeri yardımıyla değiştirilebilir. Önerilen devrenin performansını göstermek için farklı frekanslar, gerilimler ve sıcaklıklar gibi bazı analizler sunulmuştur. Ayrıca devrenin yüzen özelliğini göstermek için seri ve paralel bağlı memkapasitör devrelerinin sonuçları verilmiştir. Tüm benzetim sonuçları teorik analizlerle iyi bir uyum göstermektedir.

Anahtar Kelimeler: memkapasitör, aktif devre elemanları, DDCC, CCCII, elektronik olarak kontrol edilebilirlik

1. Introduction

Chua introduced a new fundamental passive circuit element, called a memristor, in his seminal paper “Memristor-The missing circuit element” (L. Chua, 1971; L. O. Chua & Sung Mo Kang, 1976). There are four fundamental parameters: Voltage, current, charge, and flux. Passive elements connect these four parameters. For example, resistor connects voltage and current, capacitor connects voltage and charge, inductor connects current and flux. But before

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the seminal paper of Chua(L. Chua, 1971), the relationship between charge and flux was missing. The element which is introduced by Chua(L. Chua, 1971), provides the missing connection between charge and flux. After Chua's definition, this new element is fabricated by the HP research team in 2008 (Strukov, Snider, Stewart, & Williams, 2008). There are different application areas such as neuromorphic circuits (Madsar, Babacan, & Çiçek, 2020; Orman, 2020), chaotic circuits(M. Chen, Sun, Bao, Hu, & Bao, 2020), and logic (Babacan & Kacar, 2021; Q. Chen, Wang, Wan, & Yang, 2017). These three papers (Babacan & Kacar, 2021; M. Chen et al., 2020; Q. Chen et al., 2017) were a milestone for memristors and after these papers, researchers introduced other memristive elements: memcapacitor and meminductor (Di Ventra, Pershin, & Chua, 2009). Memcapacitor and meminductor provide the relationship between integral of charge and flux, integral of flux and charge, respectively. Common properties of memelements are nonvolatility, nonlinearity, low energy consumption, and frequency dependency. For these reasons, memelements are a popular research field among researchers.

Memcapacitors cannot found easily in literature as a discrete circuit element. So, researchers presented various models and circuits(Babacan, 2018; D. Biolek, Biolek, & Biolkova, 2010; D. Biolek & Biolkova, 2010; Dalibor Biolek, Biolek, & Biolková, 2011; Demir, Yesil, Babacan, & Karacali, 2021; Fouda & Radwan, 2012; Madsar et al., 2020; Radwan & Fouda, 2015; Sah, Budhathoki, Yang, & Kim, 2013; Wang, Fitch, Iu, & Qi, 2012; Yesil & Babacan, 2020b; Yu, Liang, Chen, & Iu, 2013) which behave as memcapacitor to overcome this problem. While some researchers presented memcapacitor mathematical and SPICE models (D. Biolek et al., 2010; Dalibor Biolek et al., 2011; Radwan & Fouda, 2015), other parts of researchers designed emulator circuits using active circuit elements (Babacan, 2018; D. Biolek & Biolkova, 2010; Demir et al., 2021; Fouda & Radwan, 2012; Madsar et al., 2020; Sah et al., 2013; Wang et al., 2012; Yesil & Babacan, 2020b; Yu et al., 2013). Also, designed memcapacitor emulators can be found as grounded (D. Biolek & Biolkova, 2010; Demir et al., 2021; Fouda & Radwan, 2012; Madsar et al., 2020; Wang et al., 2012; Yesil & Babacan, 2020b) and floating in terms of structure in literature (Babacan, 2018; Sah et al., 2013; Yu et al., 2013).

Biolek and coworkers purposed a memcapacitor SPICE model which has floating behavior (D. Biolek et al., 2010). Fouda and Radwan presented a charge-controlled memcapacitor emulator (Fouda & Radwan, 2012). This emulator consists of a multiplier to provide nonlinear behavior of memcapacitor and composed of many types of circuit elements. Wang et. al, proposed a memcapacitor mutator circuit based on an LDR-based memristor (Wang et al., 2012). The circuit is also implemented using discrete circuit elements. Madsar and co-workers purposed FCS based memcapacitor emulator circuit(Madsar et al., 2020). This memcapacitor has a grounded structure. Biolek and Biolkova presented a memcapacitor emulator by converting memristor which is based on a second-generation current conveyor (CCII). The proposed memcapacitor circuit has two CCII, a capacitor, a floating resistor, and a memristor (D. Biolek & Biolkova, 2010). Babacan suggested Operational Transconductance Amplifier (OTA)-based floating memcapacitor and meminductor emulator circuits. The simulation results for these circuits are given in 100-300Hz and 100-500Hz ranges for memcapacitor and meminductor circuits, respectively (Babacan, 2018). A grounded memcapacitor circuit with electronically controllable was presented by Konal M. and Kacar

F. This memcapacitor circuit has a multi output OTA (MO-OTA), an OTA circuit element and a voltage multiplier as active circuit element. As passive elements in this memcapacitor circuit, two grounded capacitors, a floating resistor, and one grounded resistor are employed. The presented memcapacitor has an electrically controllable and it works between 1 and 10Hz frequency range(Konal & Kacar, 2021). Yesil A. & Babacan Y. (Yesil & Babacan, 2020b) proposed grounded memcapacitor circuits. The first circuit consists of two CCIIs, three capacitors, one voltage multiplier and one resistor. The resistor provides electronically controllable behavior. Experimental and simulation results of the presented memcapacitor are given. Second circuit has one CCII, one OTA, three capacitors and one voltage multiplier. The memcapacitor has electronically controllable feature thanks to the transconductance of OTA. Different types of memcapacitor emulator circuits can be found in the literature. Each of these emulator circuits has advantages and disadvantages in term of operating frequency, grounded or floating structure, electronically controllable property etc. Researchers prefer to the most suitable circuit according to features of the application area.

In this study, we proposed an electronically controllable floating memcapacitor emulator circuit. The proposed circuit has one differential difference current conveyor (DDCC), one second-generation current controlled conveyor (CCCII), one multiplier, one resistor, and three capacitors. Besides the simple structure, both electronically controllable property and floating structure are important properties of the circuit. All simulations are implemented using the LTSPICE simulation program with TSMC 0.18 µm parameters. Furthermore, so as to demonstrate floating feature and the performances of the proposed memcapacitor, a MC-R circuit is given and compared with C-R circuit simulation results.

2. Material and Methods

The Proposed Memcapacitor Emulator Circuit

As an active circuit element, only one DDCC and one CCCII are used to implement our memcapacitor emulator circuit. The used DDCC active element has Y_1, Y_2, Y_3, X, Z_P, Z_N terminals. The X, Y, and Z terminals represent voltage and current, respectively. The relationships for all CCCII terminals are given with details in Eq. (2) The circuit symbols of the DDCC and CCCII are shown in Fig. 1a and Fig. 1b, which show the two types of output terminals. Here, the positive and negative outputs are represented by terminal Z_P and Z_N, respectively.

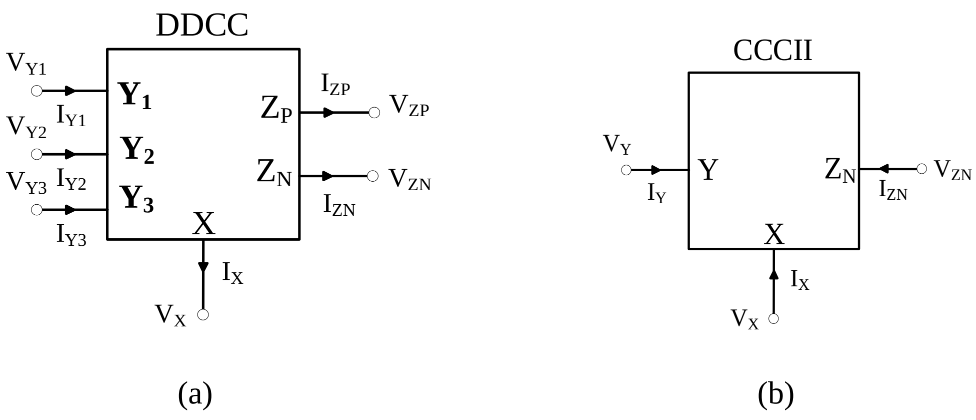

Figure 1. Circuit symbols of (a) DDCC and (b) CCCII

The terminals of the active elements have directly relationships between terminals and are shown in matrix format. The terminal characteristics of the DDCC and CCCII can be described by the following matrix equations,

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & \beta_1 & -\beta_2 & \beta_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_{p1} & 0 & 0 & 0 & 0 & 0 \\ -\alpha_{n1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{ZP} \\ V_{ZN} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} I_Y \\ V_X \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_4 & R_X & 0 \\ 0 & -\alpha_{n2} & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2)$$

where, α and β are non-ideal values of current and voltage gains, respectively. These parameters are ideally equal to unity. Regarding these equations, we designed a floating memcapacitor emulator circuit using only one DDCC, one CCCII, one multiplier, one resistor, and three capacitors. The proposed floating memcapacitor is shown in Fig. 2. The Z_P terminal is connected to the C_1 component to provide memory. Also, this terminal is connected to the Y terminal of the CCCII. The same connections are applied to the CCCII using C_2 and R_1 components. The voltage on the C_1 element is multiplied with the voltage on R_1 and C_2 elements to provide the nonlinear property of the memcapacitor. This multiplication is implemented using an ideal multiplier which is connected to the Y_1 terminal of the DDCC.

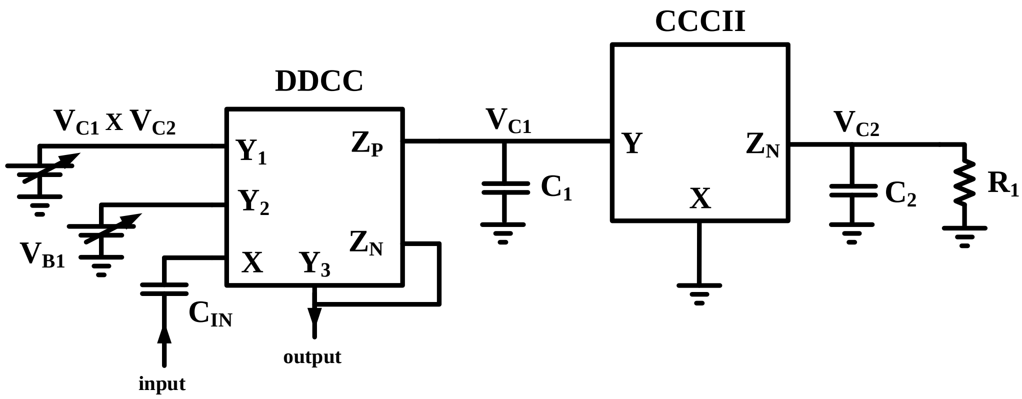

Figure 2. The proposed memcapacitor circuit schematic. C_{IN}=1nF, R_1=15k, C_1=650pF, C_2=250pF, V_{B1}=-30mV

The mathematical equations for the proposed memcapacitor are shown below. The input current, I_{IN},

$$I_{IN} = I_{OUT} = C_{IN} \frac{d(V_{IN} - V_X)}{dt} \quad (3)$$

Input voltage,

$$V_{IN} = \frac{q(t)}{C_{IN}} + V_X \quad (4)$$

The voltage of the Z_P equals to the C_1 capacitor and called V_{C1},

$$V_{C1} = \frac{1}{C_1}\int_0^t I_{ZP}dt = -\frac{1}{C_1}\int_0^t I_{IN}dt$$
$$V_{C1} = -\frac{q(t)}{C_1} \qquad (5)$$

Considering equation (1) and X terminal of CCCII is grounded so Eq. (6) becomes as below,

$$V_{Y1} = V_{C1} = -R_X I_X \qquad (6)$$

The currents for X and Z_N terminals of CCCII are given,

$$I_{ZN} = -I_X = \frac{V_{C1}}{R_X} = -\frac{q(t)}{R_x C_1} \qquad (7)$$

If a capacitor and resistor is connected parallel; the total current value is the sum of two currents so equals to (8).

$$I_{ZN} = C_2\frac{dV_{C2}}{dt} + \frac{V_{C2}}{R_1} \qquad (8)$$

First, this equation is converted to s domain from time domain. When Laplace transform is applied to this s domain equation, VC2 terminal can be obtained as,

$$V_{C2}(t) = \frac{R_1 q(t)}{R_X C_1}\left(1 - e^{-\frac{t}{R_1 C_2}}\right) \qquad (9)$$

The multiplication of VC1 and VC2 terminals,

$$V_{Y1} = V_{C1} \times V_{C2} = -\frac{R_1 q^2(t)}{R_X C_1^2}\left(1 - e^{-\frac{t}{R_1 C_2}}\right) \qquad (10)$$

Considering that the DDCC's terminal links,

$$V_X = V_{Y1} - V_{Y2} + V_{Y3}$$
$$V_X = -\frac{R_1 q^2(t)}{R_X C_1^2}\left(1 - e^{-\frac{t}{R_1 C_2}}\right) - V_{Y2} + V_{Y3} \qquad (11)$$

When a DC voltage is applied to VY2 terminal, the circuit's hysteresis offset point can be adjusted electronically. In addition, if VY3 and IZN terminals are connected to the ground, the circuit acts as a grounded memcapacitor circuit. When VY2 and VY3 terminals are grounded, VX voltage can be defined as,

$$V_X = -\frac{R_1 q^2(t)}{R_X C_1^2}\left(1 - e^{-\frac{t}{R_1 C_2}}\right) \qquad (12)$$

The inverse capacitance can be obtained as below using equation (4),

$$C_M^{-1} = D_M = \frac{V_{IN}}{q(t)} = \frac{1}{C_{IN}} + \frac{V_X}{q(t)} \qquad (13)$$

if equation (12) is substituted in equation (13), inverse capacitance is found as,

$$C_M^{-1} = D_M = \frac{1}{C_{IN}} - \frac{R_1 q(t)}{R_X C_1^2}\left(1 - e^{-\frac{t}{R_1 C_2}}\right) \qquad (14)$$

In Eq. (14), $\frac{1}{C_{IN}}$ and $\frac{R_1 q(t)}{R_X C_1^2}\left(1-e^{-\frac{t}{R_1 C_2}}\right)$ are defined as a fixed part and a variable part, respectively. Furthermore, since R_X resistor can be changed by using a biasing voltage source so, the inverse memcapacitance can be electronically controlled. Considering the proposed memcapacitor circuit, we can easily use the circuit as a floating emulator since the I_{IN} equals to I_{OUT} (Hyongsuk Kim, Sah, Changju Yang, Seongik Cho, & Chua, 2012; Yeşil, Babacan, & Kaçar, 2014). When memcapacitors are connected as serial, they behave as serial connected capacitors. The same situation is valid for parallel-connected memcapacitors. Taking into non-ideal gains of DDCC and CCCII, inverse capacitance of the proposed memcapacitor can be found as,

$$C_M^{-1} = D_M = \frac{1}{C_{IN}} - \frac{\eta \alpha_{p1} \alpha_{n2} \beta_1 \beta_4 R_1 q(t)}{R_X C_1^2}\left(1-e^{-\frac{t}{R_1 C_2}}\right) \quad (15)$$

where η is the multiplier coefficient. It can be clearly seen from equation (15) that non-ideal gains of active elements slightly change variable part of its inverse capacitance.

3. Results and Discussion

The Simulation Results of Memcapacitor Emulator Circuit

In this study, the presented memcapacitor circuit contains two active elements which are implemented MOS transistors. TSMC 0.18µm parameters are used for all MOS transistors. The circuit implementation of Furthermore, the CMOS realization of the CCCII circuit is depicted in Fig. 3(Yesil & Babacan, 2020a). The circuit's aspect ratios are given as 60µm/0.72µm for M_1-M_4 transistors, 50µm/0.72µm for M_5 transistor and 10µm/0.72µm for M_6-M_9. DDCC is shown in Fig. 4. The aspect ratios for an internal circuit of DDCC are 14µm/0.72µm for PMOS transistors and 3µm /0.72µm for NMOS transistors(Yesil, Babacan, & Kacar, 2020). The DC power supply voltages of DDCC and CCCII are selected as V_{DD}=-V_{SS}=1.25V while V_{B2} is chosen as 0V. Furthermore, in this study, the parasitic resistance seen at port X of CCCII changes from 573Ω-913Ω from V_B=-300mV to 300mV.

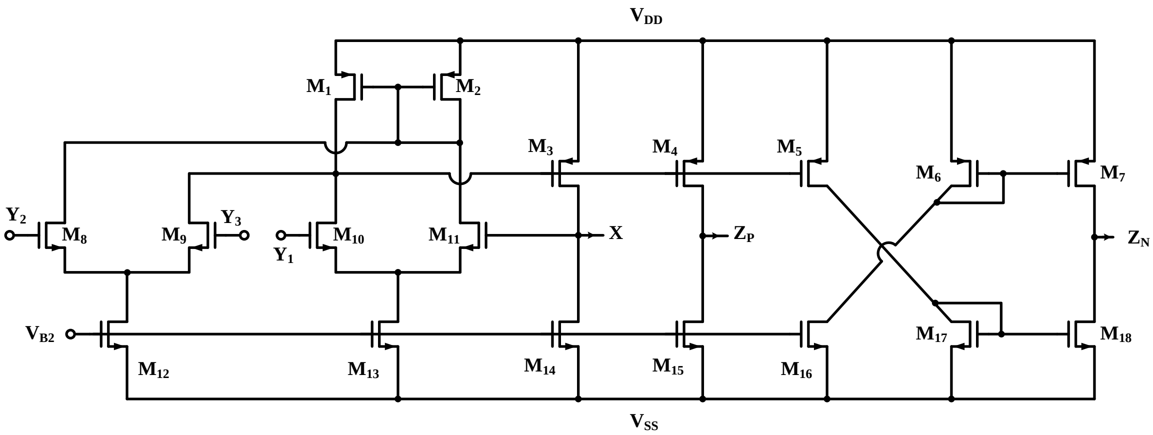

Figure 3. The MOS implementation of DDCC(Yesil et al., 2020).

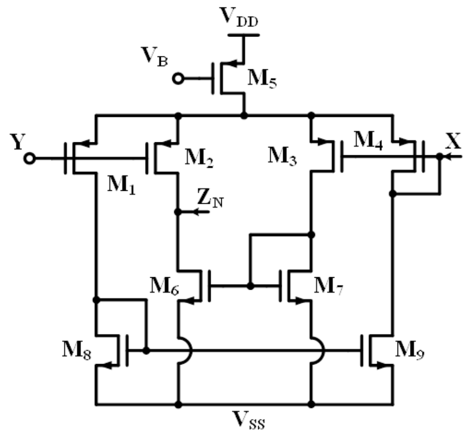

Figure 4. The internal structure of CCCII (Yesil & Babacan, 2020a)

To show the performance of the proposed memcapacitor, various simulations are investigated. Firstly, the charge change is investigated when applied periodic sinusoidal signal. As shown in Fig.5, the proposed circuit exhibits pinched hysteresis curves when applied sinusoidal signals. The amplitude of the signals is 75mV, and their frequencies are 125kHz, 150kHz, 200kHz. It can be observed from Fig. 5 that the nonlinear pinched hysteresis loops become linear with increasing frequency.

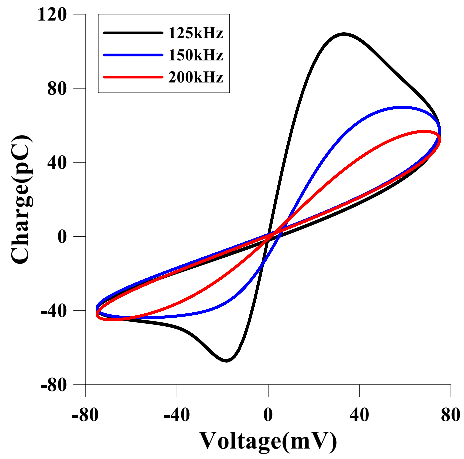

Figure 5. Charge-Voltage relationships of the proposed circuit with an applied sinusoidal signal with various frequencies.

The memcapacitor circuit is an electronically controllable property different from a real memcapacitor. This property provides directly control the memcapacitor at real-time operations. So, we can control the memcapacitor-based circuits only by changing V_B control parameter of the proposed memcapacitor emulator. As shown in Fig.6, the V_B voltage is changed from -300mV to 300mV with 300mV steps.

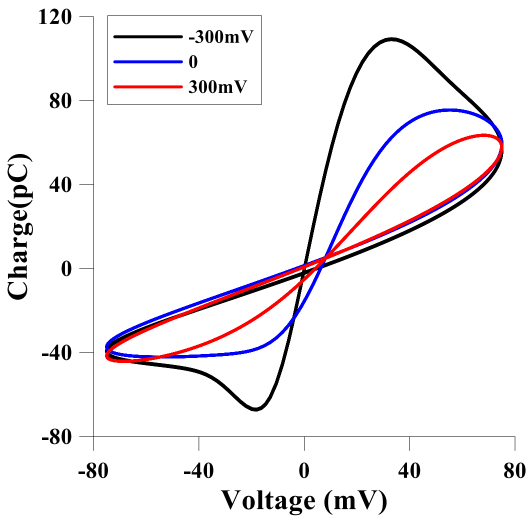

Figure 6. Charge change with applied different V_B voltages for 125kHz sinusoidal applied signal.

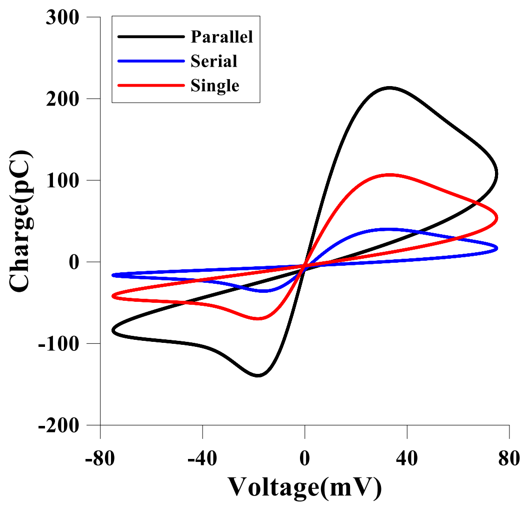

Figure 7. The voltage-charge relationships for single, paralel and serial connected memcapacitor. This curves are obtained for 125kHz input signal frequency and -300mV V_B voltage.

Grounded emulators cannot connect as serial with other circuit elements. But our emulator can be connected as a serial with other elements so we showed the charge-voltage relationship for the parallel and serial connected memcapacitor in Fig. 7.

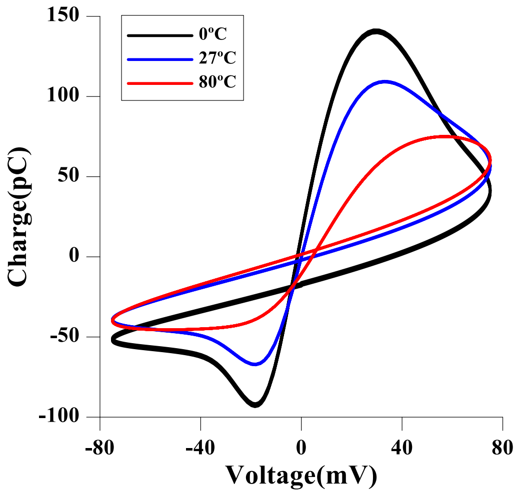

Figure 8. The voltage-charge relationships for different temperatures. Here, the applied signal frequency and V_B value are 125kHz and -300mV, respectively.

As expected, when compared single memcapacitor, more current flows through the parallel connected memcapacitors while less current flows through the serial connected memcapacitors. The temperature dependency of circuits is an important parameter for high operating performance. For this reason, we analyzed the effect of the temperature on the proposed circuit. As shown in Fig.8, we investigated the performance of our circuit at 0°C, 27°C, and 80°C environments. The increasing temperature causes the transition from hard switching behavior to smooth switching behavior of the emulator characteristic. In Fig.9, it is shown that the memcapacitor is sensitive the applied signal and signal direction when considering the charge response. Also, between the applied input pulses, as shown the charge is stable. For example, the last value of the response for the first pulse has the same value the first value of the response for the second pulse. For this reason, we can say that the emulator circuit is nonvolatile. The temperature and supply voltage directly effect the electrical performance of the circuit. As shown in Fig.10, the simulation results show that any radical changes are not observed for hysteresis loops even if temperature and supply voltages are changed in wide ranges.

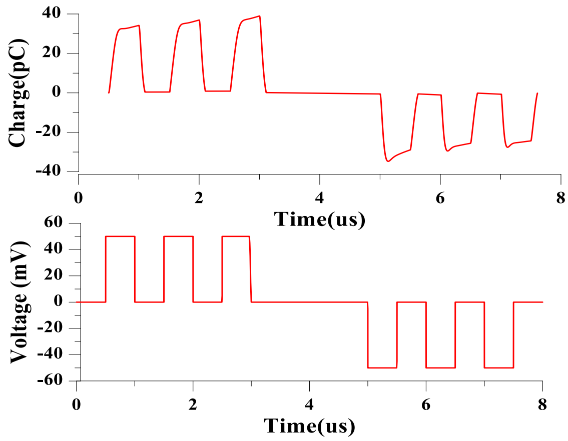

Figure 9. The charge changes of the proposed memcapacitor circuit when applied positive and negative pulse train.

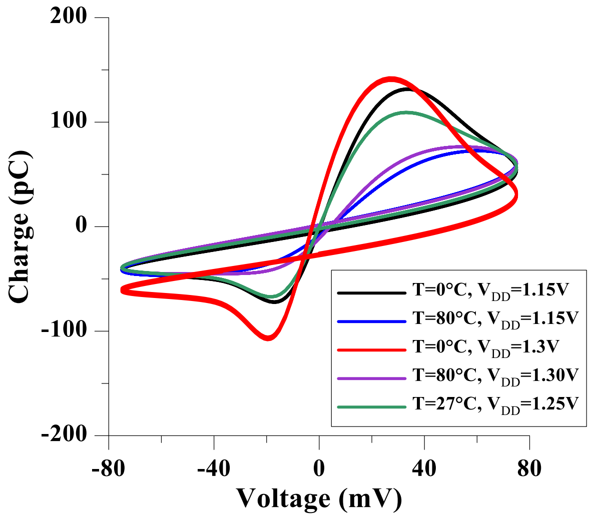

Figure 10. Hysteresis property according to temperature and supply voltage of active elements

Application of the Proposed Memcapacitor

In order to demonstrate floating feature and the performances of the proposed memcapacitor, high pass filter application is selected. Fig. 11a depicts MC-R and C-R circuits while their gain-frequency and phase-frequency responses are given in Fig. 11b.

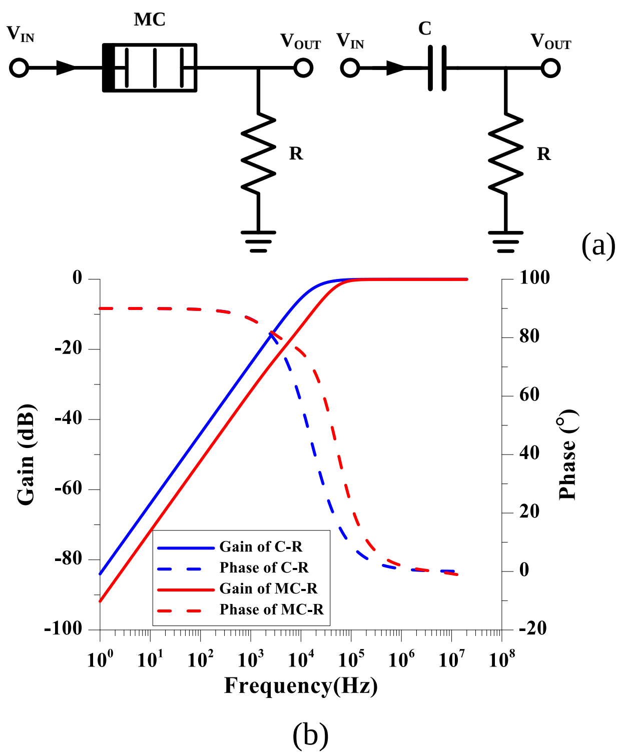

Figure 11 a) The MC-R and C-R circuits and b) Gain-phase curves according to frequency.

Values of passive elements are chosen as R=10 kΩ and C=1nF. Considering Fig. 11, the proposed floating memcapacitor circuit behaves as a floating capacitor for HPF applications. According to the number of active/passive elements, floating/grounded structures, and operating frequencies, Table 1 presents a detailed summary comparing previously proposed memcapacitors. It can be easily observed from Table 1 that the proposed memcapacitor circuit enjoys the following advantageous features; floating structure, low number of active and passive elements and electronically tunable.

Table 1. Summary of several studies on literature

References	Number of Active Elements	Number of Passive Elements	Floating / Grounded	Operating Frequency	Electronically Controllable
(Madsar et al., 2020)	1	2	Grounded	1-7Hz	No
(Yesil & Babacan, 2020b)	3	4	Grounded	500-2kHz	Yes
(Konal & Kacar, 2021)	3	4	Grounded	1-10Hz	Yes
(Sah et al. 2013)	4+Memristor	2	Floating	100-900 Hz	No
(Yu et al. 2013)	4+ Memristor	3	Floating	12-1000Hz	No
This work	3	4	Floating	125kHz-200kHz	Yes

4. Conclusion

In this paper, we presented an electronically controllable active circuit element-based memcapacitor emulator circuit. Many memcapacitor emulators have grounded structures and cannot connect as serial with other circuit elements. For this reason, memcapacitor emulators which have grounded structures are used in limited applications. But the proposed emulator can be connected as both parallel and serial besides simple structure. Also, the circuit is electronically controllable behavior by changing V_B voltage sources. All simulation results are obtained using TSMC 0.18 micron parameters and compatible with real memcapacitive behavior.

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Ethics in Publishing

There are no ethical issues regarding the publication of this study.

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