FPGA-based ANN Design for Detecting Epileptic Seizure in EEG Signal

B. Karakaya, T. Kaya and A. Gulten

***Abstract*—This study aims to represent an FPGA (Field Programmable Gate Array) design of Artificial Neural Network (ANN) for Electroencephalography (EEG) signal processing in order to detect epileptic seizure. For analyzing brain's electrical activity, feedforward ANN model is used for classification of EEG signals. The designed ANN output layer makes a decision whether the person has epilepsy or not. In the proposed system, the ANN model is programmed and simulated on Xilinx ISE editor via computer and then, EEG signal data are transferred to FPGA-based ANN emulator core. The Core is trained on data which are patient's data and healthy person's data. After training, test data is loaded to ANN Emulator Core to detect any epileptic seizure of person's EEG signal. The main advantage of FPGA in the system is to improve speed and accuracy for epileptic seizure detection.**

Index Terms—**ANN, EEG, FPGA, Epilepsy.**

I. Introduction

ELECTROENCEPHALOGRAM (EEG) which is obtained from recording of brain's electrical activity is important data to analyze brain's normal and abnormal activities. Epilepsy that is significant disease of brain is a chronic disease which causes sensory loss, unbalanced deictic gesture or muscular contraction comprised by abnormal activity of a group of neuron in brain. On the recognition of this disease, analysis of EEG has great importance [1].

In the analysis of EEG signal, many methods are used. In [2], high frequency and low frequency noise were suppressed by moving average and derivative-based filter. This method was used to classify normal or epileptic EEG signals. In [3], the user interface program was generated in Laboratory Virtual Instrument Engineering Workbench (LabVIEW) that has visual programming language in order to analyze EEG signals in determination of sleep stages. EEG signals can be analyzed in two domains. Due to the characteristic of signal in frequency domain, signal differs from before, during and after attack. Analyzing the characteristic of signal in time domain gives better result.

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In literature, there are many studies which are based time domain but the best one is Wavelet Transform Technique on epileptic seizure detection [4], [5]. There are also classification studies of EEG signal by using ANN model. In [6], the design of a new window function that has side-lobe roll-off ratio characteristic of ultra-spherical window and Kaiser Window's main-lobe width and ripple ratio was obtained by helping ANN. ANN model can be used for pattern recognition as well as EEG signal processing and classification [7], [8].

In literature, there are few studies on classification of EEG signals based on FPGA using neural network algorithms. One of them has two neural network algorithms that are implemented with the best accuracies into FPGA which achieves on 68% accuracy for MIT-BIH data and 70% accuracy for Mitra data [9]. In [10], simulation platform is introduced and starting from simulation in the learning phase with fixed-point operators, a methodology has been developed that is able to realize EEG signal processing with ANN model. The aim of this paper is to process EEG signal that is filtered in time domain by using ANN architecture, increase operating frequency and parallel processing ability of design. Furthermore, designed ANN model is programmed on FPGA and then signal is classified. ANN is preferred for its speed and parallel processing ability. Also, ANN can solve complex mathematical problems in real-time based on observations.

II. Materials and Methods

A. The Study Area

Nowadays, new disease recognition implementations attract researcher's attention who work in hospitals and biomedical device industry because of faster and more accurate results requirement.

In this study, three groups of data [11] are formed from pre-processed EEG signal. These are patient's data, healthy person's data and test data. ANN is trained by transferring patient's data and healthy person's data to FPGA-based ANN Emulator Core and processing respectively. After training, test data is loaded to ANN Emulator Core on Xilinx ISE simulator to detect any epileptic seizure of person's EEG signal.

B. The Experimental Design

This simulation study is named as FPGA-based ANN Emulator Core and illustrated in Figure 1. ANN Emulator Core consists of two parts. They are Adder and Multiplier

circuits. EEG data that are obtained from patient and healthy person, are filtered and normalized -1 to 1. These data must be transformed to a binary number format which has to be in fractional mode. Therefore, fixed-point number format is chosen. Numbers are arranged as 16 bit in width and quantized in the range of -1 to 1.

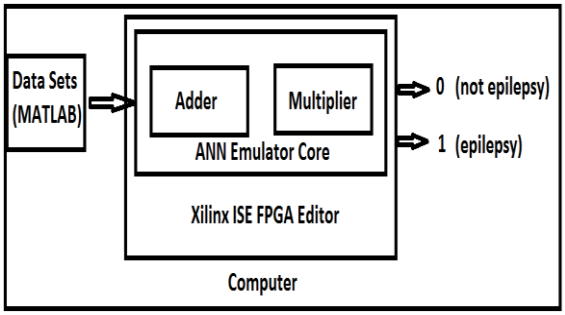

Fig. 1. A scheme of FPGA-based ANN Emulator Core Design.

Fixed-point number format is symbolized as Qm.n where m and n stand for integer part and fractional part of number respectively. All numbers for this design are used as signed form. Therefore, 1 bit is reserved for sign bit. Finally, number representation format is organized as Q2.13 16 bit signed fixed-point format for MATLAB. In this case, the precision of numbers is obtained as 0,122. 10-4.

Network that is programmed in the study is shown in Figure 2. As shown in Figure 2, ANN model has 4 inputs, 1 hidden layer, 1 output layer and 2 activation functions with input, bias and coefficient weightiness. ANN model is trained toward given inputs and weightiness by solving these equations below.

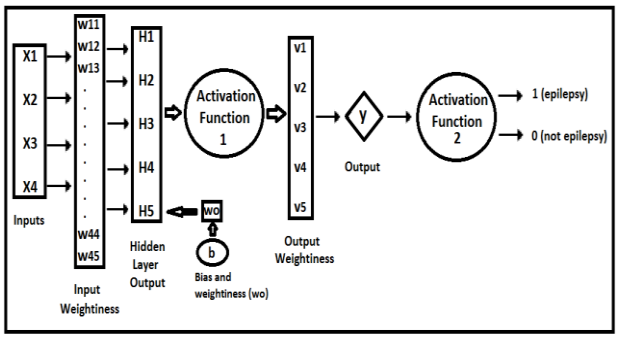

Fig. 2. Artificial Neural Network Processor Design.

$$
\begin{aligned}
H_1 &= x_1 * w_{11} + x_2 * w_{21} + x_3 * w_{31} + x_4 * w_{41} + b * wo_1 \\
H_2 &= x_1 * w_{12} + x_2 * w_{22} + x_3 * w_{32} + x_4 * w_{42} + b * wo_2 \\
H_3 &= x_1 * w_{13} + x_2 * w_{23} + x_3 * w_{33} + x_4 * w_{43} + b * wo_3 \\
H_4 &= x_1 * w_{14} + x_2 * w_{24} + x_3 * w_{34} + x_4 * w_{44} + b * wo_4 \\
H_5 &= x_1 * w_{15} + x_2 * w_{25} + x_3 * w_{35} + x_4 * w_{45} + b * wo_5
\end{aligned} \tag{1}
$$

Activation function 1 is given as below

$$
H_{(i)} = \begin{cases} -1, \ldots\ldots, H_{(i)} < -1 \\ H_{(i)}, \ldots\ldots, |H_{(i)}| \le 1 \\ 1, \ldots\ldots, H_{(i)} > 1 \end{cases} \tag{2}
$$

and concluding calculation is y_{net}.

$$
y_{net} = H_1 * v_1 + H_2 * v_2 + H_3 * v_3 + H_4 * v_4 + H_5 * v_5 \tag{3}
$$

Activation function 2 is given as below

$$
y = \begin{cases} 1, \ldots\ldots, y_{net} > 0 \\ 0, \ldots\ldots, y_{net} < 0 \end{cases} \tag{4}
$$

and decision is determinated as,

$$
error = y_{desired} - y \tag{5}
$$

if error is greater than required error limit, all weightiness are updated as below equations where α is training parameter. Then, ANN model is reworked with new weightiness. If not, y is the correct output.

$$
\begin{aligned}
\Delta w &= error * input(j) * w(i, j) \\
w &= w + \alpha * \Delta w \\
\Delta v &= error * H(i) * v(i) \\
v &= v + \alpha * \Delta v \\
\Delta wo &= error * wo(i) \\
wo &= wo + \alpha * \Delta wo
\end{aligned} \tag{6}
$$

Arithmetic circuits in the design that are Adder and Multiplier Circuits are coded and synthesized on Xilinx ISE FPGA Editor. These two arithmetic circuits give the response in 2 clock cycles. Figure 3 illustrates port information of arithmetic circuits [12].

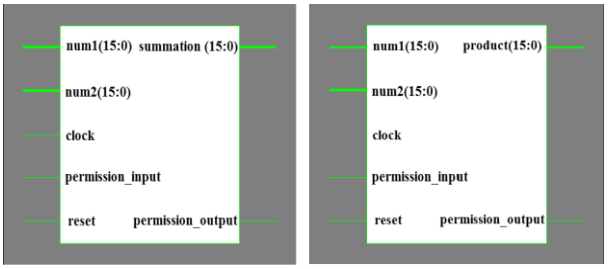

Fig. 3. Adder & Multiplier Circuit of ANN Emulator Core [12].

Arithmetic circuits begin to work with *permission_input* signal. After addition or multiplication operation, arithmetic circuits send *permission_output* signal with result in order to indicate that circuits are ready for new calculation.

Table 1. Resource utilization and latencies of Adder and Multiplier circuits [13].

	Adder	Multiplier
Used Logic Slices	9	35
Used Flip-Flops	1	20
Used LUTs	18	61
Latency	2	2

Table 1 represents resource utilization and latencies of Adder and Multiplier circuits which are used for ANN Core design. Table 2 represents resource utilization of ANN Core design overall.

Table 2. Resource utilizations of ANN Core design.

Used Logic Slices	9255
Used Flip-Flops	11246
Used LUTs	17149

III. RESULTS

In the simulator screen, clock cycle is selected as 100 Mhz. Total clock cycle that is needed to complete emulation of signal is 136. It means total time that is needed for emulation is 1360 ns. After training completed by using ANN model above, patient's and healthy person's data are implemented to the emulator core respectively. It is required that when a group of patient's data are applied to the core, it must give a result of 1 while in the case of healthy person's data, it is 0. Figure 4 shows the outcome of ANN Core when a group of healthy person's data are applied to the core. Figure 5 shows the outcome of ANN Core when a group of patient's data are applied to the core. Figure 6 shows the outcome of ANN Core when a group of healthy person's data are applied to the core, but in this case ydesired is selected as the person has epilepsy. Therefore, well-trained ANN gives an error as 1. Because the person is healthy.

In outcomes of ANN Emulator Core, y[15:0] represents output of the ANN model that is used for detection of seizure on EEG signal. e_hata[15:0] represents error of the ANN model calculation that is used for recalculation of weightiness if it is greater than 0. ydesired[15:0] is used for if it is 1, it means the signal is belong to epilepsy patient. If it is 0, it means the signal is belong to healthy person.

The accuracy of the study can be determined by using Mean Square Error (MSE) algorithm after signal progressed. A MATLAB function is created and the design achieves on 86.7% accuracy of detection epilepsy event.

IV. CONCLUSION

As a result of this study, it is proven that EEG signal can be classified as normal or epileptic by using ANN Core design on FPGA platform with more accuracy. Furthermore, the total required time to classify EEG signal is 1360 ns. Maximum operating frequency is obtained as 82 MHz from Xilinx Synthesis Tool. The speed of real-time implementation may change respect to design.

ANN Core design can be updated and implemented in real-time on FPGA. Furthermore, fixed-point arithmetic can be arranged as obtaining better precision.

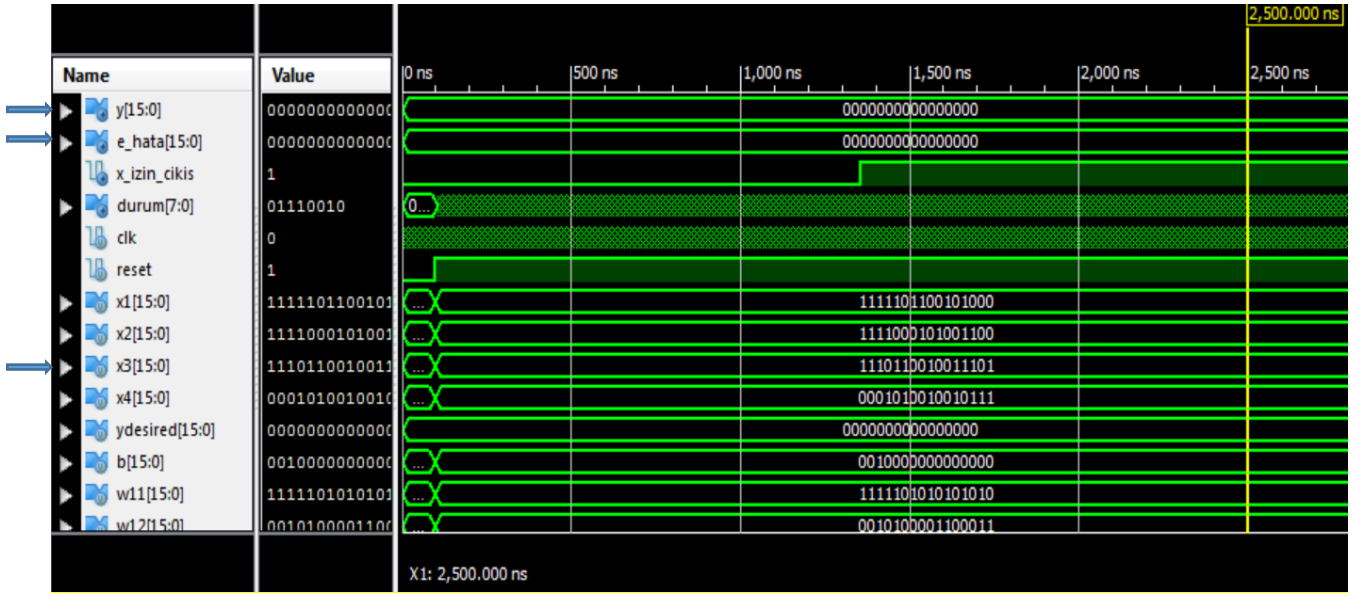

Fig. 4. Outcome of the Core when ydesired= 0, y= 0 and error=0.

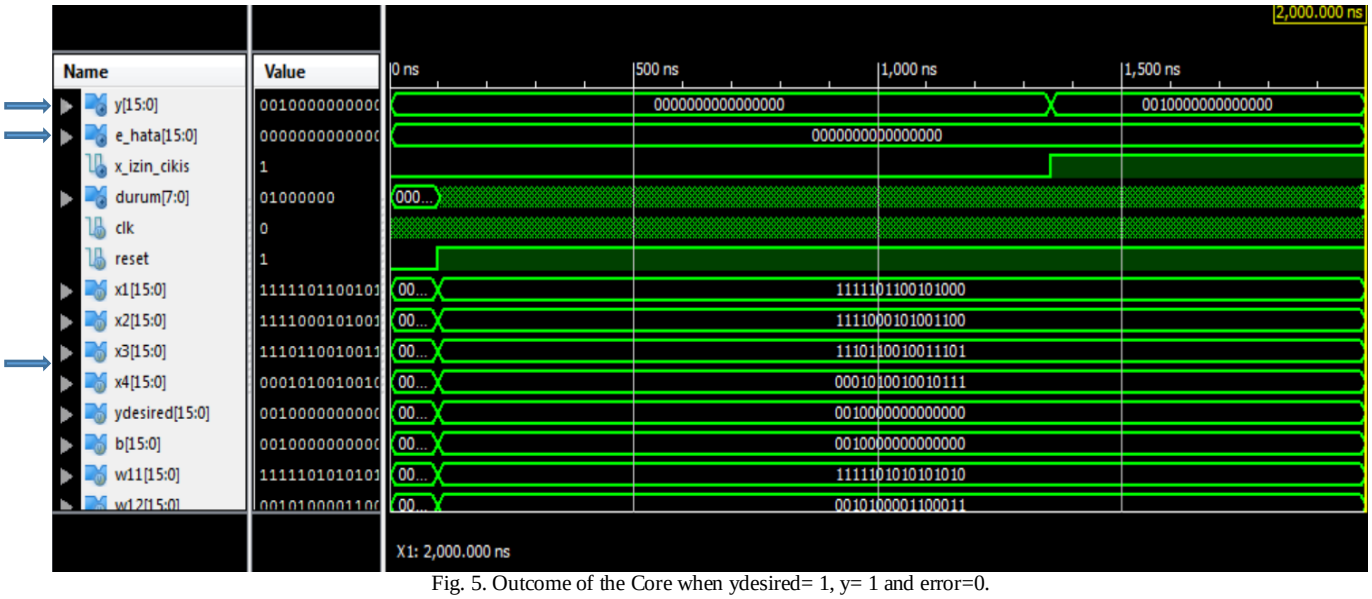

Fig. 5. Outcome of the Core when ydesired= 1, y= 1 and error=0.

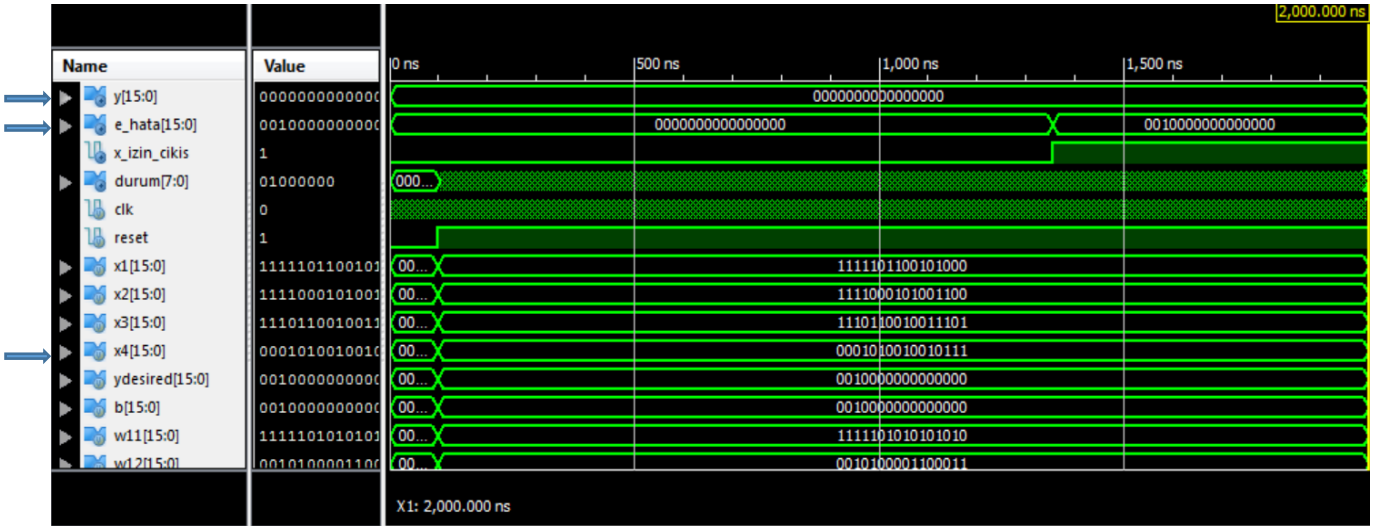

Fig. 6. Outcome of the Core when ydesired= 1, y= 0 and error=1

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