A New Topology for UPQC Based on Reduced-Switch-Count Converter

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ABSTRACT

Recently, reduced switch count converter switch numerous advantages such as low cost and weight, small size and high reliability have been introduced to be used in unified power quality conditioner (UPQC). In this paper a novel topology for UPQC based on back-to-back B4 converter and its control system are proposed. The conventional UPQC consists of twelve switches while the proposed topology for UPQC has 8 switches. By reducing the number of switches, the price of the whole system and losses are decreased. In addition, the proposed control system can be used in conventional UPQC when one of converter legs has a faulty condition. This increases reliability of the system. Special control and modulation schemes have been offered to compensate oscillations in load and utility currents and voltages and also input power factor of UPQC. The experimental and simulation results verify the efficiency of proposed control and modulation schemes of proposed topology.

Keyword: Unified Power Quality Conditioner (UPQC), Reduced Switches Count Converter, B4 Inverter

1. INTRODUCTION

Nowadays, increasing interest for efficient non-linear loads like rectifiers, inverters, adjustable speed drives and etc. has increased harmonic current injection to the utility that has caused great concerns about other customers and grid. In recent years, usage of sensitive devices has been increased that need high quality power supply. Temporary interrupts, voltage distortions and other power quality issues has destructive effects for the modern and sensitive loads. Recently, power quality issues have become a major problem for utilities and customers [1-4]. The unified power quality conditioner (UPQC) is one of the most important and effective custom power devices which has a wide ability to solve most of power quality problems [5-11]. UPQC consists of a shunt and a series converters with common DC-link. Therefore, this device can compensate all of voltage and current distortions, such as voltage sag and swell, poor power factor, current and voltage harmonics and etc. The role of series converter is to inject a series voltage into the line in order to compensate the harmonic, unbalance and other voltage distortion at source side. Therole of shunt converter is to compensate the currents unbalance and harmonics of the load current and power factor and to regulate DC-link voltage. Reduction of the number of switches is one of the ways to reduce UPQC cost. In order to reach this purpose, a UPQC topology based on nine-switch converter has been presented in [12]. The nine-switches-double-output converter can operate in different frequency (DF) and constant frequency (CF) modes. In DF mode, the sum of modulation indexes of two outputs equals to one. Since in
the UPQC applications, the injected voltage by series converter is small, about 0-0.3 p.u., though the modulation index for series converter will be small. But the output voltage of shunt converter should be greater than the grid voltage. Therefore, for proper operation of UPQC based on nine-switch converter, the DC-link voltage should be considerably increased. An alternative concept is proposed in this paper, where the four switch converter is chosen to replace a shunt and a series converter found in conventional twelve switch power conditioner. The B4 converter uses four switches to form two phase legs with its third phase drawn from the midpoint of a split dc capacitive link. For tying two ac systems together, two B4 converters as a proposed converter are needed with their split dc link shared. The total number of switches in the proposed converter is eight, which probably is the minimum achievable for interfacing two ac systems. Two sets of control schemes are designed for the proposed topology. The first control schemes are proposed to compensate for harmonic currents, reactive power flow and three-phase unbalance caused by nonlinear loads is proposed to proposed converter. With the proposed method, the grid currents drawn from the utility are then sinusoidal, having only fundamental component. Also, the second control scheme which is the series inverter control, are designed to compensate for any detected grid voltage harmonics and unbalance, so that only a set of balanced three-phase voltages appears across the loads under normal operating conditions. During voltage sags, the series inverter control scheme also has the ability to continuously keep the load voltages within tolerable range.

This paper is composed of seven sections. In second section, the proposed topology and its modulation method is presented in details. In third section, proposed control methods for series and shunt converters are presented. After introducing the proposed topology and control methods, in fourth section, the switching losses are calculated. In next section, the simulation results for different operation conditions are presented. Sixth section presents the experimental results. These results confirm the proper operation of proposed topology, modulation method, control system and verify simulation results. Finally, the last section is dedicated to conclusion.

2. PROPOSED TOPOLOGY AND MODULATION METHOD

UPQC based on the conventional back-to-back converter, in which one of the legs in series and shunt converters is eliminated, is shown in Fig. 1. In proposed topology for UPQC, instead of using B6 inverter, B4 inverter is used.

![Fig. 1: UPQC based on conventional back-to-back structure](image)
Fig. 2 shows the circuit diagram of proposed topology of UPQC based on back-to-back B4 converters. The number of switches in proposed topology is eight while it is twelve in the conventional topology. Therefore, due to less number of switches in proposed topology, the cost of UPQC for low voltage applications (low voltage distribution system) and switching losses will be lower in comparison with conventional topology.

2.1. B4 Inverter Structure

In low voltage application, the reduced switch count topologies have attracted a great attention in industry. The most well-known reduced switch count topology is B4 converter which was introduced by Van Der Broeck[13]. Fig. 3 shows so-called B4 inverter with four switches and three output phases. In this structure, one leg of conventional three-phase inverter have been eliminated and replaced with two series capacitors. In this case the third phase of inverter is connected to the mid-point of series capacitors.

Fig. 3: Four-switch B4 converter
There are two methods for B4 inverter’s switching [13, 14-17]:
1. Carrier Based Pulse Width Modulation (CBPWM)
2. Space Vector Modulation (SVM)

2.1.1. Carrier Based Pulse Width Modulation (CBPWM)

This inverter has two legs. Consequently in this modulation method, two reference signal is required. The reference signal of B4 inverter in the UPQC structure, are generated using shunt and series controllers. Since, line voltage of converter is controllable, these references which are defined as follows and are shown in Fig. 4:

\[ V_{ref,ba} = m\sin(\alpha t) \]  \hspace{1cm} (1)

\[ V_{ref,ca} = m\sin(\alpha t + \frac{\pi}{3}) \]  \hspace{1cm} (2)

Where \( m \) is modulation index and \( \Omega \) is the output voltage angular frequency. As it can be seen in Fig. 5, these signals are compared with carrier signal and the logical results of the comparison define the gate pulses. If the reference signal is greater than carrier signal, the upper switch of each leg is turned on. If not, the lower switch of each leg is turned on.

![Fig. 4: Reference signal for B4 inverter](image1)

![Fig. 5: CBPWM switching method for B4 inverter](image2)

Consequently, the maximum phase output voltage (\( u_m \)) by SVM method is the same as CBPWM and can be calculated as [16]:

\[ U_m = \frac{1}{\sqrt{3}} \frac{V_{dc}}{2} \]  \hspace{1cm} (3)

This value is equal to phase voltage amplitude where the modulation index of PWM method is considered to be one. Like conventional B6 inverter, the B4 inverter operates as a step-down converter but in comparison with B6 inverter, it can be seen that the output voltage of B4 inverter has decreased by a factor of \( \sqrt{3} \).

With assuming the same load for both converters, a comparison between B6 and B4 converters is derived as follows:

1. Less number of switches in B4 structure causes the lower cost in low voltage applications than B6 inverter.
2. With same output voltage, the maximum peak inverse voltage (PIV) for switches in B4 converter will be more than B6 converter.
3. Due to less number of switches in B4 converter, the conduction losses of B4 converter
3. B4 INVERTER’S CONTROL SCHEME IN THE PROPOSED UPQC

In this paper, the synchronous reference frame theory is supplied as a control system of proposed UPQC. The CBPWM and hysteresis methods are used as modulation methods of series and shunt B4 converters, respectively. Different types of carrier-based modulation methods are introduced in [18].

UPQC control system consists of two subsystems [19]:

- Shunt inverter control system.
- Series inverter control system.

Shunt inverter’s control system, based on synchronous reference frame theory, is shown in Fig. 6(a). \( i_{sa}, i_{sb} \) and \( i_{sc} \) are load currents and \( v_{sa}, v_{sb} \) and \( v_{sc} \) are source voltages. The synchronous reference frame transformation (Park’s transformation) is used to transform the measured load currents into dq0 frame. Direct and quadrature components of load current can be decomposed into AC and DC components. These components are separated by a low-pass filter.

\[
\begin{align*}
    i_{ld} &= \tilde{i}_{ld} + \Delta i_d^* \\
    i_{dq} &= \tilde{i}_{dq} + \Delta i_q^*
\end{align*}
\]

(4)

For factor correction and load current harmonics compensation, the reference currents of shunt converter are calculated as follows:

\[
\begin{align*}
    i_{fd} &= \tilde{i}_{fd} \\
    i_{fq} &= \tilde{i}_{fq} + i_{iq}
\end{align*}
\]

(5)

After injecting the reference currents by shunt converter, the utility side currents will be as follows:

\[
\begin{align*}
    i_{sd} &= \tilde{i}_{dq} \\
    i_{sq} &= 0
\end{align*}
\]

(6)

Due to power losses and series inverter’s real power injection, DC-link voltage fluctuates. Thus, a PI controller is used to regulate the DC-link voltage (Fig. 6(a)).

![Diagram](image_url)
By injecting or absorbing active power through the utility, the shunt converter regulates the DC-link voltage. The PI controller output, $\Delta i_{dc}$, is added to $d$ component of reference current. Finally, the dq components of reference current can be stated as follows:

$$i_{cd}^* = i_{ld} + \Delta i_{dc}, \quad i_{cq}^* = i_{lq}$$ (7)

As seen in Fig.6(a), the reference currents in synchronous reference frame are transformed to abc components using the inverse park’s transformation. Difference between the reference currents ($i_{fa}^*, i_{fb}^*, i_{fc}^*$) and output currents of shunt inverter ($i_{fa}, i_{fb}, i_{fc}$) are fed to hysteresis current control block that produces gate signals for shunt inverter’s switches.

Load side voltage control is done through the series B4 inverter of UPQC. The control system of series B4 inverter is used to calculate reference signals in order to compensate the voltage unbalance and distortions. The control system for Series inverter is illustrated in Fig. 6(b). In order to preserve the load voltage at its constant value, reference voltage is compared with direct component of load voltage. Regarding, error is defined as the difference between the injected reference voltage and the measured voltage.

It is obvious that the controllability of the system can be enhanced, if the error value decreases. In this regards, the obtained error is multiplied by $k$ and then is added to injected reference voltage. The series connected converter is controlled as a two phase system, because it composed by two legs. The required switching pulses for each switch are produced by using PWM method. The values of decrease in are listed in table (2).

<table>
<thead>
<tr>
<th>Table 2: values parameters control</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Shunt converter</strong></td>
</tr>
<tr>
<td>$k_p$</td>
</tr>
<tr>
<td>0.5</td>
</tr>
</tbody>
</table>

4. LOSS CALCULATION FOR PROPOSED TOPOLOGY

In the proposed topology for UPQC the number of switches is reduced. It should be noticed that PIV of the switches is increased, in return. Converter’s losses ($P_L$) can be divided to conduction loss ($P_{con}$) and switching loss ($P_{sw}$). Conduction loss is due to the non-ideal current–voltage characteristic of semiconductors (diodes and IGBTs) and switching loss is due to drastic changes of current and voltage in switching intervals [20, 21].

4.1. Conduction Losses

Conduction loss of IGBT can be calculated using the equivalent circuit of IGBT in the state of being on. This circuit consists of a DC voltage source ($u_{CEO}$) which represents the IGBT on-state zero-current collector-emitter voltage and a collector-emitter on-state resistance ($r_C$)

$$u_{CE}(i_C) = u_{CEO} + r_C i_C$$ (8)

The same definition can be used for the anti-parallel diode:
\[ u_D (i_D) = u_{D0} + r_D i_D \quad (9) \]

The instantaneous value for IGBT conduction loss can be written as:

\[ P_{CT}(t) = u_{CE}(t)i_C(t) = u_{CE0}i_C(t) + r_C i_C^2(t) \quad (10) \]

Defining the average current of IGBT as \( I_{\text{avg}} \), and its rms value as \( I_{\text{rms}} \), the average conduction loss of IGBT can be expressed as follows:

\[ P_{CT} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_C(t) dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{CE0}i_C(t) + r_C i_C^2(t)) dt = u_{CE0}I_{\text{avg}} + r_C i_{\text{rms}}^2 \quad (11) \]

And instantaneous value of the diode conduction losses is:

\[ P_{CD}(t) = u_D(t)i_D(t) = u_{D0}i_F(t) + r_D i_F^2(t) \quad (12) \]

If the average and rms values of diode current are considered as \( I_{\text{avg}} \), and \( I_{\text{rms}} \), then conduction loss for diode during the switching period \( (T_{sw}) \) will be calculated as follows:

\[ P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_D(t) dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{D0}i_D(t) + r_D i_D^2(t)) dt = u_{D0}I_{\text{avg}} + r_D i_{\text{rms}}^2 \quad (13) \]

### 4.2. Switching Losses

The turn-on energy losses in IGBT \( (E_{\text{onT}}) \) can be calculated as the sum of the switch-on energy without taking the reverse recovery process into account \( (E_{\text{onT}}) \) and the switch-on energy caused by the reverse-recovery of the free-wheeling diode \( (E_{\text{onTr}}) \):

\[ E_{\text{onT}} = \int_{t_o}^{t_r + t_{ru}} (u_D i_D(t)) dt = E_{\text{onT}_I} + E_{\text{onTr}} \quad (14) \]

The peak value of the reverse-recovery current can be calculated as:

\[ I_{\text{Drpeak}} = \frac{2Q_{rr}}{t_{rr}} \quad (15) \]

Great portion of turn-on energy in the diode consists of the reverse-recovery energy \((E_{\text{onDr}})\):

\[ E_{\text{onD}} = \int_{0}^{t_o + t_{ru}} (u_D(t)i_F(t)) dt \approx E_{\text{onDr}} = \frac{1}{4} Q_{rr} U_{Drr} \quad (16) \]

Where, \( U_{Drr} \) is the diode voltage during reverse recovery interval. For the worst case calculation this voltage can be approximated with DC-link voltage \( (U_{\text{Di}}) \). The turn-off energy loss for IGBT can be calculated in the similar manner which is mentioned in calculating the turn on energy losses. The turn-off losses for the diode is normally neglected \( (E_{\text{offT}} = 0) \). Therefore:

\[ E_{\text{offT}} = \int_{0}^{t_o + t_{ru}} u_{ce}(t)i_D(t) dt \quad (17) \]

The switching loss for IGBT and diode can be calculated as product of switching energies and the switching frequency \( (I_{sw}) \) like:

\[ P_{\text{onI}} = (E_{\text{onI}} + E_{\text{offI}}) f_{sw} \]

\[ P_{\text{onD}} = (E_{\text{onD}} + E_{\text{offD}}) f_{sw} \approx P_{\text{onD}} = E_{\text{onD}} f_{sw} \quad (18) \]

Power losses in IGBT and free-wheeling diode can be expressed as sum of the conduction and switching losses which results in:

\[ P_I = P_{\text{onI}} + P_{\text{offI}} = u_{CE0}i_{\text{avg}} + r_C i_{\text{rms}}^2 + (E_{\text{onT}} + E_{\text{offT}}) f_{sw} \]

\[ P_D = P_{\text{onD}} + P_{\text{offD}} = u_{D0}i_{\text{Davg}} + r_D i_{\text{Drms}}^2 + E_{\text{onD}} f_{sw} \quad (19) \]

### 5. Simulation Results

In this study, power circuit consists of a 3-phase 3-wire system with non-linear load which is composed of a three phase diode rectifier with RL load. The parameters of the system and load are presented in Table 3.
In the proposed topology, the third phase of both shunt and series converter is connected to DC-link mid-point. In this study, the capacitance of both capacitors has been considered to be 2000µf. Increasing the capacity of capacitors causes to slow dynamic response and a decrease in capacitor voltage ripple. Some disturbances such as sag, swell, harmonic (i.e., 5, 7 and 11) and flicker are considered to evaluate the operation of the suggested UPQC topology. The detailed properties of these disturbances are given in Table 4. The source side voltage, load side voltage and injected voltage through the series inverter of UPQC for four types of above mentioned disturbances are shown in Figs. 7. (a)-(d). As it can be seen from these figures, UPQC’s series inverter compensates the load side voltage properly and turns it into balanced sinusoidal three-phase voltages. The presented simulation results show that the utility side disturbances are not observed at load side voltage.

Table 4: Characteristics of utility side disturbance

<table>
<thead>
<tr>
<th>Disturbances utility side</th>
<th>Occurred time</th>
<th>Amplitude voltage</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sag</td>
<td>0.5-0.6 s</td>
<td>62v</td>
<td>50Hz</td>
</tr>
<tr>
<td>Swell</td>
<td>0.7-0.8 s</td>
<td>62v</td>
<td>50Hz</td>
</tr>
<tr>
<td>Flicker</td>
<td>0.9-1 s</td>
<td>70v</td>
<td>20Hz</td>
</tr>
<tr>
<td>harmonic</td>
<td>1.1-1.2 s</td>
<td>30, 50, 70v</td>
<td>550, 350, 250Hz</td>
</tr>
</tbody>
</table>

Fig. 7: Source side voltage, Injected voltage by series inverter of proposed UPQC, load side voltage for different disturbances in the utility side
(a) sag  (b) swell  (c) flicker  (d) harmonic
In order to show the proper operation of UPQC’s shunt inverter, a non-linear load which consists of a diode rectifier with RL load, connected to the utility is considered. In this case the THD of non-linear load’s currents is more than 17%. The source side current, load side current and injected current by UPQC’s shunt inverter are represented in Figs. 8(a)-(d) for four types of disturbances in source side voltages. The presented results show that with good performance of UPQC’s shunt converter, the source side current are almost free of harmonics and in phase with source side voltages (Fig. 9(a)) and the reactive power which is required by load is provided by UPQC. Fig. 9(b) shows the utility side and load side reactive powers.

According to (7), voltage gain of B4 converter is $\frac{1}{\sqrt{3}}$ times of conventional back-to-back converter. Therefore, to generate a voltage with same amplitude in two topologies, the DC-link voltage in B4 structure should be increased up to $\sqrt{3}$ times. The DC-link voltage under different disturbances is shown in Fig. 9(c). It can be seen from this figure that the DC-link voltage is properly regulated at its reference value 1100V due to proper operation of presented DC-link voltage controller.
One of the important parameters in power quality issues is THD of load voltages and source currents. The THD and amplitude of fundamental component of load voltage and source current under different disturbances such as sag, swell, flicker and distorted source voltage are given in Table 5 when the suggested UPQC is installed.

The results of Fourier analysis (FFT) indicate that THD of source side current, depending on the type of disturbance, reaches a value within 6.25-11.35%. It should be noted that this value has been improved respect to the THD of pre-compensated load current (17%). The data presented in this table shows that the value of THD for load side voltage and utility side current meet power quality standards [1].

Table 5: THD and amplitude of fundamental component of load voltage and source current in different disturbances

<table>
<thead>
<tr>
<th>INDEX</th>
<th>Sag</th>
<th>Swell</th>
<th>Flicker</th>
<th>Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Voltage</td>
<td>THD</td>
<td>2.71%</td>
<td>2.57%</td>
<td>3.49%</td>
</tr>
<tr>
<td></td>
<td>Fundamental</td>
<td>313.5 (V)</td>
<td>308.2 (V)</td>
<td>311.1 (V)</td>
</tr>
<tr>
<td>Source Current</td>
<td>THD</td>
<td>5.34%</td>
<td>4.25%</td>
<td>7.35%</td>
</tr>
<tr>
<td></td>
<td>Fundamental</td>
<td>50.96 (A)</td>
<td>31.71 (A)</td>
<td>40.68 (A)</td>
</tr>
</tbody>
</table>

To calculate the switching losses in UPQC based on the back-to-back converter, nine-switch converter and proposed topology, the equation (23) is used. The required parameters for loss calculation are given in [22]. The results for power losses calculation for back-to-back, nine-switch and proposed topology are presented in Table 6. The load and source parameters are considered to be same for three topologies.
Fig. 10 shows the converter proposed efficiency curves obtained for load different. The nominal power of load is considered as 14kw for active power and 7kvar for reactive power. The maximum efficiency 97.5% is achieved at 0.6 p.u. load condition.

6. EXPERIMENTAL RESULTS

For implementing a prototype of proposed UPQC, based on back-to-back B4-converter, the BUP400D [23] and HCPL316j[24] are used as power IGBT and IGBT drivers, respectively and the control system is implemented on aTMS320F2812 DSP.

In the test case, a Thyristor based rectifier as nonlinear load and a voltage source with sag depth of 0.2 p.u. are considered. The parameters of test system are given in Table 7. Fig. 11 shows the source voltage, injected voltage and load voltage inabovementioned conditions. It can be seen from this figure that the load side voltage is not been affected by utility side voltage sag. This confirms the proper operation of series converter in proposed UPQC and its control system.

Table 7: Characteristics of test system

<table>
<thead>
<tr>
<th>Utility side disturbance</th>
<th>time</th>
<th>Injected voltage</th>
<th>Source Phase Voltage</th>
<th>DC-link voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sag</td>
<td>0.1 s</td>
<td>30v</td>
<td>150v (peak)/50Hz</td>
<td>500v</td>
</tr>
</tbody>
</table>
To show the proper operation of shunt converter of proposed UPQC and its control system, the load currents, injected currents by shunt converter and utility side currents of same test case are presented in Figs 12 (a)-(c), respectively. It can be seen from these figures that after compensation the utility side currents are nearly sinusoidal while the load currents are non-sinusoidal. These results confirm proper operation of shunt converter in proposed topology for UPQC and its control system.
7. CONCLUSION

In this paper design, simulation and implementation of unified power quality conditioner (UPQC) based on back-to-back B4 converter is presented applying synchronous reference frame theory. The number of switches in the proposed topology for UPQC is decreased in comparison with previously proposed topologies. The PIV of the switches in the proposed topology is greater in comparison with topology based on conventional back-to-back converter but lower than the PIV of the switches in the nine-switch converter. Also the proposed topology as four and one less switches in comparison with

The measured DC-link voltage is presented in Fig. 12(d). This figure shows that the DC-link voltage regulator has properly regulated the DC-link voltage at its reference value.

Fig. 12: (a) Load current (b) Injected current (c) Source current (d) DC-link voltage during voltage sag
above mentioned topologies, respectively. The proposed UPQC topology can lead to a decrease in whole system cost, power losses and an increase in efficiency and reliability of the system because of less number of circuit elements. Simulation results show the ability of proposed UPQC topology in the voltage distortion, reactive power and harmonic current compensation. The PI controller stabilizes DC-link voltage by balancing the power between series and shunt inverters. Experimental results confirm the results achieved from simulation by MATLAB/SIMULINK.

CONFLICT OF INTERESTS

The authors declared that there is no conflict of interests.

REFERENCES