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Low Power-High Gain Bulk-Driven 3 Stages CMOS Miller OTA in 130nm Technology

Engin AFACAN*[1]

Abstract

The requirement of low-power analog circuits has been raised in recent years due to the strict limitation of power consumption in modern applications. Therefore, the trend in analog circuit design has been changed such that they are able to meet the required specifications with lower power dissipation. Design of low power operational transconductance amplifiers, which are the main building blocks in many analog applications, has been more pronounced to keep the power dissipation below certain levels. In this concern, this study presents a low power, high-performing bulk-driven 3 stages CMOS OTA in a 130 nm standard CMOS technology. The proposed circuit leverages the bulk-driven architecture at the input stage; thus it can operate under sub 1-V. The design process of the proposed OTA is explained in detail and the results are validated via post-layout simulations. The proposed OTA is powered by ±0.45 V symmetric voltage sources, where the power consumption is around 27 µW. The area overhead is only 0.0017 µm2. The open-loop gain, unity gain frequency, and the phase margin are 73.24 dB, 5.167 MHz, and 78º, respectively. To demonstrate the performance of the proposed circuit, a comparison is made with other circuits published in the last five years considering the well-known figures of merit (FOMs). Comparison results indicate that the proposed solution outperforms the other circuits for small-signal operation while it is the runner-up for large-signal operation.

Keywords: Analog, CMOS, bulk-driven, low power, OTA, 130nm.

1 INTRODUCTION

Operational amplifiers are one of the most important building blocks in analog integrated circuit design, which has a wide range of applications (e.g., ADCs, DACs, and filters). Over the years, numerous different topologies (two stage, folded, telescopic, etc.) have been developed to design high performing operational amplifiers and the effort is still ongoing since the requirements of the modern electronics have been changed.

Nowadays, a large portion of the consumer electronics consists of portable devices (e.g., PDAs and smart phones), so the power consumption has been strictly limited for those devices to increase working durations without charge plug-in. Therefore, low power design has become a major concern in recent years for IC industry [1-7].

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Considering the analog design problem consisting of difficult trade-offs among specifications, designing low power circuits while keeping the performance of the circuits at certain levels is not trivial, even it is highly challenging. To demonstrate the analog circuit design essentials and trade-offs among several circuit specifications, an illustration is provided in Fig. 1.

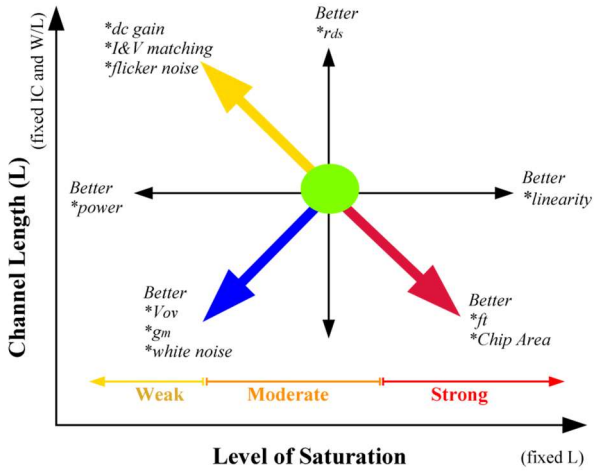

Figure 1 An illustration of saturation level vs. channel length guidance for analog circuit design [8,9]

As seen from the figure, both the channel length and the saturation level of the transistor are the major parameters to achieve the targeted design specifications for a given analog design problem (e.g., keeping the length minimum while pushing transistor into strong inversion provides higher bandwidth). Considering the low power analog circuit design, one possible solution is to design transistors such that they operate in weak inversion (sub-threshold) region. Since the bias current of transistors in the weak inversion is commonly a few nano-amperes, the power consumption can be reduced. However, the intrinsic unity-gain bandwidth of transistors decreases as the transistors come close to weak inversion region.

Therefore, weak-inversion based analog circuit design may not be a proper solution for low-power applications that also need high speed. Sub-threshold based designs addresses ultrasonic, biomedical, and wireless sensor interface applications [5, 10-15]. The obstacle with design of low power analog circuits is relatively high threshold voltages, which is the result of scaling difference between the power supply and the threshold voltage (V_t). Intentionally, V_t has not been aggressively scaled to meet the noise performance of integrated circuits.

Employing low V_t transistors is another way to mitigate the power consumption; however, one should consider the noise problem and the increased cost bringing with the low V_t technology. Besides, the bulk-driven transistor approach is a quite efficient way to surpass the effect of threshold voltage, where the bulk terminal is used as the input of the circuit [16-23]. This modification enhances the low voltage operation capability of transistors and allows to low power high performing analog circuits. The idea behind the bulk-driven approach is to bias the gate properly and apply the signal to the bulk terminal in order to control the saturation current by $g_{mb}V_{bs}$. Therefore, there is no V_t barrier at the input, which enhances the dynamic input range and enables low-voltage operation [17]. A major problem of the bulk-driven transistors is that they have considerably lower transconductance (g_{mb}) compared to a typical connection (input applied to the gate terminal). In this paper, a low-power and high performing bulk-driven three-stage CMOS OTA is presented. To decrease the chip area and increase the DC gain, the circuit architecture presented in [5] has been adopted. The proposed circuit is explained in detail and validated through post-layout simulations.

The Remainder of the paper is as follows. The proposed solutions is described and analyzed in Sections 2 and 3, respectively. Experimental results are presented in Sections 4. Section 5 provides a comparison with other published solutions in the last five years is provided. Finally, the paper is concluded in Section 6.

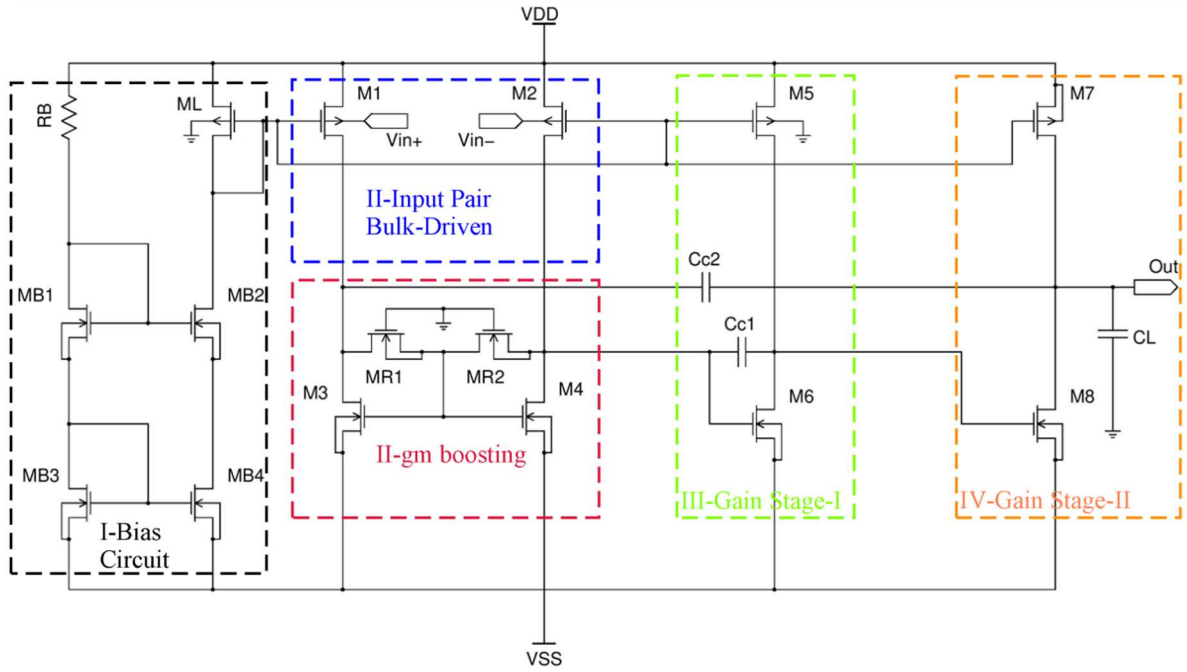

Figure 2 Schematic of the improved bulk-driven 3 stages operational transconductance amplifier

2. DESCRIPTION OF THE PROPOSED CIRCUIT

The circuit schematic of the proposed 3 stages Miller OTA circuit is given in Fig. 2. The proposed amplifier has been adopted from the circuit presented in [5], where a biasing circuit (cascode current mirror) has been replaced rather than a constant current source, the resistors in the gain boosting part have been replaced by MOSFETs acting as resistors, and two transistors at the output stage have been removed. The details for the applied modifications will be explained in the following section.

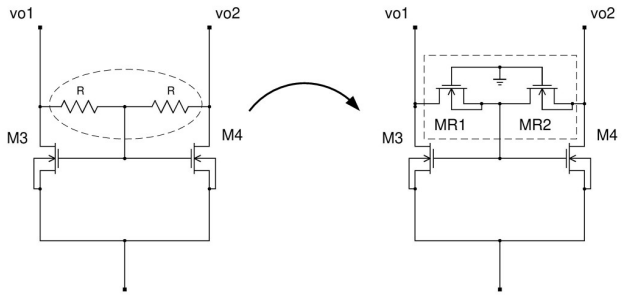

Figure 3 Modification of the effective g_m boosting stage. MR1 and MR2 operate in linear regime and act as resistors

As seen from the circuit schematic, the proposed circuit is comprised of four stages: Biasing, input differential pair, effective gm boosting stage, the first gain stage, and the second gain stage (output stage). A cascode current mirror is employed to generate the bias current, where MB1-MB4 and RB are the components of the biasing circuit. The saturation currents of M1-M2 and M3-M4 transistors are determined via ML. As the input stage, M1-M2 transistors are used in the bulk-driven configuration, whose gate terminals connected to ML transistor's gate for biasing aim.

The circuit proposed in [5] includes a load part (g_m boosting) consisting of M3-M4 and two resistors. The resistor values are selected relatively large in order to boost the small bulk transconductance (g_{mb}). However, using large resistors may degrade the noise performance and increase the area overhead. To palliate those problems, the resistors have been replaced by the transistors MR1-MR2 operating in linear regime. Considering the requirement of large resistance at this part, the dimensions of those transistors are critical, where longer and narrower transistors should be preferred. Here, the DC

currents through MR1-MR2 are negligible. M3-M4 transistors can be assumed as diode connected and act as current mirror with M6. Similarly, the DC current of M8 is also determined through M3-M4 since they also act as current mirror. Therefore, the saturation currents of M6 and M8 can be determined by (1).

$$I_{d6} = \frac{I_{d3,4}\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_{3,4}} \ , I_{d8} = \frac{I_{d3,4}\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_{3,4}}. \quad (1)$$

As the first gain stage, M5-M6 transistors are employed in common-source configuration, where the size of M5 is determined considering the I_{d6} given in (1). The capacitor Cc1 is included for frequency compensation for this stage. At the last gain stage, again, an active loaded common-source configuration is used though M7-M8 transistors. The capacitor Cc2 is used in a feedback network for the purpose of pole splitting; thus, enhancing the frequency response. To determine the minimum supply voltage, the rail-rail voltage drop between VDD and VSS should be equal to at least,

$$VDD - VSS = V_{GS3} + V_{DS1}. \quad (2)$$

In [5], additional NMOS and PMOS transistors in cascade configuration are included to the end of the second stage for the purpose of properly biasing of M7; thus, canceling the systematic offset errors. However, careful sizing of transistors satisfies the same function; therefore, those transistors have been removed in the proposed circuit.

3. ANALYSIS FOR MAJOR DESIGN CONSIDERATIONS

Analog circuit design (sizing) is not a trivial problem such that it cannot be solved through blind sizing iterations. Therefore, the idea behind circuit sizing should be supported with theoretical calculations, which substantially reduce the search space and the duration to achieve targeted specifications. In this section, the circuit is explained in detail by giving fundamental equations.

3.1. Bias Current Determination

The first stage is an NMOS type cascade current mirror. Assuming all transistors are identical, for the sake of simplicity, the transistor sizing ratios can be selected as follows.

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4}. \quad (3)$$

The resulting output current can be calculated as;

$$I_o = \frac{I_{ref}\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}, \quad (4)$$

where I_o is the output current (bias current for differential pair) and I_{ref} is the current flow through the resistor RB. Once a reference current is constituted, the bias current is easily determined by using those simple equations.

3.2. Voltage Gain and Common-Mode Rejection Ratio (CMRR)

The proposed circuit includes 3 gain stages. In the first stage, a bulk driven circuit and a gain boosting circuit (Figure 3) are assigned. This type of active load stage enables also fully differential operation for pair M1−M2 [5]. Considering a gate-driven amplifier, the gain is typically expressed as $g_m r_o$, where r_o is the resistance seen from the output node and commonly equals to $r_{ds}/2$. However, the proposed circuit includes a bulk-driven pair at the input, which yields an output voltage as given in (5) when an input of v_i is applied.

$$v_{o1,2} = v_{gs3,4} \pm \frac{1}{2} v_i R g_{mb1,2}. \quad (5)$$

In (5), R denotes the equivalent resistance generated by the MOSFETs in linear regime and $v_{gs3,4}$=v_{gs} denotes the gate to source voltages of M3-M4. Since the currents flow in the same branch will be equal to each other, it can be drawn that $g_{mb1}(v_i/2) = g_{m3}v_{gs}$ and $g_{mb2}(v_i/2) = g_{m4}v_{gs}$. By using these equalities, (5) can be rewritten as follows.

$$v_{o1,2} = \pm \frac{v_i}{2}\left(\frac{g_{mb1,2}}{g_{m3,4}} + R g_{mb1,2}\right). \quad (6)$$

Since $g_m >> g_{mb,}$ the output voltage of the first stage can be calculated as;

$$v_{o1,2} = \pm \frac{v_i}{2}\left(R g_{mb1,2}\right). \quad (7)$$

As seen from (7), the R value should be kept as large as possible to amplify even very small signals. Considering a MOSFET operating in linear regime, the resistance value can be calculated as follows.

$$R = L/W \mu_n c_{ox}(V_{GS} - V_t). \quad (8)$$

(8) shows that those transistors should be designed as narrower and longer as possible compared to the other transistors in order to achieve high resistance values. Moreover, one should also consider that the output resistance seen from the differential pair is actually R//r_{ds3}//r_{ds4}. After the first stage, the data signal is transmitted through two similar common-source amplifiers and the output voltage can be expressed as follows.

$$v_{out} = \frac{v_i}{2}\left(R g_{mb1,2}\right) g_{m6}(r_{out2}) g_{m8}(r_{out3}). \quad (9)$$

Once a bias current is determined (keeping small for low power), the transconductance values can be calculated; thus, a rough gain calculation can be performed.

CMRR exhibits performance of amplifier in terms of suppressing the common-mode voltage at the input. Considering the circuit schematic (g_m boosting part), resistors (MR1-MR2) sets the common mode gain through M3-M4. Namely, there is no current flow through MR1-MR2; thus, the gate and the drain voltages of M3-M4 are equal to each other. Let us apply a common voltage (v_{cm}) to the inputs of differential pair. A current of $g_{mb1,2}v_{cm}$ flows through transistors. This current is also equal to the current ($g_{m3,4}v_{gs}$) flows through M3-M4, where v_{gs} is equal to $v_{o1,2}$. The common-mode gain can be expressed as

$$A_{cm} = \left|\frac{v_o}{v_{cm}}\right| = \frac{g_{mb1}}{g_{m3}}. \quad (10)$$

As a result, the CMRR can be calculated as follows.

$$CMRR_{single\_ended} = \left|\frac{A_o}{A_{cm}}\right| = \frac{1}{2}(R)\, g_{m3}. \quad (11)$$

According to (11), the resistor values (MR1-MR2) should be kept as large as possible to maximize the CMRR.

3.3. Frequency Response

The unity-gain bandwidth of a conventional Miller OTA circuit with compensation is simply approximated as

$$W_{GBW} \cong \frac{g_m}{C_c}, \quad (12)$$

where g_m is the transconductance of the input transistors and C_c is the compensation capacitor. Even though the frequency response is quite straightforward to be handled, the stability is highly problematic for multi-stage amplifiers, so further theoretical analysis is needed for pre-design phase.

A general form of transfer function of a system including multi-poles and zero can be expressed as

$$A_s \cong A_0 \frac{1 + \frac{s}{z}}{\left(1 + \frac{s}{p}\right)(as^2 + bs + 1)}. \quad (13)$$

Considering the compensation capacitors C_{c1} and C_{c2} and the current buffer through M3-M4 pair,

the dominant pole (p) and the zero (z) are calculated as

$$p = \frac{2}{g_{m6} g_{m8} R r_{out2} r_{out3} C_{c1}} \quad (14a)$$

$$z = \frac{g_{m3} g_{m6}}{2C_{c1} g_{m6} - C_{c2} g_{m3}}. \quad (14b)$$

Considering (13), a and b denote the coefficients for non-dominant complex conjugate poles and given as

$$a = \frac{C_{c2}C_L(2g_{m6} + g_{m3})}{g_{m3}g_{m6}g_{m8}} \quad (16a)$$

$$b = \frac{C_L(C_{c1} + g_{m6}C_{c2}r_{out2})}{C_{c1}g_{m6}g_{m8}r_{out2}}. \quad (16b)$$

To ensure the stability of the amplifier, the damping factor can be calculated similar to the expression given in [5] as follows;

$$\xi = \frac{b}{2\sqrt{a}} = \frac{C_{c1} + C_{c2}g_{m6}r_{out2}}{2C_{c1}r_{out2}} \quad (17)$$

$$x\sqrt{\frac{C_L g_{m3}}{g_{m6}g_{m8}C_{c2}(2g_{m6} + g_{m3})}}$$

The first design step is to determine the targeted bandwidth and calculation of required g_{mb} and C_{c1} from (12). Then, a suitable C_{c2} can be approximated from (17) to keep the damping ratio below certain level. Another suggestion is adjusting $g_{m6}/ g_{m3} >> C_{c2}/ C_{c1}$ to avoid any negative zero [5].

4. EXPERIMENTAL RESULTS

The proposed circuit given in Fig. 2 was implemented in a 130nm standard CMOS technology. Mentor Graphics® and HSPICE® were used for design and simulation steps, respectively. Design parameters for the proposed circuit are listed in Table-1. The design parameters including transistors aspect ratios and other parameters were determined considering the design insight (major design equations) explained in Section 3. The power supply of the circuit was determined as ±0.45 V, where the circuit drives a load of 25 pF. The targeted unity-gain frequency was 5 MHz. To achieve this bandwidth, the bias current for the transistors M1-M2 was calculated as 5 µA. Then, the transistor widths were determined for the first level. Dimensions of the transistors MR1-MR2 were selected in order to achieve a considerable gain at the first stage. As previously mentioned, longer and narrower transistors were preferred in order to achieve high output resistance. The value of compensation capacitors were determined to obtain a sufficient phase margin. Some pre-layout measurements were summarized in Table 2. The total power consumption of the circuit is around 25.7 µW. The layout is provided in Fig. 4. The total area occupation of the circuit is $1.1\text{x}10^{-3}$ mm^2.

Table 1
Design parameters for proposed circuit for ±0.45V power supply and 25 pF load capacitor

L [µm]	Rbias [Ω]	WB1,2,3,4 [µm]	WR,1,2 [µm]	W3,4 [µm]	W5 [µm]	W6,8 [µm]	W7 [µm]	WR1,2 [µm]	LR1,2 [µm]	Cc1 [fF]	Cc2 [fF]
0.5	40k	12	12	2	30	5	20	0.18	10	250	10

Table 2
Pre-layout DC measurement results of some electrical parameters for the proposed circuit

I_{M1-M2} [µA]	$g_{mb1,2}$ [µA/V]	$g_{m3,4}$ [µA/V]	g_{m6} [µA/V]	g_{m8} [µA/V]	$r_{ds3,4}$ [MegΩ]	I_{DD} [µA]	I_{SS} [µA]
5.18	12.3	100	255	58	0.45	25.7	25.7

The presented layout does not include the compensation capacitors since the values are comparable with the layout parasitic capacitances. Therefore, they are externally included to the post-layout netlist. Even they were included, the area occupation would be at worst 1.7 x10^{-3}mm^2.

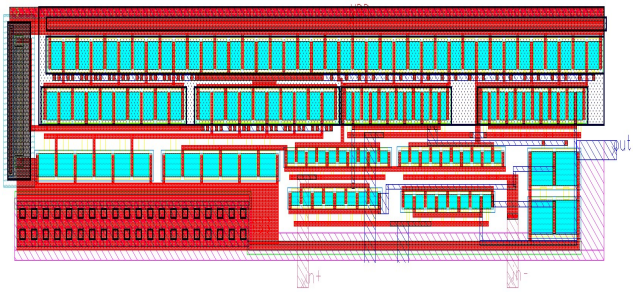

Figure 4 Layout of the proposed circuit

4.1. Frequency Domain Analysis Results

The post-layout bode plot of the proposed amplifier is provided in Fig. 5. According to the simulation results, the amplifier has 73.24 dB gain, where the gain margin is around 11dB. The unity-gain frequency was measured as 5.17 MHz. The phase margin of the amplifier is around 78^o. CMRR and power supply rejection ratio (PSRR) were also measured for the circuit. The post-layout simulation result for CMRR is given in Fig. 6. According to the results, the amplifier has a CMRR of 97.7 dB. The reason of achieving such high value is using transistors in linear regime yielding high resistance values. The PSRR of the circuit was measured as 70 dB. These values are very competitive compared to the results reported in the literature.

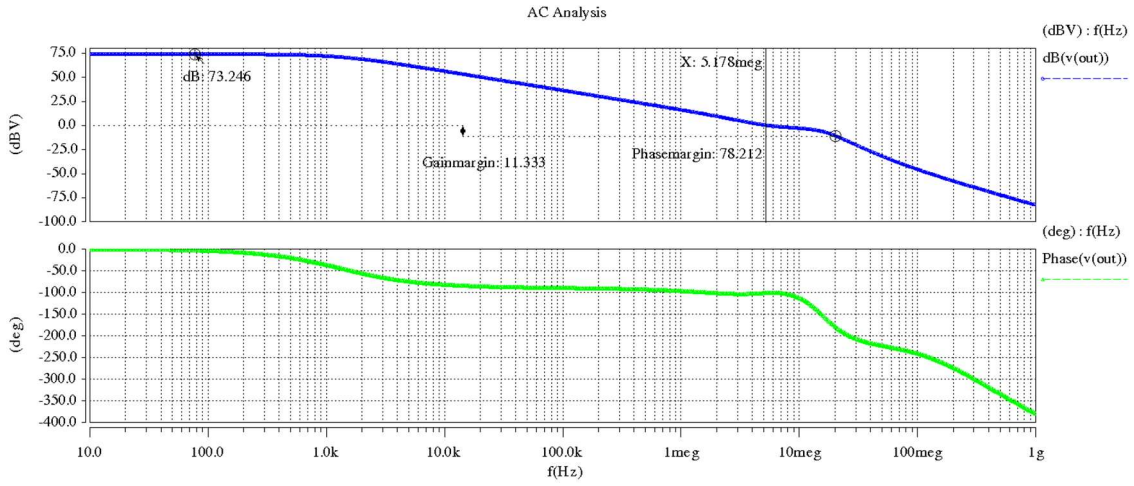

Figure 5 Post-layout bode-plot of the proposed amplifer

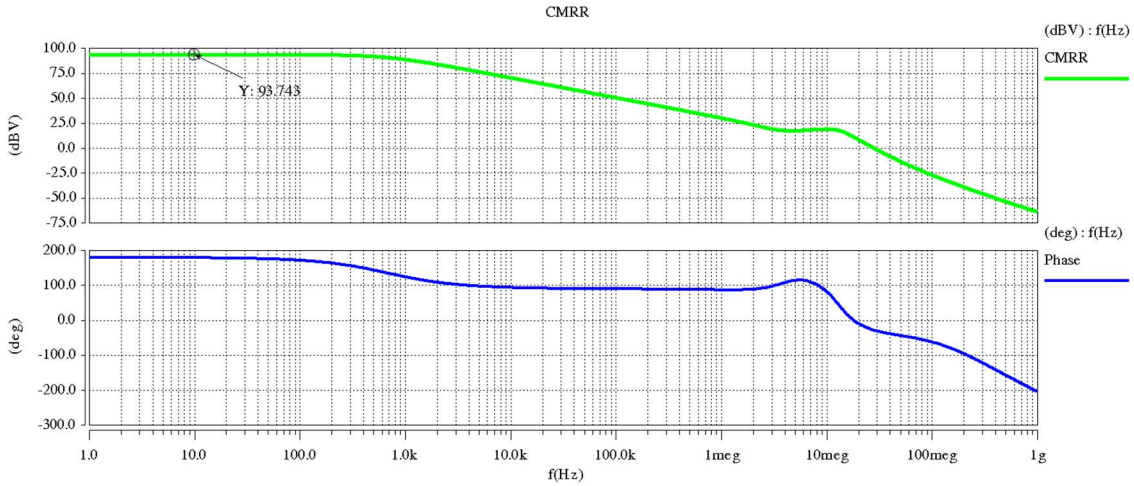

Figure 6 Post-layout simulation results for CMRR

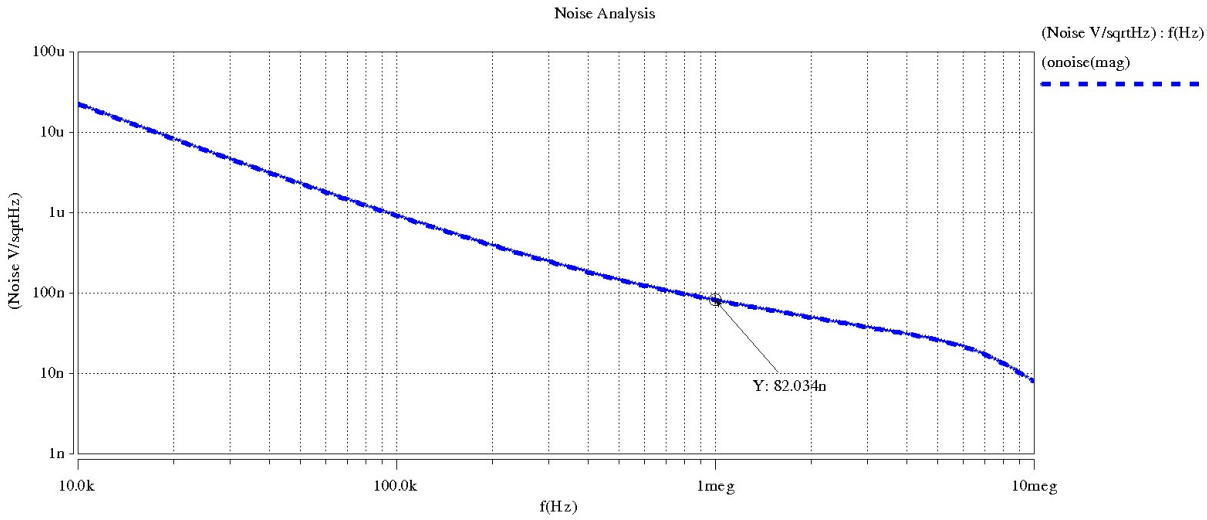

Figure 7 Post-layout simulation results for noise analysis of the proposed amplifier

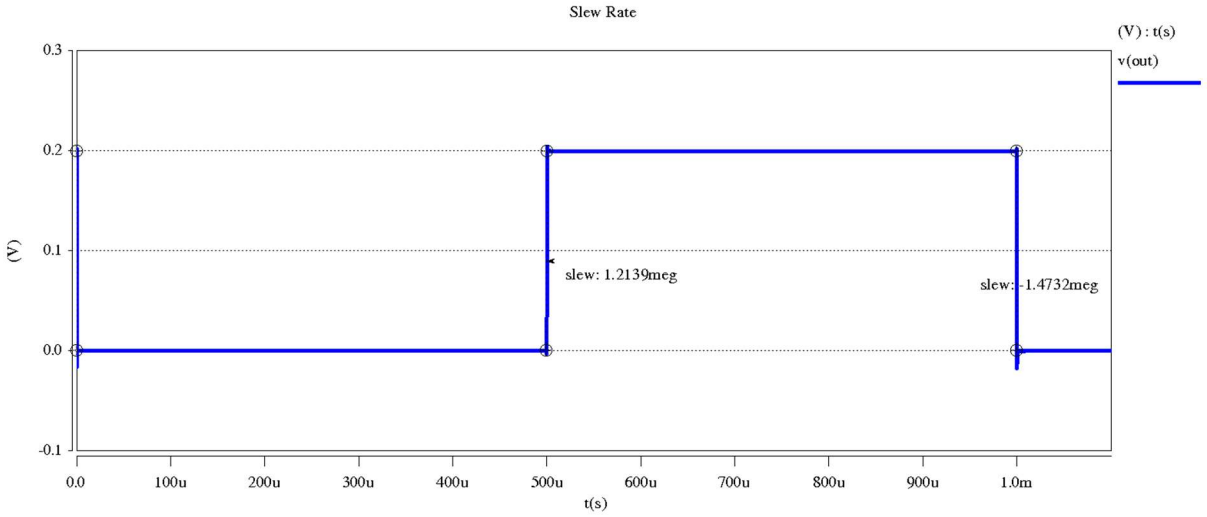

Figure 8 Slew-rate measurement result for 200 mVpp step input applied in unity-gain configuration

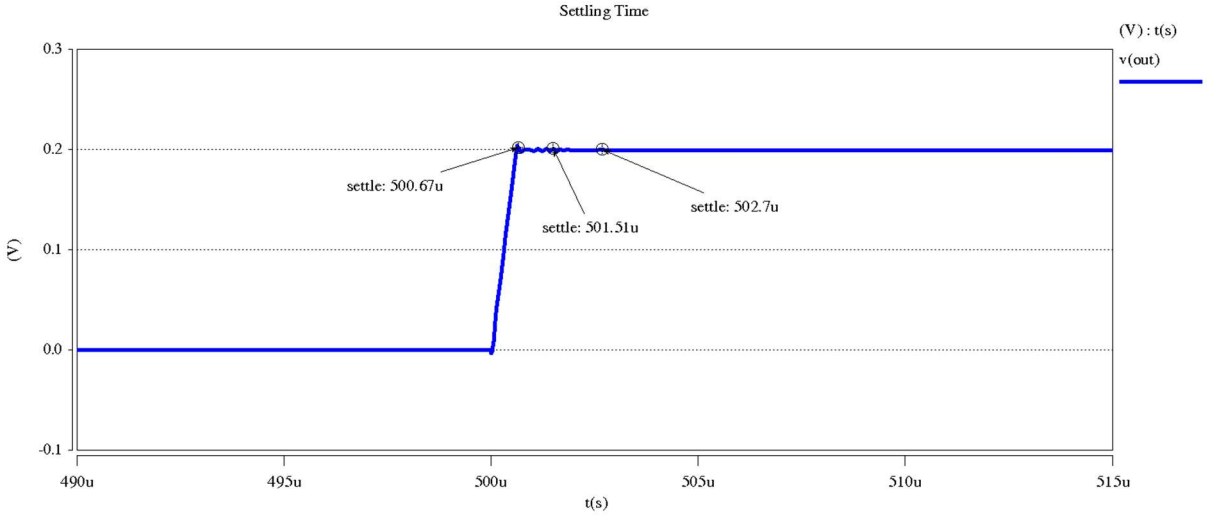

Figure 9 Settling-time measurement result for 200 mVpp step input applied in unity-gain configuration

Noise measurement result is shown in Fig. 7.The input referred noise density measured at 1 MHz is around 82 nV/$\sqrt{Hz}$.

4.2.Time Domain Analysis Results

To demonstrate the transient performance of the circuit, a 200 mV_{pp} input step was applied in the unity gain configuration. The post-layout simulation result for the slew-rate is provided in Fig. 8. The positive and negative slew rate values were measured as 1.21 V/µs and 1.47 V/µs, respectively. Moreover, the settling time was also measured using the same input configuration. According to the results provided in Fig. 9, the settling time for achieving 5%, 1%, and 0.1% maximum amplitude are 0.67 µs, 1.51 µs, and 2.7 µs, respectively. The total current drawn from power supplies is 30µA. The total power consumption of the circuit was measured as 27 µW. The output and input offset voltages were also measured, where the circuit has 68 mV output offset voltage whereas the input offset was measured as 32 µV.

4.3. Variability Analysis: Process-Voltage-Temperature (PVT) Analysis

To verify the design against variation effects, PVT analysis was performed. To observe the process variations, Monte Carlo analysis was perfumed with 5000 samples. The histogram plots for the gain and the unity-gain bandwidth are provided in Fig. 10 and Fig. 11, respectively.

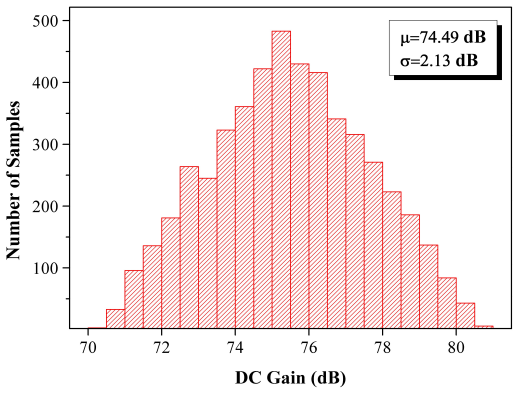

Figure 10 Monte Carlo analysis result for the gain

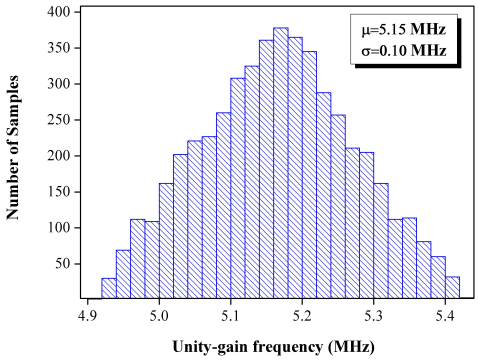

Figure 11 Monte Carlo analysis result for the unity gain-bandwidth

As seen from the results, the mean value of 5000 samples is around 5.15 MHz while the standard deviation is just 0.10 MHz. Similar results were obtained for the open loop gain, where the average gain value and the standard deviation are 74.5 dB and 2.13 dB, respectively. According to the results, the circuit can exhibit sufficient gain and bandwidth even the worst case occurs.

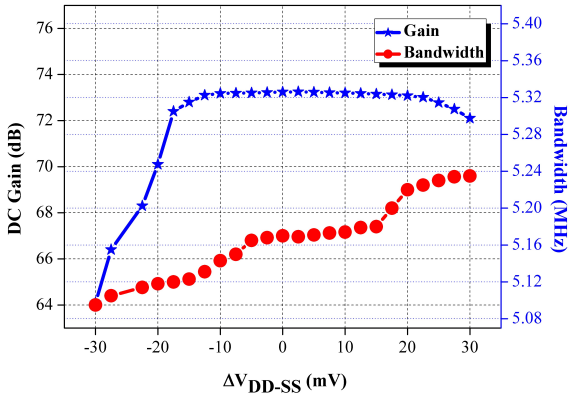

Figure 12 Monte Carlo analysis result for the gain. The sample size of the analysis is 5000

To consider the effect of variations in power supplies, the supply voltages were swept by up/down to ±30 mV and results are provided in Fig. 12. Simulation results indicate that the bandwidth of the circuit is not affected by the power supply variations. On the other hand, the open-loop-gain is quite different, where the gain decreases when a negative change in power supply occurs. For the positive variations, the gain is almost the same up to certain point, then, it also decreases.

At last, the temperature variation analysis was performed for the proposed circuit and the results are provided in Fig. 13. As seen from the results, the circuit performance degrades at low temperatures. The case for the high temperature is more dramatic, where a considerable performance loss occurs. Even though those degradations, the performance of the circuit is still sufficient to be used as an OTA.

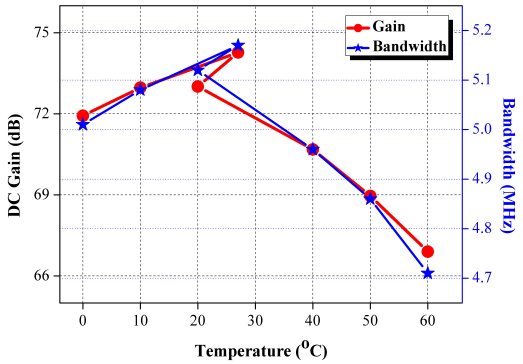

Figure 13 Effect of the temperature variations on the open-loop-gain and the unity gain frequency

4.4. Design Summary

A single-ended three stage OTA with low power consumption circuit was analyzed and designed in a 130 nm CMOS technology. Post-layout measurement results and the design details are summarized in Table 3.

Table 3
Summary of the design specifications of the proposed circuit

Specification	Value
Unity-gain frequency (MHz)	5.17
Open-loop-gain (dB)	73.24
Phase Margin (°)	78.21
Gain Margin (dB)	11.33
CMRR (dB)	93.74
PSRR (dB)	70
Input referred noise ($nV/\sqrt{Hz}$)	82
Slew Rate (V/µs) (Pos. - Neg.)	1,21-1.47
Settling Time (µs) (5% - 1% - 0.1%)	0.67 - 1.51 - 2.7
Input Offet Voltage (mV)	0.032
Output Offset Voltage (mV)	68
Power Consumption (µW)	27
Chip Area (mm^2)	6
Supply Voltage (V)	±0.45

Table 4
Benchmark comparison

Specification	This Work	2015 [24]		2016 [5]	2016 [19]	2017 [6]	2018 [25]	2019 [26]	2020 [27]
Technology (nm)	130	65		180	180	350	180	180	40
Supply Voltage (V)	±0.45	0.5	0.45	0.7	0.6	0.9	0.3	0.5	0.6
Load Capacitance (pF)	25	3		20	15	27	20	15	1
Open-loop-gain (dB)	73.24	46	43	57.5	82	65	65.8	111.5	60
Unity-gain bandwidth (MHz)	5.17	38	3.6	3	0.019	1	0.0028	0.0095	45
Phase Margin (°)	78.21	57	56	60	60	60	61.2	66	86.5
Slew Rate (V/µs)	1.34	0.043	5.6	2.8	0.012	0.25	0.0072	0.0009	18.2
Settling Time (µs) (1%)	1.51	N.A.		1.15	75	1.8	166	N.A	0.038
Power Consumption (µW)	27	182	17	25.4	0.4	21.2	0.015	0.07	30
Chip Area (μm^2)	1700	5000		19800	40000	14000	8200	19700	1632

5. DISCUSSION

To demonstrate the performance of the proposed circuit, a selection of sub-1V amplifiers published in the last five years has been explored and compared with the proposed circuit. The performance comparison table is provided in Table 4. According to the results, the proposed circuit has highly competitive specifications compared to the other circuits. Especially, the chip area, unity-gain bandwidth, phase margin, and capacitive loading capability of the proposed circuit are at the upper ranks. To generalize the comparison, the well-known two figures-of-merit given in (17) and (18) were considered. Typically, FOM_1 measures the AC performance of the circuit while FOM_2 measures the transient performance.

$$FOM_1 = \frac{UGF.C_L}{Area.Power} \quad (17)$$

$$FOM_2 = \frac{SR.C_L}{Area.Power} \quad (18)$$

UGF and SR denote unity-gain-frequency and slew rate, respectively.

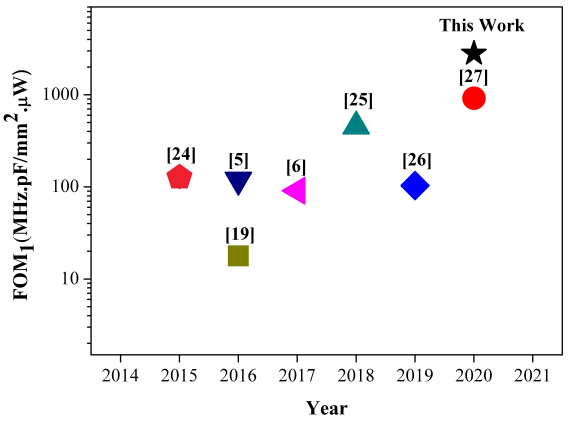

Figure 14 FOM_1 comparison results

FOM_1 and FOM_2 results of the all circuits are visually illustrated in Figures 14 and 15, respectively. Considering the FOM1 results, it is apparently seen that the proposed circuit outperforms the all other circuits, where the FOM_1 score of it is 2816 while the runner-up [27] has a FOM_1 of 920. Regarding the FOM_2 results, the proposed circuits exhibits quite good performance (the runner-up with 730 FOM_2 score) that is close to the best score (1170) achieved by [25].

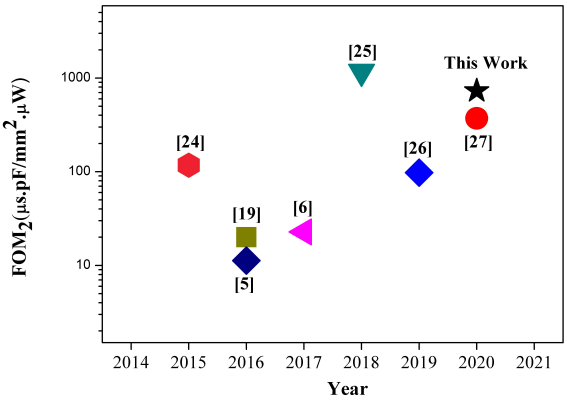

Figure 15 FOM_2 comparison results

6. CONCLUSION

In this paper, a modified bulk-driven 3 stages CMOS OTA in a 130 nm standard CMOS technology for low-power applications has been presented. Thanks to the bulk-driven configuration, the circuit can operate with sub 1-V power supply. The applied modification provides high gain and less area overhead. Post-layout simulation results indicate that the proposed circuit has 73.24 dB gain, 5.17 MHz bandwidth, and 78° phase margin, respectively. PVT analysis has been performed to verify the robustness of the circuit against process, voltage, and temperature variations. To compare the performance of the proposed circuit with the other circuits published in the last five years, the well-known figures of merit (FOMs) were calculated and demonstrated on a benchmark figure. Comparison results indicate that the proposed solution is highly competitive with the other circuits, whose ranks are 1st and 2nd for small-signal and large signal operations, respectively.

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No conflict of interest or common interest has been declared by the author.

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The author of the paper declare that he complies with the scientific, ethical and quotation rules of SAUJS in all processes of the paper and that he does not make any falsification on the data collected. In addition, he declares that Sakarya University Journal of Science and its editorial board have no responsibility for any ethical violations that may be encountered, and that this study has not been evaluated in any academic publication environment other than Sakarya University Journal of Science.

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