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Research Article

The Effect of Interlayer Thickness on Frequency Dependent Electrical Characteristics of Al/p-Si Schottky Barrier Diodes with $Bi_4Ti_3O_{12}$ Interlayer

Arayüzey Kalınlığının $Bi_4Ti_3O_{12}$ Arayüzeye Sahip Al/p-Si Schottky Engel Diyotların Frekansa Bağlı Elektriksel Özellikleri Üzerindeki Etkisi

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Abstract

Lead-free bismuth titanate ($Bi_4Ti_3O_{12}$, i.e. BiT) attracts attention of researchers due to its peculiar properties which make it a suitable material for various electronic device applications. Therefore, this study focuses on thickness dependent electrical characteristics of Schottky barrier diodes having BiT interlayer. Frequency dependent admittance measurements revealed electrical characteristics of the Schottky barrier diodes are affected by BiT interlayer thickness. An increase in capacitance and conductance is observed in a way that the intensity is higher at lower frequencies due to interface states. Also, peaks are observed in capacitance-voltage (C-V) and conductance-voltage (G/ω-V) plots and existence of these peaks was explained by the effects caused by series resistance and interface states. Series resistance was found to decrease with increasing BiT interlayer thickness whereas interface states increased. Moreover, main electrical parameters of Schottky barrier diodes; such as doping concentration of acceptor atoms, built-in voltage, image-force barrier lowering and barrier height, were extracted from C^{-2}-V plots and it was found that thickness of BiT interlayer alters these parameters.

Keywords: Admittance spectroscopy, Bismuth titanate, Electrical characteristics, Schottky barrier diode

Öz

Kurşun içermeyen bizmut titanat ($Bi_4Ti_3O_{12}$, yani BiT) kendisini çeşitli elektronik cihaz uygulamalarına uygun kılan özgün özellikleri nedeniyle araştırmacılarının ilgisini çekmektedir. Dolayısıyla, bu çalışma BiT arayüzeye sahip Schottky engel diyotlarının kalınlığa bağlı elektriksel özellikleri üzerine odaklanmıştır. Frekansa bağlı admitans ölçümleri Schottky engel diyotların elektriksel özelliklerinin BiT arayüzeyin kalınlığı tarafından etkilendiğini ortaya koymuştur. Düşük frekanslarda arayüzey durumlarından dolayı kapasite ve iletkenlik değerlerinde yüksek şiddette bir artış gözlenmiştir. Ayrıca, kapasite-gerilim (C-V) ve iletkenlik-gerilim (G/ω-V) eğrilerinde pikler gözlenmiş ve bu piklerin varlığı seri direnç ve arayüzey durumlarının neden olduğu etkilerle açıklanmıştır. BiT arayüzeyin kalınlığının artırılmasıyla birlikte arayüzey durumlarının arttığı, seri direncin ise azaldığı tespit edilmiştir. Dahası, Schottky engel diyotları için alıcı atomların katkılama yoğunluğu, difüzyon potansiyeli, görüntü kuvveti engel alçalması ve engel yüksekliği gibi temel elektriksel parametreler C^{-2}-V eğrilerinden elde edilmiş ve BiT arayüzeyin kalınlığının bu parametrelerde değişikliğe yol açtığı tespit edilmiştir.

Anahtar Kelimeler: Admitans spektroskopisi, Bizmut titanat, Elektriksel özellikler, Schottky engel diyotu

1. Introduction

Metal-semiconductor (MS) contacts (Schottky Contacts) has been on the focus of researchers for quite long time. Considerable modification in electrical characteristics of these devices became possible by growing a thin insulating layer between metal and semiconductor. Such insulating layer alters barrier height, leakage current, series resistance, interface states and device capacitance. Moreover, it helps passivation of dangling bonds, prevents interdiffusion between metal and semiconductor and alleviates electric field reduction (Gökçen et al. 2011, Çetinkaya et al. 2015).

For the last couple decade, researchers try various insulating materials both organic and inorganic in order to obtain optimized device characteristics (Başman et al. 2015, Tecimer et al. 2012, Altındal et al. 2014, Gökçen et al.

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2011, Çetinkaya et al. 2015). Reported studies confirms better passivation is achieved with materials having higher dielectric constant (Bengi et al. 2010, Jebalin et al. 2015, Usman et al. 2011). On the other hand, thickness of such insulating layer also plays an important role. For example, for a very thin insulating layer, interface states are in equilibrium with metal whereas, for a thicker insulating layer, they are in equilibrium with semiconductor (Card and Rhoderick 1971). Thickness also affects series resistance of the device and this in turn alters the current passing through the device. Also, it is likely to have larger number of structural defects with increasing volume due to larger thickness, therefore thickness of the insulating layer also modifies interface states. Since Schottky contacts with an insulating layer basically behaves like a capacitor whose plates are filled with dielectric material, thickness of insulating layer also affects the capacitance of the device. In this study, bismuth titanate (BiT) was chosen as insulating material due to several reasons such as high Curie temperature, large remnant polarization, low coercive field, low polarization fatigue, high breakdown strength (Durmuş et al. 2013, Jardiel et al. 2008, Kitanaka et al. 2010). BiT is a ferroelectric material which does not contain lead, therefore it is not harmful to environment. A metal-ferroelectric-semiconductor Schottky barrier diode (SBD) forms the gate section of several ferroelectric devices such as ferroelectric field effect transistor (FeFET) which is an important part of memory devices such as ferroelectric random access memory (FeRAM). Therefore, investigation of Schottky barrier diodes having ferroelectric interlayer is of interest from several aspects. For this reason, usage of BiT in SBDs is an attractive topic. In previous studies (Durmuş et al. 2013, Durmuş and Yıldırım 2014), current conduction and dielectric properties of Al/p-Si contacts having BiT interlayer were investigated. This study includes investigation of thickness dependent electrical characteristics in Al/BiT/p-Si SBDs through admittance spectroscopy. For this purpose, Al/BiT/p-Si SBDs were fabricated using BiT interlayer that has three different thickness values and their frequency dependent admittance measurements were held at room temperature.

2. Material and Methods

For the fabrication of SBDs, boron doped 3" p-type silicon wafer was used such that thickness and resistivity of the wafer are 280 μm and ~5 Ω.cm, respectively. Firstly, the wafer was cleaned following the same procedure of previous study (Durmuş and Yıldırım 2014). Later, back side of the wafer was deposited with pure Au (99.999%) layer with thickness of 200 nm in a thermal evaporation system. Then the sample was annealed in dry nitrogen ambient (1.5 l/min) at ~600 ^oC for 20 min. Thanks to annealing procedure, the deposited Au layer is sintered, thus low resistivity ohmic contact is achieved. The wafer was cut into four pieces. Following this step, samples were taken into a RF magnetron sputtering system in which the front side of the wafer is deposited with BiT interlayer using a hot compacting of $Bi_4Ti_3O_{12}$ powder of a stoichiometric composition as a target material. During the sputtering process, the samples were kept at 650 ^oC in the working medium of argon and oxygen mixture. Three different samples were prepared. Thickness of BiT interlayer for each sample was determined using a Veeco Dektak 6 M thickness profilemeter as 10 nm, 25 nm and 53 nm. These samples are referred as SBD1, SBD2 and SBD3, respectively, in the paper. Afterwards, pure Al (99.999%) front contacts (200 nm) in the form of circle were deposited on BiT interlayer using a shadow mask in the thermal evaporation system.

Once the fabrication process is completed, samples were prepared on a copper holder using silver paste and thin wires for electrical measurements in cryostat. Admittance data of the samples were measured between ±4 V using a HP4192A LF impedance analyzer. During the measurement, a small ac test signal (40 mV_{rms}) is applied in order to perform frequency dependent admittance measurements. Frequency of the test signal was between 10 kHz and 1 MHz. Admittance data was recorded on a computer through IEEE-488 AC/DC converter card. All measurements were held at room temperature.

3. Results and Discussion

Fig. 1 shows C-V and G/ω-V plots of the diodes at various frequencies. As seen in the figure, SBD1 and SBD2 exhibit typical SBD behavior of inversion, depletion and accumulation regions whereas such behavior for SBD3 is not clear due to thick interlayer. There are peaks in C-V plots of SBD1 and SBD2; such peak behavior appears due to density of interface states (N_{ss}) and series resistance (R_s) such that N_{ss} is dominant in depletion region whereas R_s is dominant in the high accumulation region (Altındal and Uslu 2011, Çetinkaya et al. 2015, Sharma and Tripathi 2016).

It is clearer in Fig. 1a that there exist two peaks for C-V plots; one around depletion region, the other is in high forward biases. As the interfacial layer is increased, the peaks in high forward biases disappear (Fig. 1c), therefore it can be said that

SBD with thicker BiT interlayer would yield lower R_s value. This is also supported by higher conductance values obtained for thicker BiT interlayer. On the other hand, the peaks around depletion region reveal a split between 10 kHz and 1 MHz plots such that split is larger for the SBD with thicker BiT interlayer. This suggests that higher N_{ss} values would be obtained for SBD3. When G/ω-V plots are considered, regions lose clarity as the interlayer thickness is increased, particularly G/ω-V plots of SBD3 seems saturated when all frequency levels are given in a single graph. However as can be seen in inset of Fig. 1c, conductance values of SBD3 is not indeed saturated through whole bias region. Having 53 nm BiT interlayer, SBD3 practically acts like a MOS structure with thick interlayer. Other effects of interlayer thickness are the increase in threshold voltage and larger bias voltage difference for C-V plots to reach accumulation (Fig. 1a, Fig. 1b).

Fig. 2 shows frequency dependence of capacitance and conductance in the SBDs at bias voltage of 4 V. It is seen that capacitance of all SBDs decrease with increasing frequency (Fig. 2a). At lower frequencies, interface states can follow the a.c. signal due to lower life-time of interface states, and this results in excess capacitance, therefore higher capacitance values are obtained at lower frequencies. Higher capacitance values for larger BiT interlayer tends to be smaller towards 1 MHz. This shows that main difference at lower frequencies is due to excess capacitance which is basically observed due

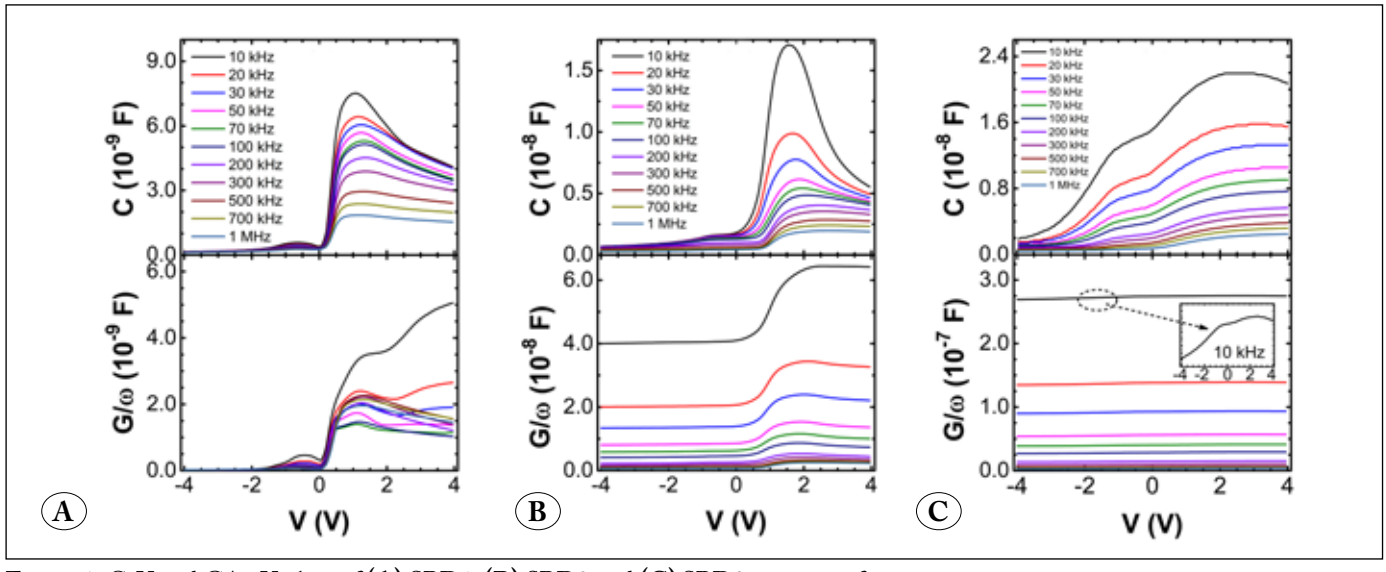

Figure 1. C-V and G/ω-V plots of **(A)** SBD1, **(B)** SBD2 and **(C)** SBD3 at various frequencies.

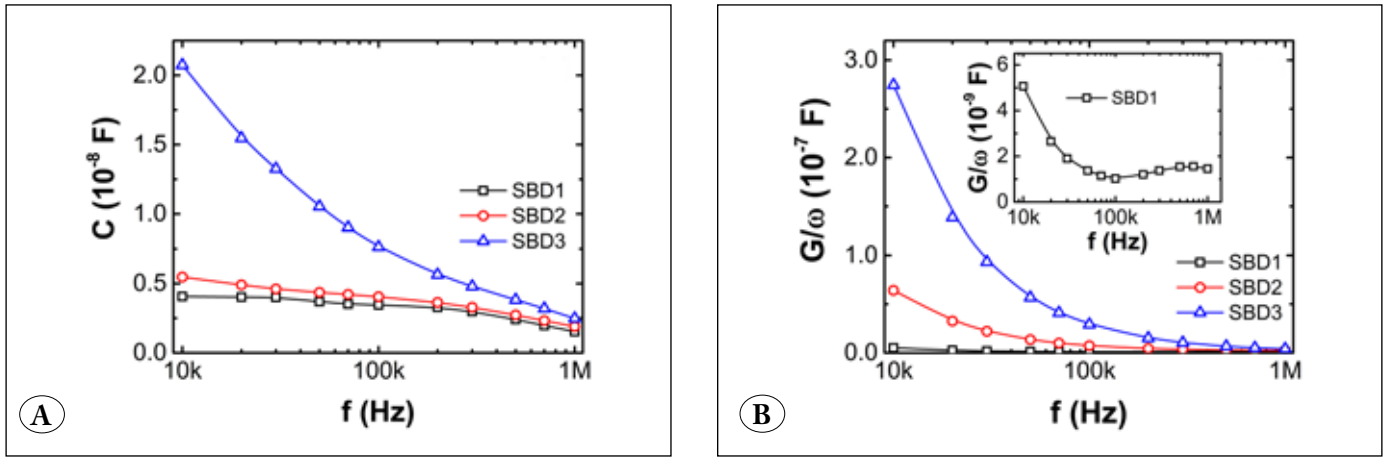

Figure 2. Semilogarithmic **(A)** C-f and **(B)** G/ω-f plots of SBD1, SBD2 and SBD3 at 4 V. Inset shows semilogarithmic G/ω-f plot of SBD1 at 4 V.

to interface states. Therefore, this also shows that higher N_{ss} values are to be expected for the SBD with thicker interlayer. Similar to capacitance, conductance values also decrease with increasing frequency (Fig. 2b). However, as can be seen in inset of Fig. 2b, there is slight deviation for SBD1 after 100 kHz, it increases after 100 kHz and exhibits peak behavior around 700 kHz. Considering imaginary part of dielectric constant is obtained by $G/\omega C_o$ where C_o is equivalent capacitance of free space, such peak behavior in G/ω–f plot can be associated with relaxation mechanism in the structure. Thus, it can be said that relaxation mechanism in the studied SBDs can be tuned by changing thickness of BiT interlayer regarding SBD2 and SBD3 do not reveal such peak in G/ω–f plots.

As mentioned above, R_s is an important device parameter that affects the device characteristics in several ways. R_s values of the SBDs are calculated using the approach of Nicollian and Brews (Nicollian and Brews 1982) that real part of impedance in the strong accumulation region reveals R_s of the device as in following equation;

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}$$

Here C_{ma} and G_{ma} stand for capacitance and conductance measured in the accumulation region. Fig. 3 shows semilogarithmic R_s-f plots of the SBDs. As seen in the figure, R_s decreases with increasing frequency. As mentioned before, trapped charges cannot follow a.c. signal at high frequencies (practically above 500 kHz), therefore these charges can be swept by the bias voltage at high frequencies and thus lower R_s values are obtained as the frequency is increased. The general trend in R_s with changing BiT interlayer is that it is lowered for thicker interlayer such that R_s values of SBD1, SBD2 and SBD3 at 1 MHz is 52 Ω, 41 Ω and 29 Ω, respectively. This is believed to be the result of particular energy distribution of the surface states in a way that there exist shallow surface states for SBD3 which are close to valance band so that trap charges have sufficient energy to escape from traps towards valance band and yield lower R_s.

Similar to series resistance, interface states also cause small-signal energy loss. N_{ss} values of the diodes were calculated using high-low frequency method which is based on the idea that excess capacitance at lower frequencies are caused by the charges trapped at interface states. According to this method, N_{ss} is given by the following equation (Castagne and Vapaille 1971);

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right]$$

where q is electronic charge, A is area of rectifier contact and C_{ox} is the oxide capacitance ($=\varepsilon_i\varepsilon_o A/d$) with ε_o is permittivity of vacuum, and ε_i and d are dielectric constant of interfacial layer and thickness of BiT interlayer, respectively. Thus, N_{ss} values of the diodes are calculated using Eq. 2 and their bias voltage evolution is given in Fig. 4. As seen in the figure, N_{ss} plots yield a peak in forward bias region since excess capacitance occurs particularly in this region. It is clear that larger number is obtained as the BiT interlayer is increased as expected previously from capacitance data.

$$C^{-2} = \frac{2}{q\varepsilon_s A^2 N_A}\left[V + \left(V_{bi} - \frac{kT}{q}\right)\right]$$

Capacitance data is also used in order to extract electrical parameters of SBDs. In the depletion region, the relationship of capacitance with applied bias voltage is given by following (Sze and Ng 2006);

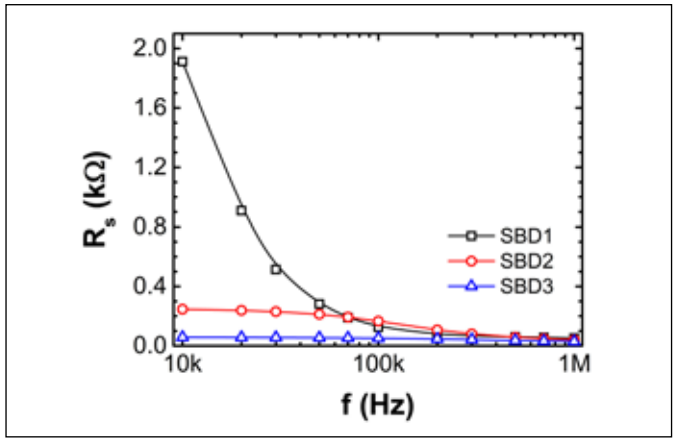

Figure 3. Semilogarithmic R_s-f plots of SBD1, SBD2 and SBD3 at 4 V.

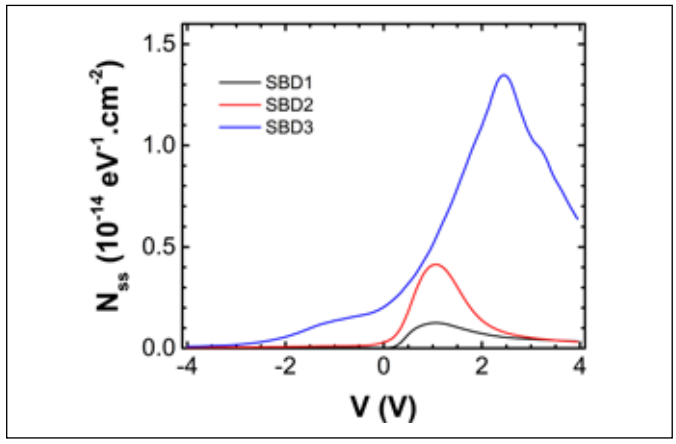

Figure 4. N_{ss}-V plots of SBD1, SBD2 and SBD3.

Table 1. Main electrical parameters of SBD1, SBD2 and SBD3 at 1 MHz

Diode	N_A (cm^{-3})	V_{bi} (eV)	E_F (eV)	W_d (cm)	$\Delta\Phi_b$ (eV)	Φ_b (ev)
MFS1	$8.22x10^{14}$	0.382	0.242	$3.21x10^{-4}$	0.011	0.613
MFS2	$4.01x10^{15}$	0.657	0.201	$1.90x10^{-4}$	0.019	0.839
MFS3	$7.60x10^{15}$	0.850	0.185	$1.59x10^{-4}$	0.023	1.012

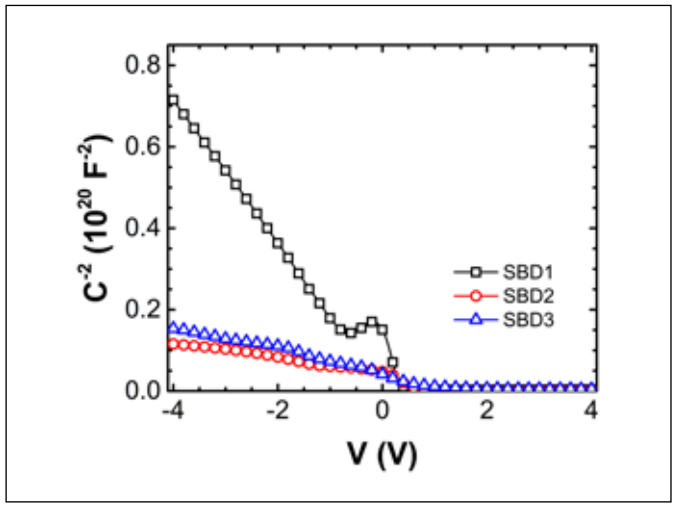

Figure 5. C^{-2}-V plots of SBD1, SBD2 and SBD3 at 1 MHz.

where ε_s is dielectric constant of semiconductor, N_A is the concentration of acceptor atoms and V_{bi} is built-in potential which is also referred as surface potential. According to this equation, C^{-2}–V plots of the diodes are supposed to reveal linearity in depletion region. Thus N_A and V_{bi} are extracted from the slope and intercept of C^{-2}–V plots given in Fig. 5. Once these parameters are obtained, one could also calculate Fermi energy (E_F), width of depletion layer (W_d), image-force barrier lowering ($\Delta\Phi_b$) and barrier height (Φ_b) of the SBDs. Details of extraction of these electrical parameters are available elsewhere (Durmuş et al. 2013). Table 1 shows electrical parameters of the diodes extracted from depletion region of C^{-2}–V plots at 1 MHz. Increasing BiT interlayer thickness leads to an increase in N_A, V_{bi}, $\Delta\Phi_b$ and Φ_b of the diode whereas E_F and W_d are lowered. This result indicates electrical parameters of Al/BiT/p-Si can be tuned through changing the thickness of BiT interlayer.

4. Conclusion

Admittance measurements of the fabricated SBDs revealed that SBDs tends to have larger capacitance and conductance values with increasing BiT interlayer thickness. This behavior becomes prominent particularly at lower frequencies due to the fact that interface states can follow a.c. signal at lower frequencies. Peak behavior in C-V plots were ascribed to series resistance and interface states. When these plots are considered, it was also seen that increasing thickness yields larger threshold voltage. Lower series resistance values were obtained with increasing BiT interlayer due to particular distribution of surface states. Moreover, interface states density also depended on the BiT interlayer thickness; larger values were obtained with increasing thickness due to larger excess capacitance at lower frequencies. Thickness also affected several other electrical parameters. Built-in potential, image-force barrier lowering and barrier height of the SBD increased with thicker BiT interlayer. Obtained results show that thickness of BiT interlayer alters the SBD's electrical characteristics, thus required device characteristics can be achieved by altering the BiT interlayer thickness.

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