

Voltage Dependent Barrier Height, Ideality Factor and Surface States in Au/(NiS-PVP)/n-Si (MPS) type Schottky Barrier Diodes

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ABSTRACT: Metal-Polymer-Semiconductor (MPS) Schottky Barrier Diodes (SBD) were manufactured and their basic electrical parameters were obtained by the measurement of the forward and reverse bias current-voltage ($I-V$) in the wide bias voltage range ($\pm 3V$) to determine the voltage dependent effects on Nickel-Sulphur (NiS) doped Poly Vinyl Pyrrolidone (PVP) polymer interlayer. The saturation current (I_0), zero-bias barrier height (Φ_{B0}), rectifying rate (RR), ideality factor (n) and the real value of series - shunt resistances ($R_s - R_{sh}$) were calculated. The voltage dependent profile of $n(V)$, $\Phi_B(V)$, and $R_s(V)$ were derived. The forward bias $\ln I-V$ plot of the MPS type SBD indicates a good rectifier behaviour and it has two distinctive linear parts with different slopes which correspond to low ($0.288 \leq V \leq 0.625 V$) and moderate ($0.672 \leq V \leq 0.960 V$) bias voltages and then deviates from linearity due to R_s and interlayer at high forward bias voltages. Energy dependent profile of N_{ss} was obtained from the forward bias $I-V$ data by considering voltage dependent barrier height (Φ_B) and n . N_{ss} plot represents U-shape behaviour in the forbidden bandgap. The mean value of N_{ss} was found at about $7.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ and this value is in the acceptable limit for a semiconductor device and such lower values of N_{ss} are the consequences of the passivation effect on the surface states.

Keywords: MPS type SBD, Voltage dependent barrier height, Series resistance, Surface states, Double exponential $I-V$ behavior

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INTRODUCTION

The electrical and optical behaviours of metal-semiconductor (MS) junction with or without an interlayer such as insulator/oxide, polymer or its composites (MIS/MOS and MPS) depend on various factors; such as, the surface preparation or manufacture processes, the formation of interlayer which is native or deposited, its permittivity and homogeneity, the nature of barrier height, surface states, series resistance, bias voltage, device temperature and donor (N_D) or acceptor atoms' (N_A) doping concentration (Card and Rhoderick, 1971; Sze, 1981; Cheung and Cheung, 1986; Bohlin, 1986; Rhoderick and Williams, 1988; Tung, 2001; Tung, 2001; Tataroglu, 2013). The formation of an oxide or insulating interlayer such as SiO_2 or SnO_2 between metal and semiconductor by traditional methods is insufficient to reduce the leakage currents in the reverse bias region and formation of N_{ss} with dislocations between interlayer and semiconductor with energies in the forbidden bandgap of the semiconductor. Therefore, some polymers undoped or doped with, for example Ni, Zn, Co, graphene, have begun to be used instead of oxide materials due to their low cost, easy production techniques, flexibility and low weight per molecule (Demirezen et al., 2013; Guçlu et al., 2016; Akhlaghi et al., 2018; Badali et al., 2018; Altindal Yeriskin, 2019).

Both poly-vinyl-pyrrolidone (PVP) and poly-vinylalcohol (PVA) are semi-crystalline, water-soluble and have low conductivity, wide range crystallinity, high dielectric strength, good charge storage capacity, interesting physical and chemical properties which arise from OH groups and formation of hydrogen bonding (Lee et al. 2004). When polymers compared with semiconductors, they have low carrier mobility and dielectric constant, but this problem can be overcome by using a suitable dopant metal/graphene (Kaya et al. 2016; Altindal Yerişkin et al. 2017). For example, Altindal Yerişkin et al. 2017 have investigated the effects of (Gr-doped PVA) interfacial layer on Au/n-Si (MS) type structure by using various concentrations of graphene (% 0, 1, 3, 5, 7, 10) and they showed that Au/(0.07 Gr-PVA)/n-Si (MPS) has lower R_s and N_{ss} , higher R_{sh} and RR with considerable increase of dielectric constant compared to a traditional MS structure with an insulator/oxide (MIS or MOS). They showed that the value of RR of MPS structure is about 500 times higher and N_{ss} is about 95 times lower than the MS structure. Kaya et al. 2016 also showed that the value of ϵ' for (GO-doped PrBaCoO) the nano-ceramic at 1 kHz is almost 200 times higher than the conventional SiO_2 and 15 times higher than TiO_2 .

Organic/polymer materials have also large surface area to volume ratio, energy/charge storage capacity with much mechanical and dielectrical strength. Moreover, they are soluble in water and easily grown on the surface of a semiconductor. Thus, some polymer materials such as polyvinyl alcohol (PVA) and PVP can be grown as an interfacial layer between metal and semiconductor. These attractive properties lead to this study and MPS type SBDs were manufactured; then, with forward and reverse bias I - V measurements in the wide bias voltage range ($\pm 3V$), the electrical parameters were derived to determine the effect of (NiS doped PVP) polymer interlayer with voltage dependent characteristics of these electrical parameters. By using the forward bias I - V data with Φ_B (V) and n , the N_{ss} dependence on the energy levels was evaluated.

MATERIALS AND METHODS

The MPS type SBDs were grown on n-type (phosphorus-doped) Si wafer with 300 μm thick and 1 Ω cm resistivity. First, it was cleaned in H_2O , H_2O_2 , and NH_4OH (3:1:1) solution at 70 $^\circ\text{C}$ in the ultrasonic bath and then rinsed in the ionized water at prolonged time and then rinsed in deionized water with high resistivity for 10 min and dried by dry nitrogen gas (N_2) to clean any oxidation. Second, ohmic contact with high-purity Au (99.999%) with 1500 \AA thick was thermally evaporated on the back side of

the Si wafer at 10^{-6} Torr and then it was annealed at $500\text{ }^{\circ}\text{C}$ in the nitrogenic atmosphere for 5 min to get a low resistivity ohmic contact. 0.2 M from nickel chloride $6\text{H}_2\text{O}(\text{NiCl}_2, \text{KBR})$ was dissolved in 40 ml distilled water and was stirred for 30 min, then 0.5 M $\text{Na}_2\text{S}\cdot 3\text{H}_2\text{O}$ (LOBA Chemie) was added to the solution drop by drop, until the pH of the solution is 7.0. Then, by adding 0.5 M NaOH (Merck), the reserved pH is 14. Next, the sample is kept 15 min in Power=180 microwave device (SAMSUNG). The sample was washed 5 times with water and was dried in oven for 48 h. Then, it was annealed at $1000\text{ }^{\circ}\text{C}$. The prepared (NiS-PVP) composite was grown on the front side of the wafer by spin coating method. The thickness of (NiS-PVP) polymer interfacial layer was estimated to be 40 nm. Circular shaped Au Schottky dot contacts with $7.85 \times 10^{-3}\text{ cm}^2$ area and 1500 \AA thick were formed on the polymer layer at 10^{-6} Torr. *I-V* measurements were performed by the use of Keithley 2400 current/voltage source-meter in wide range of bias voltage ($\pm 3\text{V}$) at room temperature.

RESULTS AND DISCUSSION

The semilogarithmic forward and reverse bias *I-V* graph of the Au/(NiS-PVP)/n-Si (MPS) type SBD is given in Figure 1 to determine the effect of the (NiS-PVP) polymer layer at room temperature. In this figure, semilogarithmic *I-V* plot of the MPS type SBD represents a satisfactory rectifier behaviour, i.e. while the value of the current in the reverse bias region becomes almost independent of reverse bias voltage, it has two different linear parts in the forward bias region with different slopes which correspond to low ($0.288 \leq V \leq 0.625\text{V}$) and moderate ($0.672 \leq V \leq 0.960\text{V}$) bias regions. By the effects of R_s and interfacial polymer layer, the linearity of the *I-V* curve deviates in the high voltage region. This type of *I-V* relation with two different linear parts in the forward bias region is explained with “two parallel diode model” in literature and the current mechanism in the MIS and MS type diodes is defined by utilizing the thermionic emission (TE) theory ($V \geq 3kT/q$ where k is Boltzmann constant, T is temperature and q is electric charge) (Bohlin, 1986).

As shown in Figure 1, due to the two linear regions the “two-parallel diode model” can be recalled and the double exponential current equation with different barrier heights (BH) and resistances is written as follows (Demirezen et al., 2013; Guclu et al., 2016):

$$I = I_{01} \left[\exp\left(\frac{q(V-IR_s)}{n_1 kT}\right) - 1 \right] + I_{02} \left[\exp\left(\frac{q(V-IR_s)}{n_2 kT}\right) - 1 \right] + \frac{(V-IR_s)}{R_{sh}} \quad (1)$$

Here I_{01} and I_{02} are the reverse saturation currents, n_1 and n_2 are the ideality factors for the low and moderate voltages and last term is the leakage current at very low voltages ($\leq 3kT/q$). Φ_{B_0} and $n(V)$ can be calculated for the two linear parts of $\ln I-V$ graph by the use of the following relations (Card, Rhoderick, 1971; Sze, 1981):

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{B_0}}{kT}\right) \quad (2a)$$

$$\Phi_{B_0} = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right) \quad (2b)$$

$$n(V) = \frac{q}{kT} \left(\frac{dV}{d(\ln I)} \right) = 1 + \frac{\delta}{\varepsilon_i} \left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V) \right] \quad (3)$$

In Equation (2a), (2b) and (3), A is $7.85 \times 10^{-3} \text{ cm}^2$, A^* is the Richardson constant ($112 \text{ Acm}^{-2}\text{K}^{-2}$ for n-Si). Thus, the main electrical parameters (I_0 , n , Φ_{B_0}) of SBD were calculated as $1.20 \times 10^{-8} \text{ A}$, 7.23, and 0.683 eV for low bias region and $3.20 \times 10^{-9} \text{ A}$, 4.23 and 0.732 eV for moderate bias region, respectively. The ideal value of n which indicates conformity to TE theory and values higher than the ideal value for the two linear region of $\ln I-V$ plot indicate deviation from TE theory. Such higher values of n are ascribed by the existence of (NiS-PVP) polymer interlayer, N_{ss} and inhomogeneities of the barrier between semiconductor and metal (Guttler and Werner, 1990; Schmitsdorf et al., 1995; Hudait et al., 2001; Orak and Kocyigit, 2016; Alptekin and Altindal, 2019). The high value of n usually stems from the existence of interfacial layer, its thickness (d_i), homogeneity and permittivity (ϵ_i), barrier inhomogeneity at M/S interface, N_{ss} , and doping concentration atoms in semiconductor or depletion layer width (W_d) as given in Equation (3). The tunneling through the barrier via surface states or dislocations, recombination-generation, and image-force lowering also affect the ideality factor and the conduction mechanism (CM) (Card and Rhoderick, 1971; Sze, 1981).

Both the forward and the reverse bias semi-logarithmic $I-V$ plots for both the Au/n-Si (MS) and Au/(NiS-PVP)/n-Si/Au devices were drawn and given in Figure 1 to see the effects of (NiS-PVP) polymer interlayer on the $I-V$ characteristics. As can be seen in Figure 1, RR at $\pm 3\text{V}$ for the MPS structure is almost 10 times higher than the MS structure. In addition, while the forward bias semi-logarithmic $I-V$ plot has only one linear region for MS structure, this plot for MPS structure has two distinctive linear regions with different slopes. In other words, such two linear behaviours for MPS structure are called as double exponential model or two-parallel diodes model with different R_s and Φ_{B_0} . As it is also seen in Figure 1, (NiS-PVP) interfacial polymer layer leads to a decrease in reverse current at about 10 times when compared with the MS structure. All these results show that the used (NiS-PVP) polymer interlayer leads to improve the performance of MS and hence, can successfully be used instead of conventional SiO_2 interlayer due to its low cost, easy preparation processes, flexibility and high dielectric/mechanical strength.

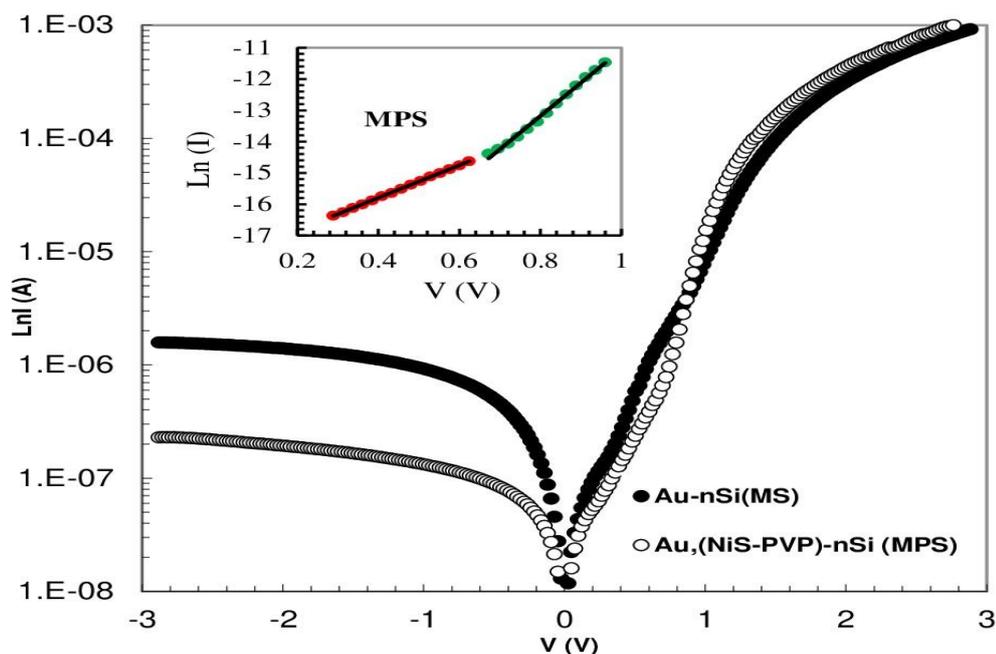


Figure 1. The $\ln I-V$ plot of the Au/n-Si (MS) and Au/(NiS-PVP)/n-Si (MPS) SBDs at room temperature. Inset shows the linear fits of the low and moderate voltage region

R_s and R_{sh} are more effective on the electrical characteristics, so they can cause serious errors in the calculations. The existence of R_s leads to serious error in the extraction of basic electrical parameters and conduction mechanisms of the MS structure with and without an interfacial layer. Usually, R_s can arise from four different sources: (i) the contact made by the probe wire to the rectifier contact; (ii) the back ohmic contact to the semiconductor; (iii) the resistance of the bulk semiconductor; (iv) inhomogeneous doping concentration of donor or acceptor atoms in the semiconductor (Nicollian and Brews, 1982). Therefore, the resistance of the diode structure (R_i) with respect to varying voltage is plotted with respect to Ohm's Law ($R_i = dV_i/dI_i$) and is given in Figure 2. The value of R_i proceeds constant both in the enough high forward and reverse bias region, shown in Figure 2. Therefore, the real value of R_s and R_{sh} for the MPS type SBD correspond to high forward and high reverse bias regions and they are found as $0.6 \text{ k}\Omega$ and $13 \text{ M}\Omega$ for ($\pm 3\text{V}$), respectively. RR of the diode is calculated at about 10^4 , which is a satisfactory rectifier property. All these obtained experimental electrical parameters from the I - V characteristics (I_0 , n , Φ_{B_0} , R_s and R_{sh}) are also tabulated in Table 1.

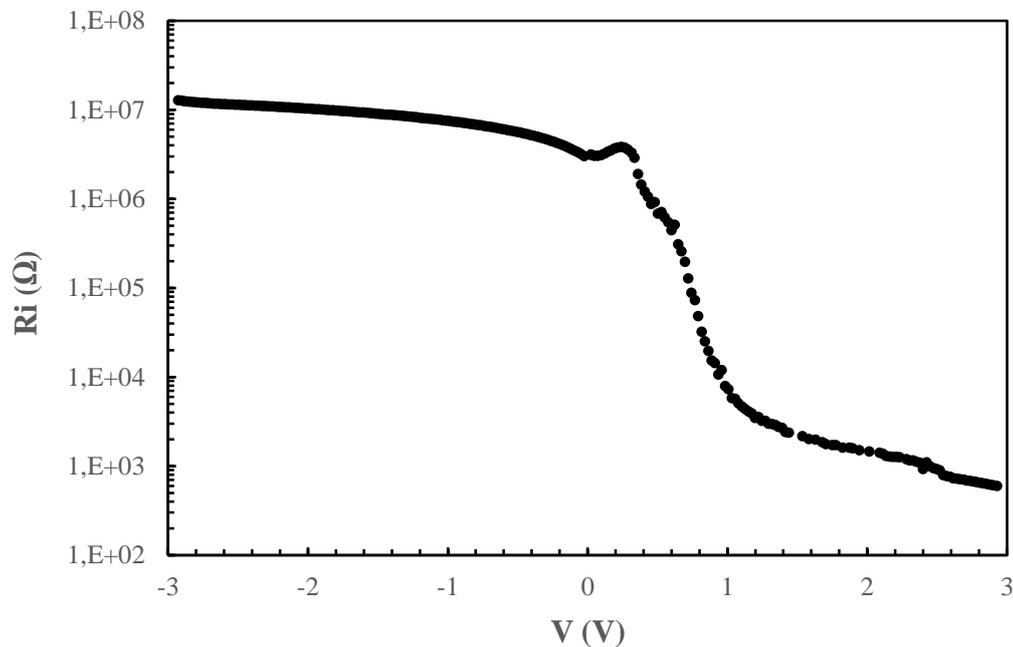


Figure 2. The R_i - V plot of the Au/(NiS-PVP)/n-Si (MPS) SBD at room temperature.

Table 1. The obtained some main experimental electrical parameters of the Au/(NiS-PVP)/n-Si (MPS) SBD from the I - V data at room temperature.

Voltage Region	I_0 (A)	n	Φ_{B_0} (eV)	R_s (at 3V) (kΩ)	R_{sh} (at -3V) (MΩ)	Mean value of N_{ss} (eV ⁻¹ cm ⁻²)
Low	1.20×10^{-8}	7.23	0.683	0.60	13.0	7.0×10^{12}
Moderate	3.20×10^{-9}	4.23	0.732			

In addition, values of the basic electrical parameters (R_s , n and Φ_B) of the diode can be obtained from the Cheung functions as another way by using the equations (Cheung and Cheung, 1986):

$$\frac{dV}{d(\ln I)} = IR_s + \left(\frac{nkT}{q}\right) \quad (4a)$$

$$H(I) = V - \frac{nkT}{q} \ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_{B_0} \quad (4b)$$

The $dV/d\ln(I)$ and $H(I)$ versus current plots were calculated from Equation (4a) and (4b), respectively, and represented in Figure 3. As can be clearly seen in Figure 3 (a) and (b), both the $dV/d\ln(I)$ vs I and $H(I)$ vs I plots have a good linear representation in the enough high forward bias voltage which corresponds to concave curvature of the $\ln I$ vs V plot. Firstly, the value of R_s is found from the slope of $dV/d\ln(I)$ vs I and $H(I)$ vs I plots in the same current range as 1.063 k Ω and 0.989 k Ω , respectively and these values are closer to the values obtained from Ohm's Law at room temperature. The value of ideality factor is found as 10.92 from the intercept of $dV/d\ln(I)$ vs I plot using Equation (4a). Thus, by using this value of n , Φ_B is found 0.64 eV from the intercept of $H(I)$ vs I graph by using Equation (4b). The observed discrepancies in the calculated basic electrical parameters (R_s , n , Φ_B) are attributed to the calculation method that corresponds to different voltage range (Bohlin, 1986; Cheung and Cheung, 1986; Tataroglu, 2013).

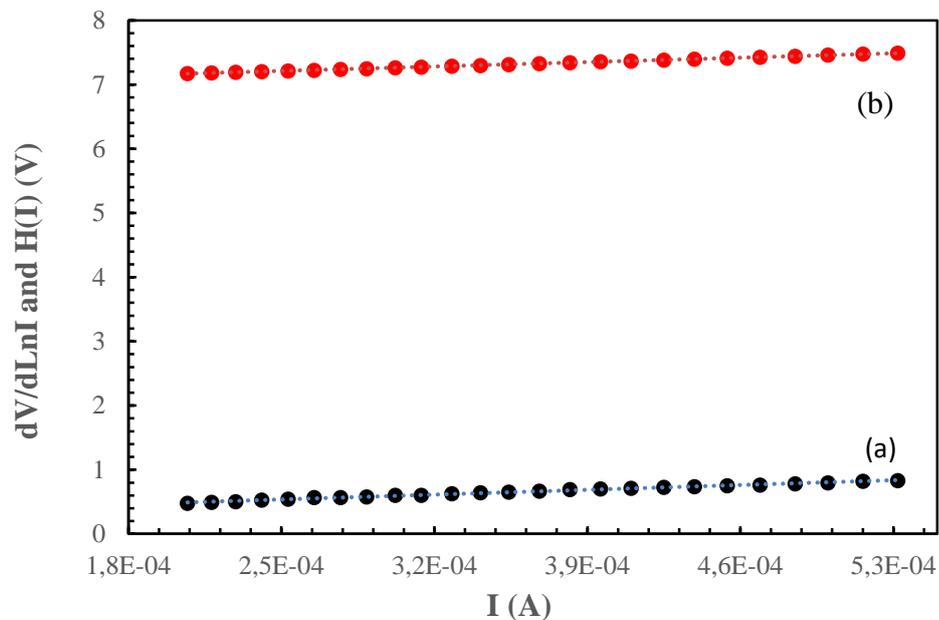


Figure 3. The $dV/d\ln I$ (a) and $H(I)$ (b) vs I plots for Au/(NiS-PVP)/n-Si (MPS) SBD at room temperature

The effect of voltage on the basic electrical parameters of SBDs is very important to detect the working capacity of the device. Therefore, the value of Φ_B (V) is also obtained as a function of forward bias I - V data except Φ_{B_0} and is given in Figure 4. As can be seen in Figure 4, the value of the BH decreases with increasing applied bias voltage and it is changed from 0.714 eV at 0.1V to 0.450 eV at 3 V, due to the effect of image force-lowering, R_s of the SBD and interfacial polymer layer. The effect of R_s and interfacial layer is considerably so high that the applied bias voltage is degraded by the depletion layer.

Many surface states and dislocations may be occurred with energies located in the forbidden bandgap of semiconductor (E_g) at layer/semiconductor interface, even though the diodes are fabricated in clean condition and they can considerably affect the performance of the devices. These states or traps are usually originated from defects such as dangling bonds in the interlayer/semiconductor interface with

energy states in the band gap (E_g), unsaturated dangling bonds, some contaminating organic impurities in the laboratory environment and the chemical composition of the interface.

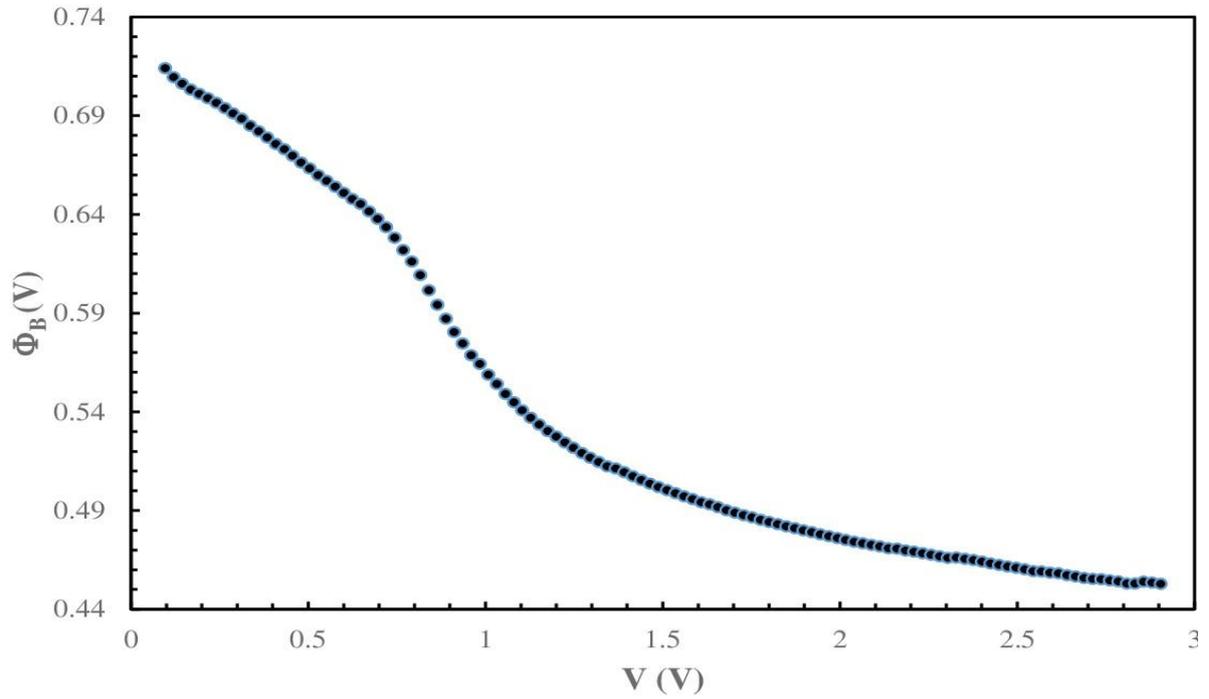


Figure 4. The voltage dependent barrier height of the Au/(NiS-PVP)/n-Si (MPS) SBD at room temperature

The energies of these states are usually in equilibrium with the semiconductor band structure rather than the metal when the interfacial layer thickness is higher than at about ~ 3 nm (Card and Rhoderick, 1971). These states are effective on the electrical parameters; thus, N_{ss} vs ($E_c - E_{ss}$) profile is obtained by the use of Φ_B (V) and n at room temperature and is given in Figure 5 by using the following relations (Card and Rhoderick, 1971; Sze, 1981; Rhoderick and Williams, 1988; Tung, 2001; Tataroglu, 2013), where E_c and E_{ss} are the energies of the conduction band and the surface states, respectively:

$$n(V) = \frac{qV_d}{kT \ln(I/I_0)} \quad (5a)$$

$$E_c - E_{ss} = q(\Phi_e - V_i) \quad (5b)$$

$$\Phi_e - \Phi_{B_0} = \left(1 - \frac{1}{n(V)}\right) V \quad (5c)$$

$$N_{ss} = \frac{\epsilon_0}{q} \left\{ \frac{\epsilon_i}{d} [n(V) - 1] - \frac{\epsilon_s}{W_D} \right\} \quad (6)$$

In Equation (6), d is the interfacial polymer layer thickness, W_D is the depletion layer width, ϵ_i , ϵ_s and ϵ_0 are dielectric values of the polymer interlayer, the semiconductor and the vacuum, respectively.

In Figure 5, the energy dependent profile of N_{ss} behaves like U-shape and the indicates that N_{ss} starts to increase from the center of the bandgap of Si to the bottom of the conduction band. The mean value of N_{ss} is found as $7.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ and they are considerably acceptable for the MPS type

structure. As a result, it can be said that the used (NiS-PVP) polymer interface between Au and n-Si wafer leads to an increase in the performance of MS. The investigation of interfacial layer effects on the electrical and performance of the MS structures were also investigated in very recently and they also obtained similar results (Orak and Kocyigit, 2016; Ulsan et al., 2019; Tataroglu et al., 2020; Eroglu et al., 2020).

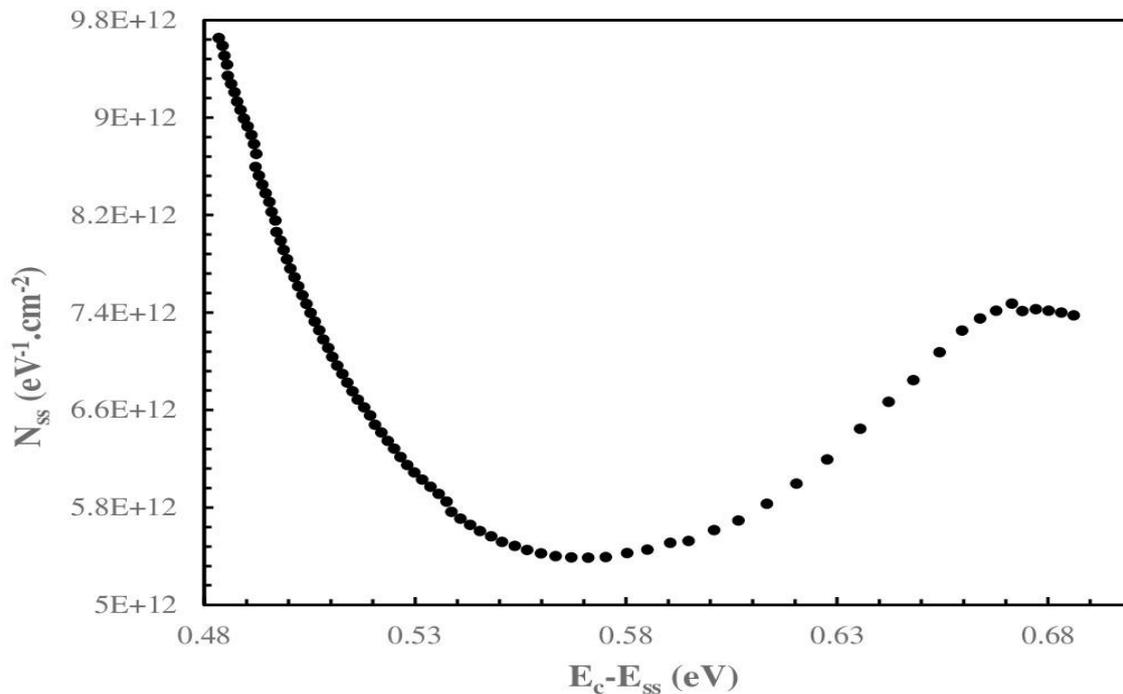


Figure 5. The energy dependent profile of N_{ss} for Au/(NiS-PVP)/n-Si (MPS) SBD at room temperature

CONCLUSION

Au/n-Si (NiS doped-PVP) SBD with polymer interlayer grown by electrospinning technique is used to determine the effects of interfacial layer and bias voltage on the electrical characteristics. Main electrical parameters (I_0 , Φ_{B_0} , RR , n , R_s and R_{sh}) are obtained at room temperature by using forward and reverse bias I - V characteristics in the voltage range of ($\pm 3V$). The forward bias $\ln I$ - V plot of the MPS type SBD represents a good rectifier behaviour and it has two linear regimes with different slopes between ($0.288 \leq V \leq 0.625$ V) and ($0.672 \leq V \leq 0.960V$) bias voltages. But it deviates from linearity because of R_s and interfacial polymer layer at enough high bias voltages ($V \geq 1$ V). N_{ss} vs ($E_c - E_{ss}$) profile is obtained by the use of Φ_B and n . The mean value of N_{ss} is calculated as 7×10^{12} eV $^{-1}$ cm $^{-2}$. Moreover, such lower values of N_{ss} can be attributed to the passivation effect on the surface states. The obtained experimental results indicate that R_s and N_{ss} , interfacial layer and bias voltage are very effective on the electrical behaviour of the device, which must be taken into consideration in the calculations to get more precise and reliable results on electrical features and conduction mechanisms.

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Conflict of Interest

I declare that there is no conflict of interest during the planning, execution and writing of the article.

Author's Contributions

I hereby declare that the planning, execution and writing of the article was done by me as the sole author of the article.

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