Interleaved High Step-up DC-DC Converter with Diode-Capacitor Multiplier Cell and Ripple-Free Input Current

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Received: 25.04.2015 Accepted:12.06.2015

Abstract- In this paper interleaving and switched-capacitor techniques are used to introduce a high step-up DC-DC converter for renewable energy systems application. The proposed converter delivers high voltage gain without utilizing transformer or excessive duty cycle and features ripple-free input current which results in lower conduction losses and decreased electromagnetic interference (EMI). Lower output capacitance is another advantage of proposed converter, leading to smaller size and lower cost. Furthermore lower voltage stress on switches allows the utilization of switches with low resistance. Simulation results verify the performance of suggested converter.

Keywords ripple-free input current; high step-up; switched-capacitor; interleaved technique; low switch voltage stress.

1. Introduction

The wide spread usage of fossil fuels in recent decades has caused resource reduction and a dramatic increase in environmental pollution. As a result, application of clean and free energy sources such as photovoltaic (PV) and fuel cell (FC) has become one of the hot topics among electrical engineers [1,2]. Considering Low output voltage level of these sources which is typically between 15-40 volts, DC-DC boost converters are needed to achieve the output voltage level required to connect these sources to the grid or local consumers. Fig. 1 depicts a conventional PV power generation system. As the figure shows PV output voltage is increased by DC-DC converter and then the inverter converts it to the sinusoidal wave ready to be injected to the grid or supply local consumers.

The utilized DC-DC converter should have characteristics such as high voltage stress on semiconductor (especially power switches) and high efficiency. Power circuit of a conventional boost voltage converter is shown in the Fig. 1. Despite the simple structure of this converter, from theoretical stand point in order to obtain high voltage gains, duty cycle should be increased to about unity however in practice this is accompanied by instability and efficiency reduction. On the other hand the voltage stress on power switches is equal to output voltage which is very high thus it is necessary to use switches with larger conduction resistance ($R_{ds\text{-}on}$) which In turn increases the conduction losses. In order to solve the mentioned problems of traditional boost converter many innovative structures such as cascade converters, quadratic converters and Luo converter families have been proposed which deliver high gain at low duty cycle [3-5].

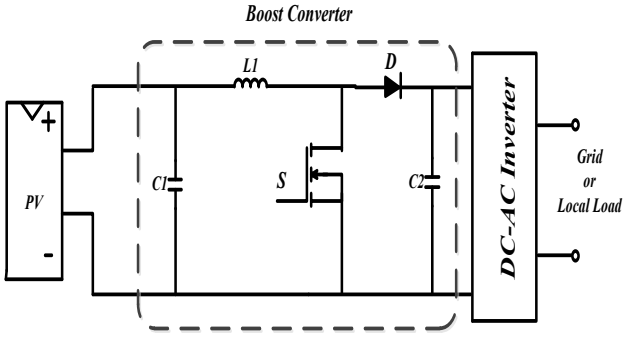


Fig.1. Diagram of Conventional PV power generation system.

However the excessive voltage stress on switches and other semiconductors is still the main drawback of these structures. When electromagnetic elements including coupled inductors and transformers are utilized, the voltage gain of converter can be improved by increasing transformer turn ratio. It is also possible to control the value of voltage stress on power switches in this way [6,7]. The disadvantage of this converters is that higher turns ratio leads to larger leakage inductance which causes problems such as resonance with parasitic capacitance and overvoltage on power switch. However overvoltage on power switches can be reduced by means of Diode-Capacitor active clamp circuit but this approach makes the converter more complex and expensive. Cascading, voltage-doublers, switched-capacitor and switched-inductor are the main approaches to implement DC-DC converters without transformer [8-13]. Some of the main drawbacks of such converters include high number of components, complexity and larger input current ripple which result in increased electromagnetic interference (EMI). This problem can be solved by utilizing interleave technique [14]. The other benefits of interleaving include reduced device stress and lower output capacitance [15]. Several high gain converters have been proposed [16-20]. This paper presents an enhanced conventional boost converter which utilizes interleaving and Diode-Capacitor voltage multiplier cells techniques to deliver high voltage gain with ripple-free input current, low electromagnetic interference and reduced output capacitance.

This paper is organized as follows: Section II describes the proposed converter, followed by its voltage and current analysis in section III. Simulation results are presented in Section IV and conclusions in Section V ends this paper.

2. Proposed Converter

The structure of proposed converter is shown in Fig. 2. This converter consists of *m* inductors, *2m-1* capacitors, 2m diodes and *m* switches. The proposed converter is the combination of switched-capacitor function along with interleaved boost conversion. In fact switched-capacitor voltage multiplier is used to provide m series connected capacitors with equal voltages and self-balance voltages in the output which yields an output voltage of $m(VC_{mm})$. At the converters input interleaved inductors are used to achieve ripple-free input current. Some of the main advantages of proposed converter are as follows: (I) High output voltage gain because of diode-capacitor voltage multiplier. (II) Ripple-free input current due to interleaved inductors. (III) Low voltage stress on switches. (IV) Capacitors with relatively good voltage balance.

For simplicity of analysis it is assumed that the converter is operating in the steady-state and continuous conduction mode (CCM). Considering *m=4* this converter comprises two equivalent circuits which are arised from switches S_1, S_2, S_3 and S_4. The equivalent circuits of each time interval is shown in the Fig. 3.

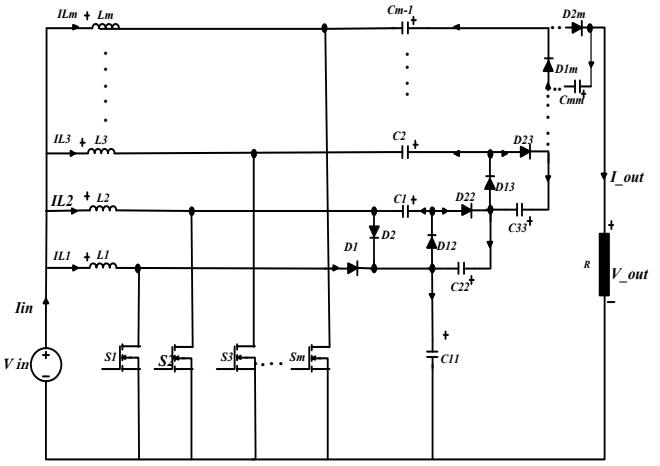
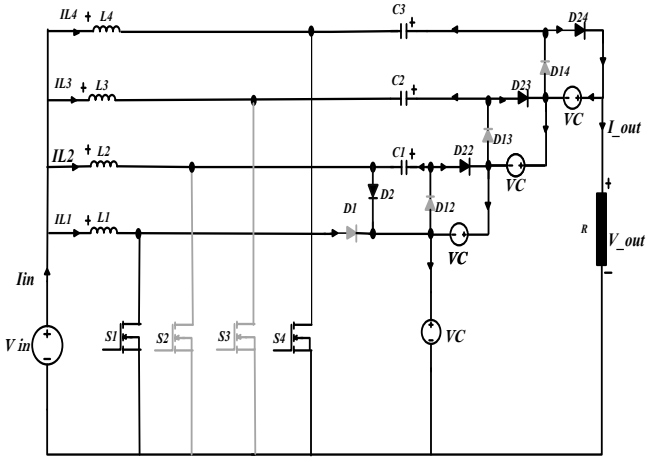
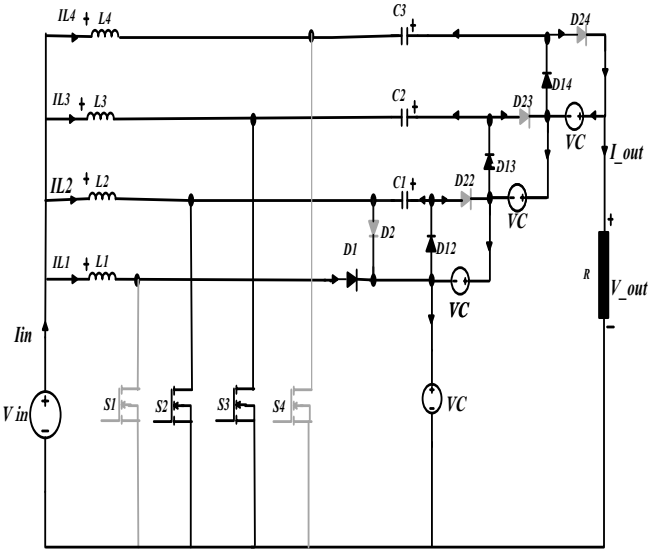


Fig. 2. Proposed converter



(a)



(b)

Fig. 3. Equivalent circuits of proposed converter for *m=4*, (a) first time interval, (b) second time interval

➢ First time interval [$0<t<DT_s$]: Fig. 3(a) depicts the equivalent circuit of converter in the first time interval. In this period S_1 and S_4 are closed and S_2 and S_3 are open. When S_1 and S_4 turn on inductors L_1 and L_4 are connected to V_{in}. If the voltage across C_1 is larger than the voltage across C_{22}, C_1 transfers energy to C_{22} through D_{22}. D_1 and D_{12} are reversed biased due to voltages across C_{11} and C_{22}, and C_3 transfers energy to C_{44} through D_{24}. While S_2 and S_3 are open, Currents through L_2 and L_3 force D_2 and D_{23} to conduct and charge C_{11} and C_{44}. As a result D_{13} and D_{14} are reverse biased and the output voltage is equal to average sum of voltages across C_{11}, C_{22}, C_{33} and C_{44}.

➢ Second time interval [$DT_s<t<T_s$]: the equivalent circuit of this period is shown in Fig. 3(b). In this interval S_2 and S_3 are closed and S_1 and S_4 are open. While S_2 and S_3 conduct, inductors L_2 and L_3 are connected to Vin. Since C_{22} is charged in the first time interval, D_{22} is reverse biased and turns off. Similarly the voltage across C_{33} which is stored in the first period turns D_{23} and D_{24} off. While S_1 and S_4 are closed, currents through L_1 and L_4 turn D_1, D_{12} and D_{14} on and as a result C_1 and C_3 are charged. In this condition the output voltage is the average sum of voltages across C_{11}, C_{22}, C_{33} and C_{44}. The typical waveforms of inductor currents of L_1 and L_4 and the switching sequence for S_1, S_2, S_3 and S_4 are shown in Fig. 4. The input current is the sum of inductors Currents and for input current to be ripple-free, four transistors operate in a complementary manner, i.e., when S_1 and S_4 are closed, S_2 and S_3 are open and vice versa. Since the input current consists of inductors currents, for a ripple-free input current, the current of each pair of inductors should be inversely symmetric with respect to the other pair, as it is shown in Fig. 4.

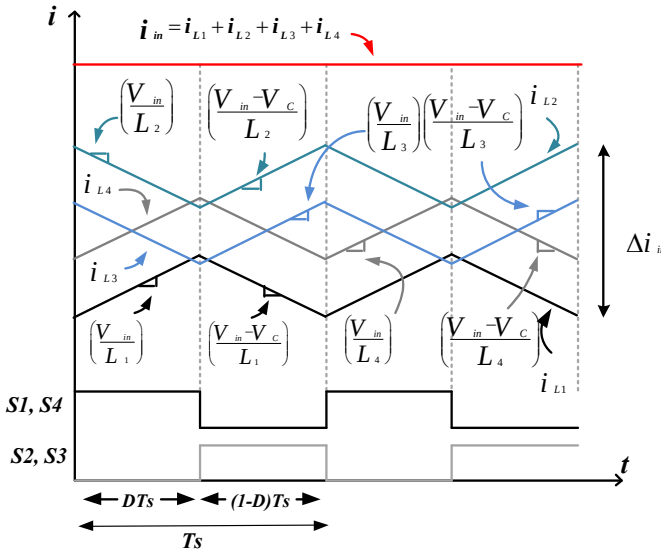


Fig. 4. Inductors currents waveforms and switching sequence for $D=0.5$.

As it can be seen in Fig. 4 while S_1 and S_4 conduct inductors L_1 and L_2 are charged with rate of $(V_{in})/L_1$ and $(V_{in})/L_4$ and when S_1 and S_4 are open they discharge with slope of $(Vin - Vc)/L_4$ and $(V_{in}-V_c)/L_1$. Similarly L_2 and L_3 are charged with Slopes $(V_{in})/L_3$ and $(V_{in})/L_2$ and are discharged by rate of $(V_{in}-V_c)/L_2$ and $(Vin-Vc)/L_3$ while S_2 and S_3 are closed and open respectively.

3. Voltage and Current Analysis

As mentioned earlier high voltage gain is one of the advantages of proposed converter but difference comparing to conventional converter is that the output voltage is equal to sum of V_{C11}, V_{C22}, V_{C33} and V_{C44} which makes it possible to avoid using extreme duty cycle values.

3.1. Voltage Gain Calculation

For sake of simplicity small ripple approximation is made for voltages across C_1, C_2, C_3, C_{11}, C_{22}, C_{33} and C_{44}. Duty cycle D is considered a fraction of each switching period T_s.

Assuming:

$$V_{C1} = V_{C11} = V_{C22} = V_{C33} = V_{C44} = V_C \quad V_{C1} = V_C, V_{C2} = 2V_C, V_{C3} = 3V_C \tag{1}$$

$$V_O = V_{C11} + V_{C22} + V_{C33} + V_{C44} \tag{2}$$

(1) and (2) yields:

$$V_O = 4V_C \tag{3}$$

Under this assumptions and neglecting for now the inductors's equivalent series resistances (ESR) and according to volts-second balance for inductors the equations that represent the average dynamics for inductors L_1 to L_4 are:

$$L_1 \frac{dI_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - V_C) \tag{4}$$

$$L_2 \frac{dI_{L2}}{dt} = D(V_{in} - V_C) + (1-D)(V_{in}) \tag{5}$$

$$L_3 \frac{dI_{L3}}{dt} = D(V_{in}) + (1-D)(V_{in} - V_C) \tag{6}$$

$$L_4 \frac{dI_{L4}}{dt} = D(V_{in} - V_C) + (1-D)(V_{in}) \tag{7}$$

In steady state, the average voltage across the inductors must be equal to zero. Thus, by zeroing the left-hand side of (4) to (7) and using (4), (5), the steady state voltage across V_c may be expressed as:

$$\left.\begin{aligned} V_{in} &= V_C(1-D) \\ V_{in} &= DV_C \end{aligned}\right\} D = (1-D) = D' \tag{8}$$

Therefore equations (4) to (7) are true for $D=0.5$ and:

$$V_{in} = (1-D)V_C \rightarrow \frac{V_C}{V_{in}} = \frac{1}{1-D} \tag{9}$$

Combining (3) and (9) results:

$$\frac{V_O}{V_{in}} = \frac{4}{1-D} \tag{10}$$

According to (10) for $m=N$ voltage gain reaches the value:

$$\frac{V_O}{V_{in}} = \frac{N}{1-D} \tag{11}$$

3.2. Input Current Calculation

As it is shown in Figure 4 current ripple of each inductor is equal to:

$$\Delta i_{L1} = \frac{V_{in}}{L_1} DTs \tag{12}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} D'Ts \tag{13}$$

$$\Delta i_{L3} = \frac{V_{in}}{L_3} D'Ts \tag{14}$$

$$\Delta i_{L4} = \frac{V_{in}}{L_4} DTs \tag{15}$$

Input current ripple which is indicated by is the sum of current ripples of L_1, L_2, L_3 and L_4 which is calculated using expressions (12) to (15):

$$\begin{aligned} \Delta i_{in} &= \Delta i_{L3} - \Delta i_{L2} - \Delta i_{L3} + \Delta i_{L4} \\ \Delta i_{in} &= V_{in} Ts \left(\frac{1}{L_1} D - \frac{1}{L_2} D' - \frac{1}{L_3} D' + \frac{1}{L_4} D\right) \end{aligned} \tag{16}$$

From (16) it's clear that if it is desired to eliminate input current ripple, the value of inductors L_1, L_2, L_3 and L_4 should be equal. With this assumption (16) can be written as:

$$\Delta i_{in} = \frac{V_{in}.Ts}{L_1}(D - D' - D' + D) = \frac{2V_{in}.Ts}{L_1}(2D - 1) \tag{17}$$

Equation (17) shows that input current ripple is linearly proportional to duty cycle. As it was demonstrated before $D=0.5$ givers zero input current ripple.

On the other hand, the equations that represent the average dynamics for C_2 and C_4 are:

$$C_2 \frac{dV_{C2}}{dt} + C_4 \frac{dV_{C4}}{dt} = (di_{L2} + di_{L4}) - \frac{4V_C}{R} \tag{18}$$

And also for C_1 and C_3 we have:

$$C_1 \frac{dV_{C1}}{dt} + C_3 \frac{dV_{C3}}{dt} = (di_{L1} + di_{L3}) - \frac{4V_C}{R} \tag{19}$$

In steady state, the average currents through C_1 and C_4 must be equal to zero, which leads to the following expressions for the currents through L_2 and L_4 and also for L_1 and L_3:

$$I_{L2} + I_{L4} = \frac{1}{2D}\left(\frac{4V_C}{R}\right) \tag{20}$$

$$I_{L1} + I_{L3} = \frac{1}{2(1-D)}\left(\frac{4V_C}{R}\right) \tag{21}$$

According to (20) and (21) the average currents through the inductors can be defined as:

$$\begin{cases} I_{L1} + I_{L2} + I_{L3} + I_{L4} = \frac{1}{D'}\left(\frac{4V_C}{R}\right) = \left(\frac{4}{1-D}\right) I_o = I_{in} \\ D = D' = 1 - D \end{cases} \tag{22}$$

3.3. Calculation of Practical efficiency and Voltage Gain of the Proposed Converter

The Voltage gains are expressed by (10) and (11) correspond to an ideal case as the inductors's ESR has been neglected. In order to calculation the voltage gain and efficiency of the converter in practical applications, converter's non-ideations should be taken into account.

In a practical implementation, the leakage resistance in inductors significantly limits this gain and expressions (4) to (7) should be rewritten to address the impact of inductors equivalent series resistances.

$$L_1 \frac{di_{L1}}{dt} = d(V_{in} - R_{L1} i_{L1}) + (1-d)(V_{in} - R_{L1} i_{L1} - V_C) \tag{23}$$

$$L_2 \frac{di_{L2}}{dt} = d(V_{in} - R_{L2} i_{L2} - V_C) + (1-d)(V_{in} - R_{L2} i_{L2}) \tag{24}$$

$$L_3 \frac{di_{L3}}{dt} = d(V_{in} - R_{L3} i_{L3}) + (1-d)(V_{in} - R_{L3} i_{L3} - V_C) \tag{25}$$

$$L_4 \frac{di_{L4}}{dt} = d(V_{in} - R_{L4} i_{L4} - V_C) + (1-d)(V_{in} - R_{L4} i_{L4}) \tag{26}$$

Where R_{L1} is the ESR resistance of L_1 And also for the other elements L_2 to L_4.

In steady state, (23) to (26) becomes:

$$\begin{aligned} 0 &= D(V_{in} - R_{L1} I_{L1}) + (1-D)(V_{in} - R_{L1} I_{L1} - V_C) = \\ & V_{in} - R_{L1} I_{L1} - D'V_C \end{aligned} \tag{27}$$

$$\begin{aligned} 0 &= D(V_{in} - R_{L2} I_{L2} - V_C) + (1-D)(V_{in} - R_{L2} I_{L2}) = \\ & V_{in} - R_{L2} I_{L2} - DV_C \end{aligned} \tag{28}$$

$$\begin{aligned} 0 &= D(V_{in} - R_{L3} I_{L3}) + (1-D)(V_{in} - R_{L3} I_{L3} - V_C) = \\ & V_{in} - R_{L3} I_{L3} - D'V_C \end{aligned} \tag{29}$$

$$\begin{aligned} 0 &= D(V_{in} - R_{L4} I_{L4} - V_C) + (1-D)(V_{in} - R_{L4} I_{L4}) = \\ & V_{in} - R_{L4} I_{L4} - DV_C \end{aligned} \tag{30}$$

By replacing (20), (21) in (27) to (30) and considering equal ESR for inductors such that $R_{L1}=R_{L2}=R_{L3}=RL4=R_L$ then practical voltage gain equals to:

$$\frac{V_O}{V_{in}} = \frac{4}{(1-D) + \frac{R_L}{D(1-D)R}} \tag{31}$$

Practical efficiency of the converter is derived by replacing (22), (31) as follows:

$$\begin{aligned} \eta &= \frac{V_o I_o}{V_{in} I_{in}} = \left(\frac{4}{(1-D) + \frac{R_L}{D(1-D)R}}\right)\left(\frac{1-D}{4}\right) = \\ & \frac{(1-D)}{(1-D) + \frac{R_L}{D'^2 R}} = \frac{1}{1 + \frac{R_L}{D'R}} \end{aligned} \tag{32}$$

4. Simulation Results

In order to confirm and validate the operation of proposed converter, a sample converter for *m=4* is simulated in PSIM. Simulation parameters are mentioned in table I.

Table 1. Simulation Parameters

Parameter	*Values*
V_{in} *(Input voltage)*	*48 v*
V_o *(Output voltage)*	*384 v*
D(Duty cycle)	*50%*
F_s *(Switching frequency)*	*50 KHz*
P_{out} *(Output power)*	*1.47 KW*
$\frac{V_o}{V_{in}}$ *(Voltage gain)*	*8*
$L_{mm}(L_1=L_2=L_3=L_4)$	*160 µH*
$C_{m-1}(C_1=C_2=C_3)$	*8µf*
$C_{mm}(C_{11}=C_{22}=C_{33})$	*8µf*
Mosfets(IRFP4668PBF)	$R_{ds-on}=8m\Omega$, $V_{ds}=200v$, $I_d=130\ A$
R(Load)	*100 Ω*

Inductor currents and input currents waveforms are illustrated in Fig. 5. As it can be seen the current of each inductor has 180° phase shift comparing to the other one. This property is utilized to reduce the input current ripple and as Fig. 5 shows the input current is almost ripple-free.

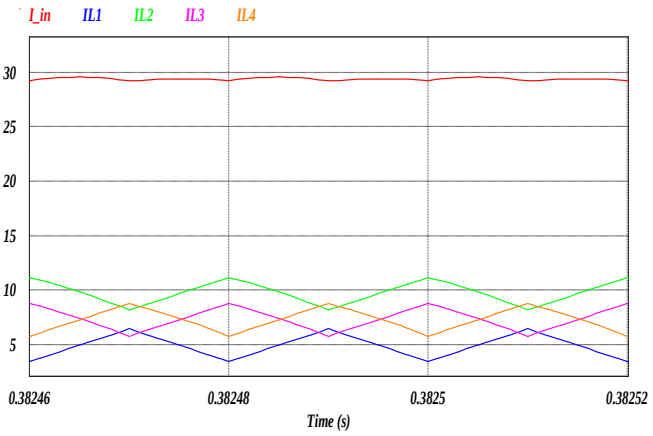


Fig. 5. Inductors and input currents waveform

The output voltage is shown in Fig. 6. The average value of converter's output voltage is equal to 368.88 V which is very close to the expected value for 50% duty cycle that is 384 volts. The difference between calculated and simulated results of output voltage is due to parasitic elements which are considered in (10).

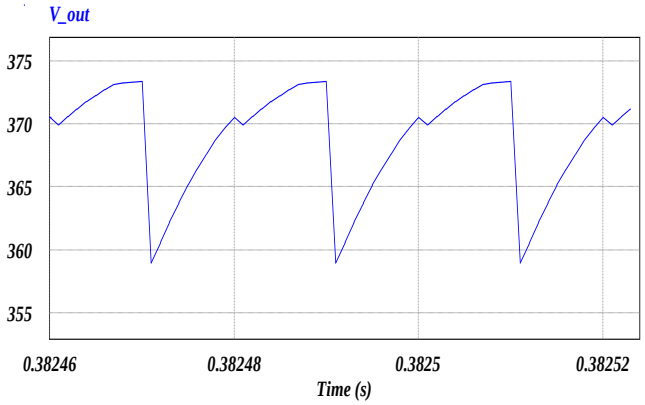


Fig. 6. Output voltage waveform

The capacitors voltages which have a relatively good voltage balance is shown in Fig. 7. Despite the fact that capacitor values are very low (8µf), their voltages experience very low ripple. This is another benefit of low input current. Converter's practical efficiency in normal load of 1346.89 W is 95.4%.

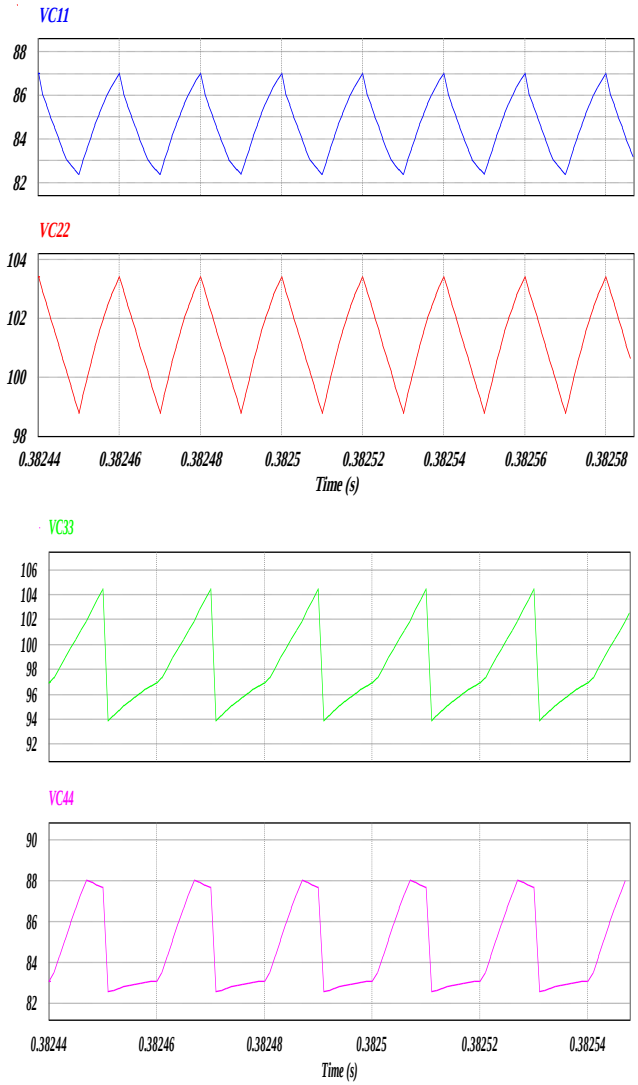


Fig. 7. Voltages across capacitances C_{11}, C_{22}, C_{33} and C_{44}.

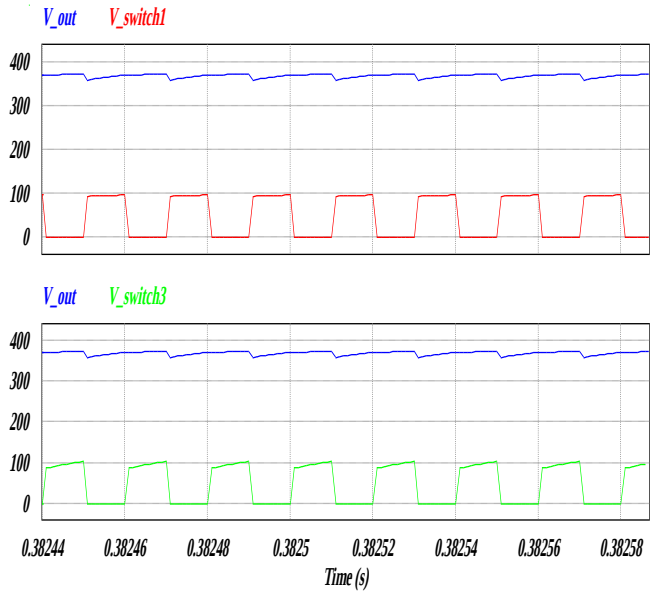


Fig. 8. Comparison between output voltage and voltage across switches S_1 and S_3.

5. Conclusion

In this paper an interleaved high step-up DC-DC converter for renewable energy systems application such as photovoltaic and fuel cell is proposed. This converter benefits from substational advantages including:

i) High voltage gain without utilizing extreme duty cycle values or transformers.

ii) Input current ripple elimination which results in electromagnetic interference reduction and low conduction losses.

iii) Low voltage stress on power switches and other semiconductors that allows utilization of low resistance switches.

iv) Relatively low output capacitance.

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