Design of a Transformer-less Grid-Tie Inverter Using Dual-Stage Buck and Boost Converters

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Abstract- This paper introduces a topology for transformer-less pure sine wave grid-tie inverter (GTI) for photovoltaic (PV) applications. The proposed GTI employs a dual-stage switch mode boost converter, a dual-stage switch mode buck converter, an H-bridge inverter and a T-LCL immittance conversion circuit. For switching of GTI power circuit, a combination of sinusoidal pulse width modulation (SPWM) and square wave signal under grid synchronization conditions are applied. As the suggested method is entirely transformer-less, it astonishingly reduces Total Harmonic Distortion (THD) which is less than 0.1%, minimizes the size of the inverter and increases inverter efficiency up to 97%. The T-LCL immittance conversion circuit not only reduces the harmonic distortation of inverter output but also provides a nearly constant output current thereby stabilizing the system instanteously. Using the designed values of circuit components, the overall performance of the proposed inverter is simulated by using PSIM software. The simulation results not only show that the proposed inverter eliminates vast harmonics but also prove that it is highly efficient, compact in size and cost effective due to being transformer-less.

Keywords- Boost Converter; Buck Converter; T-LCL Immittance Converter; Grid-Tie Inverter (GTI)

1. Introduction

The world's climate change is a serious threat to our planet. Carbon dioxide gas (CO_2) being produced by the constant use of fossil fuel is destroying our planet. Moreover, we do know fossil fuel and its possibilities is not a solution to our power crisis; knowing how the cost of fossil fuels is increasing day by day, and its demerits. On the basis of global front, creating the use of solar energy, which is clean, sustainable, renewable and good for environment, seems to be one of the best options. As Bangladesh is in a geographical location that receives a lot of sunlight, therefore by implementing a highly efficient and cost effective solar module system can be supportive in reducing power crisis, as it helps in producing large amount of power at very low cost [1-2]. Hence among all renewable energy sources, photovoltaic energy is considered to be one of the highest growing energy sources in Bangladesh.

In photovoltaic (PV) system solar energy is converted into electrical energy through PV arrays [3-6].There are two mandatory tasks in PV system. They are-(1) utilizing maximum energy from PV arrays, (2) using the most reliable, highly efficient and cost effective configuration for the power converter in order to inject only active current into the grid, i.e. pure sinusoidal current in phase with the grid voltage [6]. In a conventional inverter, transformer is used to match the inverter output with the utility grid output [7-10]. But the only limitation here is that transformers are bulky, heavy weighted and costly equipment. Moreover transformer highly influences the enhancement of Total Harmonic Distortion (THD) in inverter [11-12].

In this paper, a boost power converter is recommended instead of transformer in order to achieve low THD as well as high efficiency. The boost power converter converts a large scale of voltage similar to the grid value but a single-stage boost converter requires a high duty cycle which is inconvenient for MOSFET switching. Therefore, the DC-DC power conversion is employed through a dual-stage boost converter to obtain suitable duty cycle for MOSFETs switching. Likewise, a dual-stage buck converter is also used to synchronize the output frequency with the grid. Instead of using a conventional low-pass LC filter, a T-LCL immittance converter is employed in the proposed inverter, which not only suppresses the harmonics contained in the inverter output but also maintains a constant output current for any type of load, and thus stabilizes the inverter output [13].

The proposed inverter configuration consists of five main parts. They are-1) a PV array for converting solar energy to electrical energy, 2) a dual-stage DC-DC boost converter to step up PV array voltage to the grid level, 3) an H-bridge DC-AC converter to acquire AC voltage, 4) a T-LCL immittance converter to deliver a nearly constant as well as filtered output current, and 5) a dual-stage AC-DC buck converter which is used as gate signal by combining SPWM and square wave for switching the gate drive of the inverter. The block diagram of proposed inverter is shown in Fig.1.

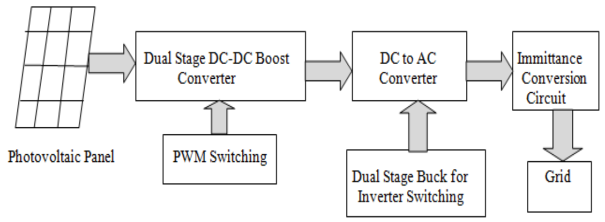

Fig.1. Block diagram of proposed GTI

2. Design of Dual-stage Boost Converter

This section describes the design of a dual-stage DC-DC boost converter for converting unregulated voltage of PV array to a fixed high level regulated voltage which is same as the grid value (312V peak or 220V rms in Bangladesh). In this paper, a dual-stage (N=2) boost converter is proposed since the duty cycle of single-stage boost converter would be large (above 90%), which is not convenient for MOSFET switching. Dual-stage converter provides a more symmetrical duty cycle, and reduces the voltage stress on the MOSFETs. Here the conversion of boost converter is done based on the conversion ratio, $x^2 = 312/24$ which is converted voltage from 24V DC to 86V DC in the first-stage and 86V DC to 312V DC in the second-stage. The design parameters of the first- and second-stage boost converters are listed in Table-1 and Table-2 respectively

Table 1. Design of first-stage boost converter

Symbol	*Actual Meaning*	*Value*
V_{in}	Given input voltage	24V
V_{out}	Desired average output Voltage	86V
f_s	Minimum switching frequency of the converter	20KHz
I_{LMax}	Maximum inductor current	260A
ΔI_L	Estimated inductor ripple current (1.75% of inductor current)	4.55A
ΔV_{out}	Desired output voltage ripple (0.05% of output voltage)	44mV
I_{out}	Maximum output current(V_{out}/R)	4.3A

Table 2. Design of second-stage boost converter

Symbol	*Actual Meaning*	*Value*
V_{in}	Given input voltage	86V
V_{out}	Desired average output Voltage	312V
f_s	Minimum switching frequency of the converter	21KHz
I_{LMax}	Maximum inductor current	230A
ΔI_L	Estimated inductor ripple current (26% of inductor current)	60A
ΔV_{out}	Desired output voltage ripple (0.1% of output voltage)	0.35V
I_{out}	Maximum output current(V_{out}/R)	10.4A

2.1 Duty Cycle

Maximum duty cycle for the first-stage is,

$$D_{1,boost} = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{24}{86} \approx 0.72$$

Maximum duty cycle for the second-stage is,

$$D_{2,boost} = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{86}{312} \approx 0.72$$

2.2 Inductor Selection

In the boost converter, a smoothing inductor is used in series with the input voltage to limit the current ripple of converter. In conventional processes, inductor value is normally chosen from the recommended data sheets. But here voltage conversion is occurred at a large scale (24V DC to 86V DC) and hence no inductor value is available in the data sheets for this voltage conversion range. Therefore, the following equation is a good estimate for choosing the right output value of inductor for the first-stage boost converter [14-15]:

$$L_{1,boost} = \frac{V_{in}(V_{out} - V_{in})}{\Delta I_L \times f_s \times V_{out}} = \frac{24 \times (86 - 24)}{4.55 \times 20000 \times 86} \approx 190\mu\text{H}$$

Similarly, the same method can be used in order to choose the inductor value for the second-stage boost converter:

$$L_{2,boost} = \frac{V_{in}(V_{out} - V_{in})}{\Delta I_L \times f_s \times V_{out}} = \frac{86 \times (312 - 86)}{60 \times 21000 \times 312} \approx 50\mu\text{H}$$

2.3 Capacitor Selection

The following equation is used to adjust the output capacitor value for a desired output voltage ripple. The estimated capacitor value for the first stage is [14-15]:

$$C_{1,boost} = \frac{I_{out} \times D}{f_s \times \Delta V_{out}} = \frac{4.3 \times 0.72}{20000 \times .044} \approx 3.5mF$$

And the estimated capacitor value for the second-stage is,

$$C_{2,boost} = \frac{I_{out} \times D}{f_s \times \Delta V_{out}} = \frac{10.4 \times 0.72}{21000 \times .35} \approx 1mF$$

2.4 The Designed 24-312V DC-DC Boost Converter

The power converter which consists of two boost converters and two PWM gate pulses to drive the MOSFETs is shown in Fig.2. The output of the designed boost converter simulates using PSIM is shown in Fig.3 which indicates that the output of the first-stage is 86V and second-stage is 312V DC and which is later converted to 312V AC (or 220V rms) using an H-bridge inverter.

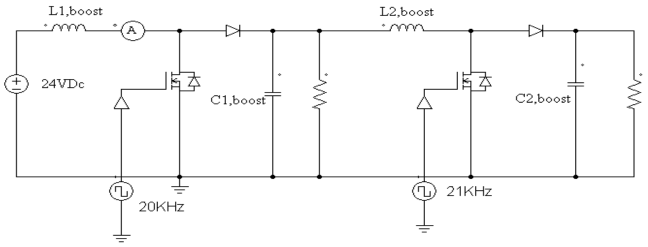

Fig.2. PSIM simulation circuit of the dual-stage boost converter using the designed circuit parameters

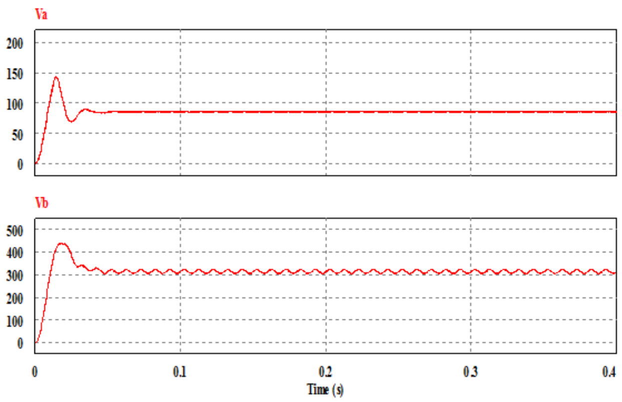

Fig.3. Boost converter output: V_a is the first-stage output (86V) and V_b is the second-stage output (312V)

3. Design of Dual-stage Buck Converter

This section describes the design of a dual-stage AC-DC buck power converter. Here AC voltage sample is taken from grid which is converted into pulsating DC through full bridge rectifier. Then 220V pulsating DC is converted into 5V DC by using buck power converter. In this paper, a dual-stage (N=2) buck converter is proposed since the duty cycle of the single-stage buck converter is very low (below 5%) and thus it will not be convenient for MOSFETs switching.

Dual-stage converter provides a more symmetrical duty cycle and reduces voltage stress on MOSFETs. Here the conversion of buck converter is done by basing on the conversion ratio, $x^2 = 220/5$ which converts voltage from 220V DC to 33V DC in the first-stage and 33V DC to 5V DC in the second-stage. The design parameters of the first- and second-stage buck power converters are listed in Table-3 and Table-4 respectively.

Table 3. Design of first stage buck converter

Symbol	*Actual Meaning*	*Value*
V_{in}	Input RMS voltage	220V
V_{out}	Desired RMS output voltage	33V
f_s	Minimum switching frequency of the converter	25KHz
I_{LMax}	Maximum inductor current	74A
ΔI_L	Estimated inductor ripple current (30% of Inductor current)	22A
ΔV_{out}	Desired output voltage ripple (1.60% of output voltage)	0.05V
I_{out}	Maximum output current(V_{out}/R)	4.3A

Table 4. Design of second stage buck converter

Symbol	*Actual Meaning*	*Value*
V_{in}	Given input voltage	33V
V_{out}	Desired average output voltage	5V
f_s	Minimum switching frequency of the converter	6KHz
I_{LMax}	Maximum inductor current	8A
ΔI_L	Estimated inductor ripple current (4.4% of Inductor current)	0.35A
ΔV_{out}	Desired output voltage ripple (1.40% of output voltage)	70mV
I_{out}	Maximum output current(V_{out}/R)	0.83A

3.1 Duty Cycle

Maximum duty cycle for the first stage is,

$$D_{1,buck} = \frac{V_{out}}{V_{in}} = \frac{33}{220} \approx 0.15$$

Maximum duty cycle for the second stage is,

$$D_{2,buck} = \frac{V_{out}}{V_{in}} = \frac{5}{33} \approx 0.15$$

3.2 Inductor Selection

In the buck converter, a smoothing output inductor is used to reduce current ripple in the output side of the circuit. In conventional processes, inductor value is chosen from the recommended data sheets. But no inductor range has been given for a very large scale voltage conversion (220V to 33V) in buck power converter. Therefore, the following equation is a good estimate for choosing the right inductor value for the first-stage buck converter [14-15]:

$$L_{1,buck} = \frac{V_{out}(V_{in} - V_{out})}{\Delta I_L \times f_s \times V_{in}} = \frac{33(220-33)}{22 \times 25000 \times 220} \approx 50\mu\text{H}$$

Similarly, the following equation is a good estimate for choosing the inductor value for the second-stage buck converter.

$$L_{2,buck} = \frac{V_{out}\left(V_{in} - V_{out}\right)}{\Delta I_L \times f_s \times V_{in}} = \frac{5(33-5)}{0.35 \times 6000 \times 33} \approx 2mH$$

3.3 Capacitor Selection

The basic selection of the output capacitor is based on the ripple current, ripple voltage and loop stability considerations. In the presented design, the following equation can be used to adjust the output capacitor values for the first-stage buck conversion [14-15].

$$C_{1,buck} = \frac{\Delta I_L}{8 \times f_s \times \Delta V_{out}} = \frac{22}{8 \times 25000 \times 0.55} \approx 200\mu F$$

Similarly, the following equation can be used to adjust the output capacitor value for the second-stage buck conversion:

$$C_{2,buck} = \frac{\Delta I_L}{8 \times f_s \times \Delta V_{out}} = \frac{0.35}{8 \times 6000 \times 0.07} \approx 100\mu F$$

3.4 The Designed 220V-5V AC-DC Buck converter

The power converter, which consists of a rectifier circuit, two buck converters, and one set of PWM gate pulse to drive the buck MOSFETs is shown in Fig.4. The output of the first-stage buck is 33V rms (44V peak) and of the second-stage buck output is 5V rms (7.07V peak) as shown in Fig.5.

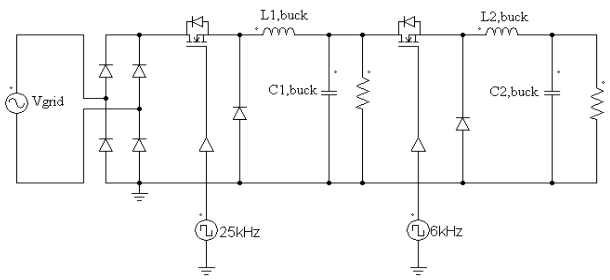

Fig.4. PSIM simulation circuit of the dual-stage buck converter using the designed circuit parameters

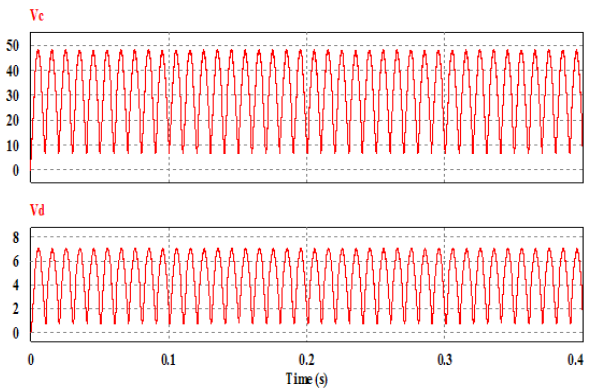

Fig.5. Buck converter output: V_c is the first-stage output (44V) and V_d is the second-stage output (7.07V)

4. Proposed Grid-Tie Inverter

4.1 Grid Synchronization

The output voltage of a grid-tie inverter should maintain some fixed requirements so that it can provide power to utility grid [6-7], [11]. The requirements are given below:

i. The output voltage amplitude of the grid-tie inverter should be same as the grid amplitude.
ii. The frequency of inverter should be same as the grid frequency (50Hz in Bangladesh).which is
iii. The phase of inverter should match with the grid.

To fulfill the grid synchronization, a buck converter is employed. The buck converter is used to take sample from the grid. The sampled 5V DC is used to generate the SPWM signal which ensures that the output voltage from GTI will have the same frequency as the utility grid. During synchronization, the inverter produces output which is in phase with the grid by employing a 50Hz square-wave pulse taken from the grid and applying AND operation with comparator output which generates four sets of switching signals. With this kind of switching the output voltage and current of GTI is controlled.

The boost converter is designed so that the inverter output amplitude is matched with the utility grid (312V peak or 220V rms). Then the GTI is directly tied with the grid where the load is quite larger than GTI. Therefore, force is transmitted to the GTI for generating power from PV array into the grid.

4.2 Power Circuit

In the proposed inverter circuit, four MOSFETs have been used for switching purpose. A DC-DC boost power converter, an AC-DC buck converter and an H-bridge inverter are employed in the circuit as shown in Fig.6. The design of the DC-DC boost converter is shown in section 2 and it is used to step up the unregulated input voltage from 24V to regulated voltage 312V, which is then finally converted to 312V pure AC (220V rms) applicable to the grid by using inverter.

4.3 Switching Circuit

The switching control circuit of the proposed inverter contains analogue and digital circuits. Here, the analogue circuit generates pulse for the power circuit while the digital circuit controls the sequence of gate drive [11]. In conventional inverter design, Sinusoidal Pulse Width Modulation (SPWM) is generally used to get AC output [4],[7-8].

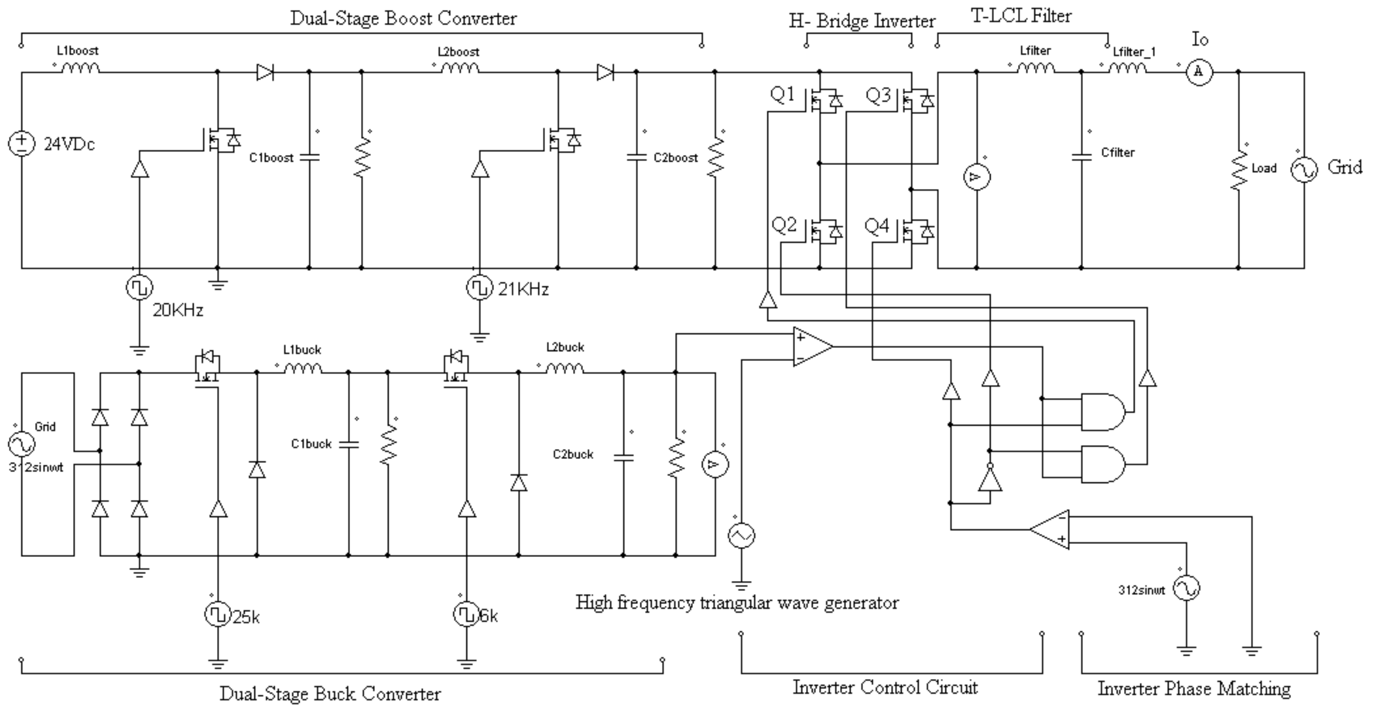

Fig.6. Proposed transformer-less grid-tie inverter

However, in this article, the combination of SPWM and a square wave is used for inverter switching as this new technique reduces the losses by reducing switching frequency [4]. The output of the buck converter is compared with high frequency triangular wave (20KHz) using comparator to build SPWM signals. A square wave with 50% duty cycle and frequency similar to the grid frequency (50 Hz in Bangladesh) and in phase with the grid voltage is used. The square wave is also passed through a NOT gate which produces a signal of 1800 out of phase with the original signal.

The inverter requires four sets of gate signal as it uses four MOSFETs in the circuit. Under this situation two sets of SPWM signal and two sets of AND gate operations are performed. The four sets of gate signal can be labeled into two groups. The first group consists of MOSFETs Q1 and Q4 while the second group consists of MOSFETs Q2 and Q3. When Q4 is switched on by the square wave signal, SPWM appears at Q1, and at that time Q2 and Q3 switches are off. Again when Q2 is turned on by the square wave signal, SPWM appears at Q3, at that time Q1 and Q4 switches remain off. For Q1 and Q4 pair, positive voltage emerges across the load while for Q2 and Q3 pair, negative voltage emerges across the load. The gate switching signals for Q1 and Q3 are shown in Fig.7. Thus the inverter produces a full square wave output which contains lots of harmonics at the output side of the inverter as shown in Fig.8 in section 5.

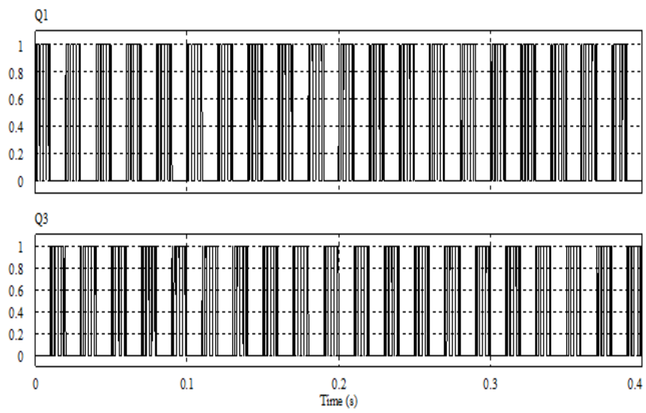

Fig.7. Switching signal from control circuit to MOSFETs Q1 and Q3

4.4 Filter Circuit

To eliminate harmonics from the inverter output, a filter circuit is employed. In conventional inverters, an LC filter is used. In this article, a T-LCL immitance converter is employed as shown in Fig.6 which consists of two inductors L1 and L2 as well as a capacitor, C in T shape. The equations of the output current and efficiency of the filter are found as [13], [16], [17]:

$$I_2 \cong \frac{V_1}{Z_0}\left[1-\frac{1}{Q}\frac{Z_2}{Z_o}\right] \tag{1}$$

$$\eta \cong \frac{1}{1+\frac{1}{Q_1}\frac{Z_2}{Z_0}+\frac{1}{Q_2}\frac{Z_0}{Z_2}} \tag{2}$$

where, V_1 is the input voltage, Z_2 is the load impedance and Z_0 is the characteristic impedance which determined by the filter components, L and C:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3}$$

Q is the quality factor

$$Q = \frac{\omega L}{r} \tag{4}$$

Here ω is the angular frequency, $\omega = 2\pi f$ and r is the internal resistance of the inductor.

For special case $Q \cong Q_1 \cong Q_2$ and $Z_0 \cong Z_2$. The efficiency characteristic of T-LCL filter configuration is the same and approximate as:

$$\eta \cong 1 - \frac{2}{Q} \tag{5}$$

When the internal resistance of the inductor is negligible or zero, the quality factor becomes infinity. Under this condition, the second term becomes zero and giving the ideal condition:

$$I_2 \cong \frac{V_1}{Z_0} \tag{6}$$

From equation (6), it is observed that the output current of T-LCL filter is independent of load. Therefore, in the proposed inverter, a T-LCL immittance converter is applied as a filter circuit because it is not only capable of reducing harmonic distortion but also helpful in maintaining constant current at the load.

The value of C and L of T-LCL filter (considering Butterworth type) is calculated using the condition of cut-off frequency of low pass filter,

$$Z_O = X_C = \frac{1}{2\pi f_C C} \tag{7}$$

where, Z_0 is the characteristic impedance given by equation (3). In the proposed design, the cutoff frequency, f_C =50Hz and characteristic impedance is assumed as 20Ω. Therefore, the values of C and L are calculated using Eqs. (7) and (3) as,

$$C = \frac{1}{2\times\pi\times f_C \times Z_0} = \frac{1}{2\times\pi\times 50\times 20} \approx 0.159\,mF$$

$$L = CZ_0^2 = 0.159\times10^{-3}\times(20)^2 \approx 63.60mH$$

5. Simulation Results and Discussion

5.1 Inverter Output Voltage

Fig.8 shows the simulated output voltage waveform which is non-sinusoidal, distorted and contains excessive harmonics. A low-pass T-type LCL filters is employed at the output terminal of the inverter to reduce the harmonics which produces a pure sinusoidal output voltage.

After filtering, 220V (RMS), 50Hz pure sine wave output voltage is obtained as shown in Fig.9. It is observed that the output voltage of the proposed inverter becomes stable after a couple of cycles since it is connected to the grid.

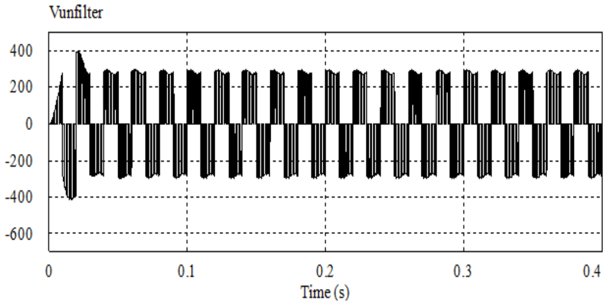

Fig.8. Output voltage waveform without filtering in PSIM

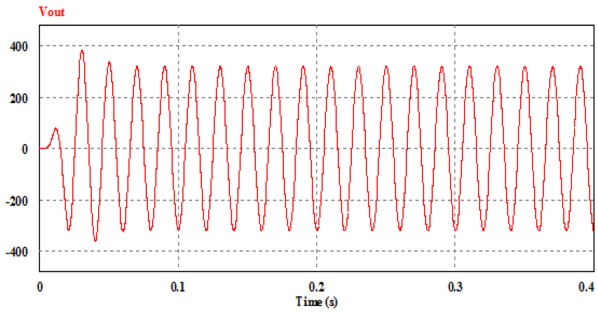

Fig.9. Output voltages after filtering in PSIM

5.2 Inverter Output Current

The peak value of the inverters output current is an important factor in designing the inverter stack size. The inverter current rating is normally determined by the filter impedance and the rated load impedance in steady state condition. The output current should be maintained constantly. Fig.10 shows the inverter output current which becomes stable within a couple of cycles (0.04sec.).

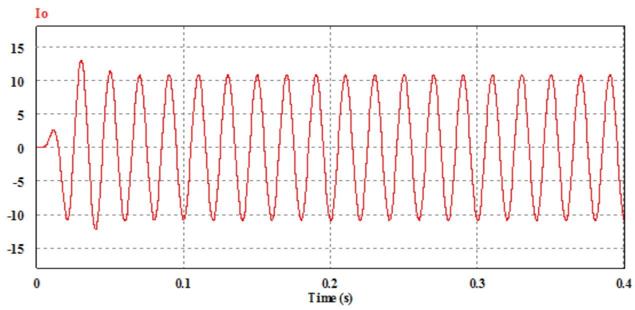

Fig.10. Output voltages after filtering in PSIM

5.3 FFT analysis of Inverter

Fig.11 presents the FFT analysis of output voltage in unfiltered and filtered conditions. The Fast Fourier

Transform ensures that the unfiltered inverter output has harmonics with mentioned value whereas the filtered output has only fundamental component which lies in 50Hz and the rest of the harmonics are negligible. After filtering, the output has very low level of THD which is less than 0.1% because the proposed circuit is totally transformer-less.

In order to test the performance of the inverter, the load current was measured for both R and RL load with and without applying the filter circuit. The inverter was tested by employing both LC and LCL filter. The load impedance was varied from 5Ω to 100Ω for both R and RL load by considering the characteristic impedance as Z0=20Ω. It was observed that without filter, the load current varies in a larger range than that of the load current with filter circuit being employed as shown in Fig.12. It was also observed that the load current for resistive and inductive load were almost constant, which confirms that the output current is independent of load when a T-LCL filter is used.

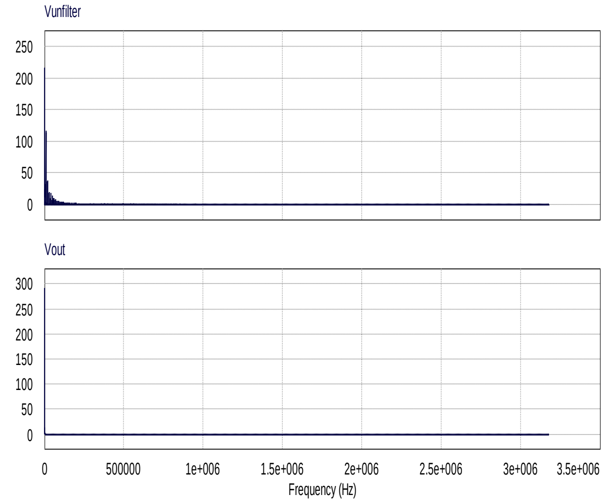

Fig.11. Output Voltage's FFT unfiltered and filtered condition in PISM

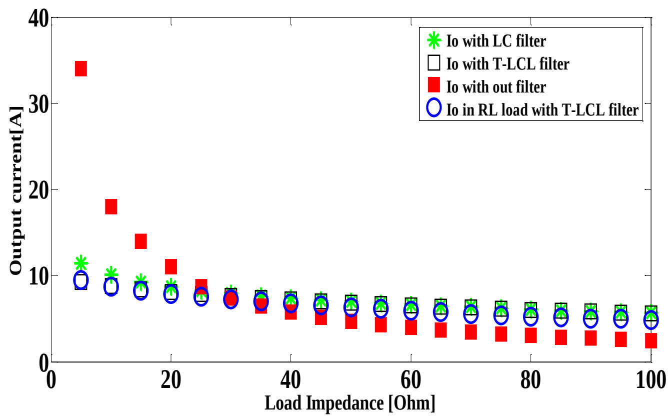

Fig.12. Output current vs. load impedance

5.4 Inverter Efficiency

The inverter's efficiency is calculated using the following formula:

$$\eta = \frac{p_{out}}{p_{in}} \times 100\% \quad (8)$$

where Pin and Pout are the input and output power of the inverter respectively. By varying resistive load, the efficiency of the inverter was monitored with LC and T-LCL filter as illustrated in Fig.13. It is observed that the efficiency of T-LCL filter is slightly higher than that of the conventional LC filter due to its constant current characteristic.

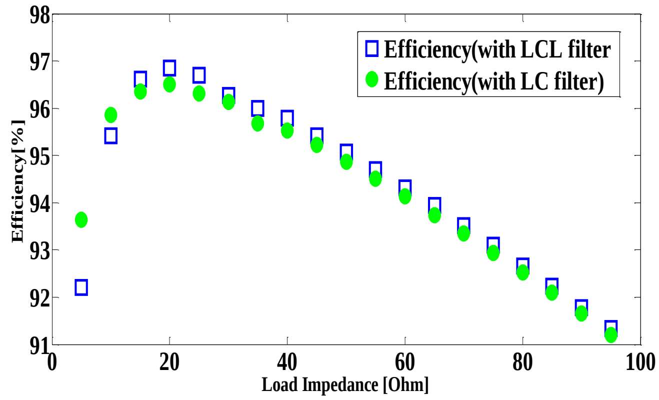

Fig.13. Efficiency vs. Load impedance

6. Conclusion

Mathematical modeling, analysis and computer simulation of a transformer-less GTI is presented in this paper. The simulation result ensures that the frequency of the inverter output voltage is exactly 50Hz with a magnitude of 312V peak (220V rms) and is in same phase with the utility grid voltage. The total harmonic distortion (THD) of the inverter output is less than 0.1% which is much lower than the IEEE519 standard, and the efficiency of the inverter also found up to 97%. Therefore the results verified the viability of the proposed transformer-less inverter for grid-tie photovoltaic applications and confirmed the capability of the inverter to feed a sinusoidal voltage to the utility grid.

In future, hardware of the proposed transformer-less GTI will be constructed with the help of a microcontroller.

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