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Clamping of Switch Peak Voltage with Diode and Transformer at Output of Class E Amplifier for Renewable Energy Applications

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Abstract- Solar cells should have shortened life time in order to achieve effect circulation of renewable energy. In the semiconductor manufacturing operations, plasma process such as CVD, etching dominates large value of energy consumption. Reducing energy consumption of plasma processing is urged. With using switching power amplifier as a replacement of linear amplifier, significant energy reduction can be done. However, switching power amplifier has a drawback of destruction of switching device due to high transient switch voltage during practical operation. In this paper, a voltage clamp circuit consists of diode and transformer is proposed. This circuit reduces the transient peak switch voltage of the class E amplifier. With adjusting winding ratio of transformers, clamp voltage can be arbitrary value. Namely, the diodes can be inactivated in ordinary variations of load impedance. But, it activates in sudden and significant change of load impedance. Simulation results showed that the proposed diode clamp circuit successfully reduces the transient peak switch voltage.

Keywords- Voltage clamp circuit, renewable energy, transformer, transient peak switch voltage, maximum permissible value.

1. Introduction

It is expected that the Class E amplifier [1-3] can be serve as a replacement of low efficient linear power amplifiers of RF energy sources, especially in application of plasma generator [4].

In plasma generation, the load impedance varies significantly during operation [5, 6]. In the plasma chamber, the load resistance is equal to via impedance matcher when the plasma spark resumes. On the other hand, the load resistance is approximately an open circuit when the plasma spark diminishes. Because the load impedance suddenly varies to an open circuit during operation, the amplitude of output voltage of the class E amplifier becomes very high and sometimes a high switch voltage destroys the switching device. In order to avoid a high peak switch voltage, several voltage clamp methods were proposed. In [7] and [8], a Zener diode across the switch [7] and the choke coil [8] of a class E amplifier were presented.

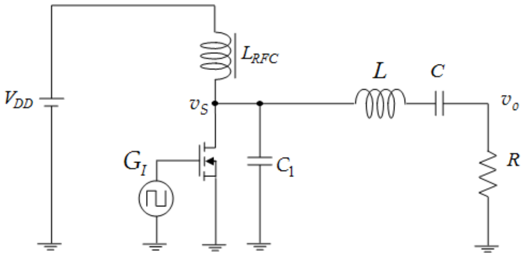

Fig. 1. Basic circuit of voltage switching class E amplifier.

However, in both methods, a significant power loss occurred in the Zener diode. Lossless voltage clamping with transformer and diode was proposed [9]. However, it could not reduce the peak switch voltage as expected due to leakage inductance of the transformer. Hence, lossless voltage clamping using transmission transformer was introduced [10]. These efforts to reduce the peak switch voltage were dedicated for the steady-state operation.

Therefore, due to leakage inductance of the transformer, they could not reduce the transient peak switch voltage enough. Instruments company MKS invented diode clamping circuit to reduce the transient peak switch voltage [5]. However, the peak switch voltage could not be reduced enough by using the circuit.

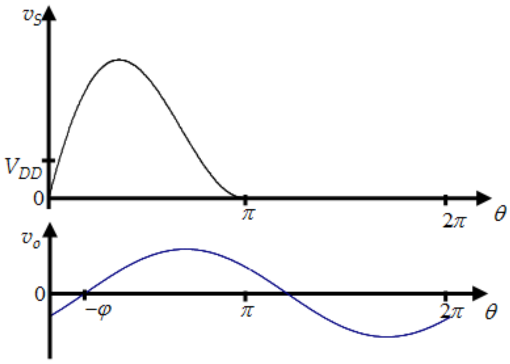

Fig. 2. Switch voltage waveform and output voltage waveform at duty ratio $D = 0.5$.

In this paper, a voltage clamp circuit for the class E amplifier is proposed to reduce the transient peak switch voltage. This circuit clamps the output voltage of the class E amplifier when the amplitude of output voltage goes over the designated clamp voltage level. A rough estimation of the amplitude of output current when the output voltage is clamped is described. It was shown with simulation that the transient peak switch voltage was reduced by the proposed clamp circuit.

2. Class E Amplifier and Peak Switch Voltage due to Load Variation

A basic circuit of the zero-voltage switching (ZVS) class E amplifier [1] is shown in Fig. 1. This circuit inputs a dc voltage from the dc power supply V_{DD}. The MOSFET switch is driven by a high-frequency gate signal and it switches periodically at the switching frequency f. A periodical switch voltage v_S, which is shown as Fig. 2, is generated across drain and source of the switching device. The L-C band-pass filter extracts the fundamental frequency component from the switch voltage waveform v_S. A sinusoidal voltage waveform is output to the load resistance R. A choke inductance L_{RFC} is high enough to reduce the ac component in it. Hence, the input current through the choke inductance can be considered as a dc current. The loaded-quality factor of L-C-R band-pass filter is high enough so that the output current can be considered as a pure sinusoid. Hence, the current through the switch is the sum of a dc current and a sinusoidal current. The class E amplifier can achieve high efficiency when the switch turns on at zero voltage.

In this paper, the class E amplifier was designed to operate under ZVS operation at switching frequency $f = 2\ \mathrm{MHz}$, dc supply voltage $V_{DD} = 15\ \mathrm{V}$, load resistance $R = 50\ \Omega$, duty ratio $D = 0.5$, and the loaded-quality factor of output L-C-R band-pass filter $Q = 5$.

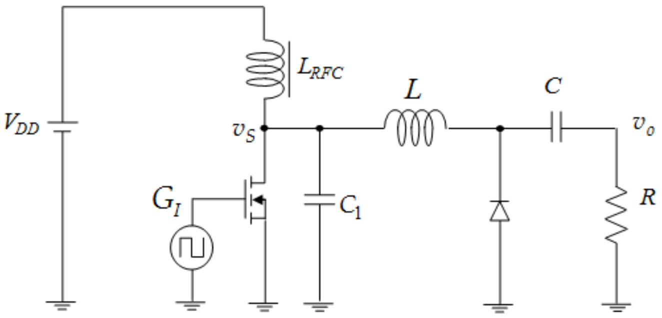

Fig. 3. Conventional diode clamp circuit [10].

The circuit components are derived in [1] and are given by the following equations:

$$P = \frac{8}{\pi^2+4}\frac{V_{DD}^2}{R} \tag{1}$$

$$C_1 = \frac{8}{\pi\left(\pi^2+4\right)}\frac{1}{\omega R} \tag{2}$$

$$L = \frac{RQ}{\omega} \tag{3}$$

and

$$C = \frac{1}{Q - \dfrac{\pi\left(\pi^2-4\right)}{16}}\frac{1}{\omega R} \tag{4}$$

where $\omega = 2\pi f$ is the angular frequency of the switching frequency f. Then, the circuit parameters are calculated to be as follows: $C_1 = 292\ \mathrm{pF}$, $C = 413\ \mathrm{pF}$, and $L = 20\ \mu\mathrm{F}$. If the class E amplifier is operated with the designed load resistance $R = 50\ \Omega$, the peak switch voltage is approximately 52.5 V. Namely, it is approximately 3.5 times higher than the dc supply voltage V_{DD}. On the other hand, the peak switch voltage changes with load variations. The steady-state value of the peak switch voltage was calculated in [11] when the load resistance stayed away from the designed value. In [11], the peak switch voltage is higher than the designed value when the load resistance is lower than designed value. And the peak switch voltage is lower than that of the designed value when the load resistance is higher than the designed value.

However, in some applications, e.g. in the plasma generation, the load resistance suddenly changes to much higher than the design value, even to be open-circuited, which results in high peak switch voltage. In particular, it also causes extremely high transient peak switch voltage. Both the high peak switch voltage and extremely high peak switch voltage bring about the damage of the switching devices. Hence, one remedy for this problem is reducing the equivalent load impedance by short circuiting the load resistance by a diode. Fig. 3 shows a conventional diode clamp circuit invented by MKS [5].

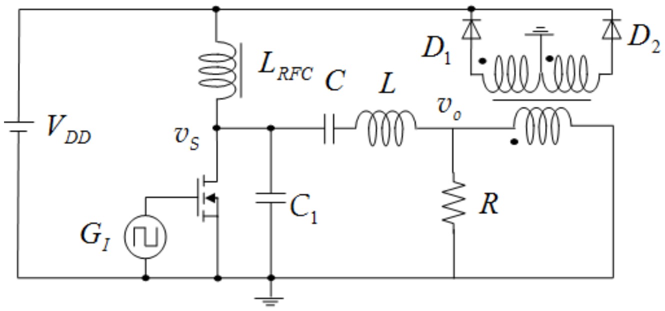

Fig. 4. Single power supply configuration of diode clamp circuit for class E amplifier using transformer.

In this circuit, the diode turns on when the voltage across C-R circuit drops below ground level. Then, the equivalent load resistance is reduced and the peak switch voltage is also reduced. However, there is a problem in this circuit. The dc bias of the voltage across the load resistance can move to a higher voltage when the load resistance is open-circuited. Then, the voltage waveform is not clamped by the diode.

3. Clamping of Switch Peak Voltage with Diode and Transformer

In this paper, we propose a modification of this circuit. Fig. 4 shows the proposed diode clamped class E amplifier. Two diodes, transformer, and dc voltage source V_{DD}, connected to the load resistance R, form a voltage limiter. The dc supply voltage source V_{DD} of the class E amplifier is used as one of the dc voltage source of the voltage limiter. The output voltage of the class E amplifier in the range $-V_{DD} \le v_o \le V_{DD}$. In this circuit, even if the bias of the output voltage waveform moves to a higher or lower voltage, two diodes clamp the output voltage waveform. Hence, the output voltage is successfully clamped and the equivalent output impedance is reduced. In addition, because of the application of the transformer, the circuit requires only one dc supply, which can decrease the circuit scale.

The effect of diode clamping is estimated by deriving an expression for the equivalent load resistance when the output voltage is clamped. Fig. 5 shows a typical clamped voltage waveform. In this analysis, it is assumed that the output current is a pure sinusoid and can be described as

$$i_o = I_m \sin\left(\omega t + \varphi\right) \tag{5}$$

If the clamp diode is not present, it is assumed that the output voltage is sinusoidal and can be described as

$$v_O = V_m \sin\left(\omega t + \varphi\right) = RI_m \sin\left(\omega t + \varphi\right) \tag{6}$$

The actual output voltage is clamped by the diode when $\left|v_O\right| > V_{DD}$. Therefore, the output voltage waveform is described as

$$v_O = \begin{cases} V_m \sin\left(\omega t + \varphi\right) & \text{when} \begin{cases} -\dfrac{\varphi}{\omega} < t < t_1 \\ t_2 < t < t_1 + \dfrac{\pi}{\omega} \\ t_2 + \dfrac{\pi}{\omega} < t < \dfrac{2\pi}{\omega} - \dfrac{\varphi}{\omega} \end{cases} \\ V_{DD} & \text{when} \begin{cases} t_1 < t < t_2 \\ t_1 + \dfrac{\pi}{\omega} < t < t_2 + \dfrac{\pi}{\omega} \end{cases} \end{cases} \tag{7}$$

where

$$t_1 = \frac{\sin^{-1}\dfrac{V_{DD}}{V_m} - \varphi}{\omega} \tag{8}$$

and

$$t_2 = \frac{\pi - \sin^{-1}\dfrac{V_{DD}}{V_m} - \varphi}{\omega} \tag{9}$$

Then, the equivalent load resistance can be obtained using Fourier analysis to find the fundamental frequency component

$$R_{eq} I_m = \frac{2}{T} \int_0^T v_o \sin\left(\omega t + \varphi\right) dt \tag{10}$$

where R_{eq} is the equivalent load resistance and $T = 2\pi / \omega$. Expanding and rearranging (10), R_{eq} is obtained as

$$\begin{aligned} R_{eq} &= \frac{2}{TI_m} \int_0^T v_O\left(t\right) \sin\left(\omega t + \varphi\right) dt \\ &= \frac{2}{TI_m} \int_0^T v_O\left(t' - \frac{\varphi}{\omega}\right) \sin \omega t' dt' \\ &= \frac{4}{TI_m} \left[\begin{aligned} &\int_0^{t_1'} RI_m \sin^2 \omega t' dt' + \int_{t_1'}^{t_2'} V_{DD} \sin \omega t' dt' \\ &+ \int_{t_2'}^{T/2} R_0 I_m \sin^2 \omega t' dt' \end{aligned} \right] \\ &= \frac{2R_0}{\pi} \left[\sin^{-1}\frac{V_{DD}}{V_m} + \frac{V_{DD}}{V_m} \sqrt{1 - \left(\frac{V_{DD}}{V_m}\right)^2} \right] \end{aligned} \tag{11}$$

where

$$t' = t + \frac{\varphi}{\omega} \tag{12}$$

$$t_1' = \frac{\sin^{-1}\dfrac{V_{DD}}{V_m}}{\omega} \tag{13}$$

$$t_2' = \frac{\pi - \sin^{-1}\dfrac{V_{DD}}{V_m}}{\omega} \tag{14}$$

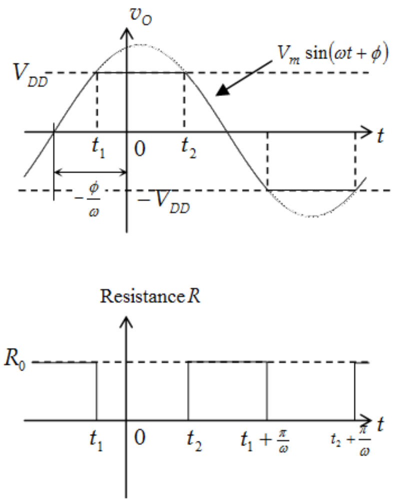

Fig. 5. (a) Clamped output voltage waveform and (b) transition of load resistance.

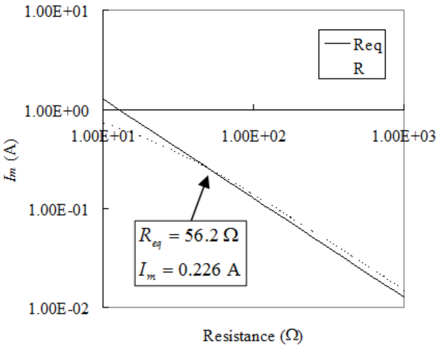

Fig. 6. Graphical determination of amplitude of output current I_m.

The equivalent reactance X_{eq} is obviously 0 because v_O is the even function.

Applying (11) to the circuit parameters described in Section 2, R_{eq} is plotted as a function of I_m as a solid line in Fig. 6. In this plot, it is assumed that $R = 500\ \text{k}\Omega$. On the other hand, in the operation of the class E amplifier, I_m varies with load resistance [2] because it is outside the designed condition. I_m versus R outside the design conditions as was obtained in [2]. Both functions $I_m - R_{eq}$ and $R - I_m$ are extremely complicated nonlinear functions. Hence, graphical method is one easy way to determine the operating point. Plotting I_m of [2] versus R in Fig. 6, we can find a intersection point of two plots $I_m - R_{eq}$ and $R - I_m$ This point is the operating point of I_m and R. In the example circuit, we can be obtain $R_{eq} = 56.2\ \Omega$, $I_m = 0.226\ \text{A}$.

The currents flowing through the clamp diodes are

$$i_{D1} = \begin{cases} I_m \sin(\omega t + \varphi) - \dfrac{nV_{DD}}{R} & \text{when } t_2 < t < t_1 \\ 0 & \text{otherwise} \end{cases} \tag{15}$$

$$i_{D2} = \begin{cases} I_m \sin(\omega t + \varphi) + \dfrac{nV_{DD}}{R} & \text{when } t_1 + \dfrac{T}{\omega} < t < t_2 + \dfrac{T}{\omega} \\ 0 & \text{otherwise} \end{cases} \tag{16}$$

where

$$n = \frac{L_1}{L_2} \tag{17}$$

Hence, the peak diode currents are

$$\max(i_{D1}) = \max(i_{D2}) = I_m - \frac{nV_{DD}}{R} \tag{18}$$

4. Simulation Results

Simulation was done at $f = 2\ \text{MHz}$, dc supply voltage $V_{DD} = 15\ \text{V}$, load resistance $R = 50\ \Omega$, and duty ratio $D = 0.5$ of the class E amplifier. The simulated circuit parameters were $C_1 = 210\ \text{pF}$, $C = 430\ \text{pF}$, $L = 18\ \mu\text{H}$, and $L_{RFC} = 175\ \mu\text{H}$. Spice model of power MOSFET IRF510 were used as switching devices and diode D1N4148 as clamping devices. Self inductances of transformer were $100\mu\text{H}$, $100\mu\text{H}$, and $200\mu\text{H}$. The gate port G_I was operated at 2 MHz and 4 Vp-p and -2 V offset rectangular signal. In addition, the load resistance is connected to a MOSFET which is driven by G_{II} as shown in Fig. 7. Therefore, the load resistance varied between $50\ \Omega$ and open circuit periodically at 10 kHz.

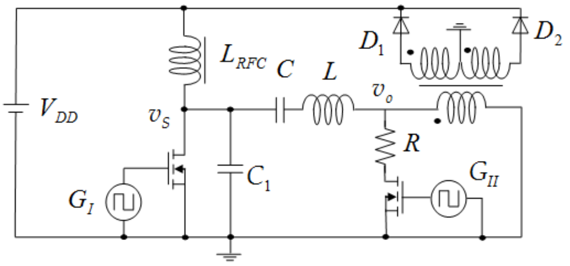

Fig. 7. Actual diode clamp circuit for simulation.

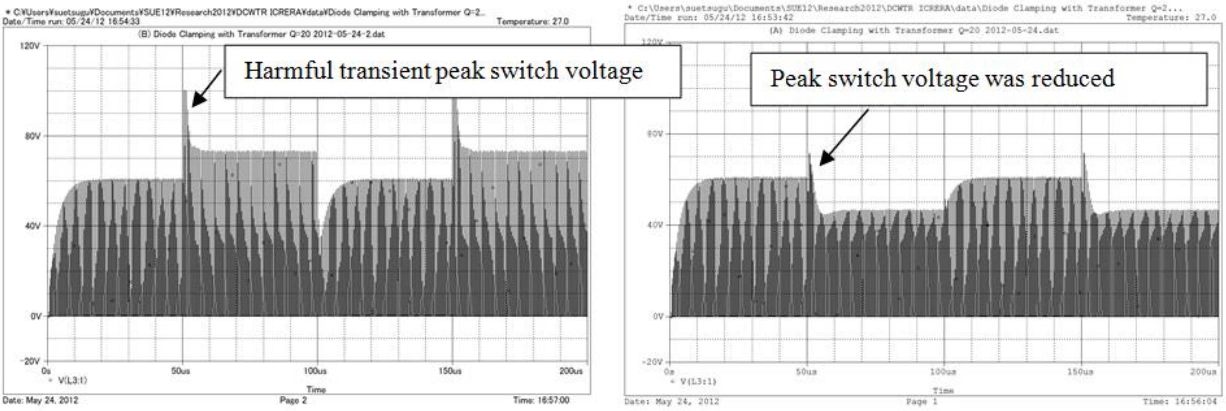

Fig. 8. Transient switch voltage waveforms of class E amplifier. (a) Basic class E amplifier of Fig. 1. (b) Proposed class E amplifier of Fig. 4.

Simulation waveforms are shown in Fig. 8. In the basic circuit of Fig. 1, the transient peak switch voltage was approximately 110 V (Fig. 3(a)). In the proposed circuit, transient peak switch voltage was reduced to 70 V (Fig. 8(b)).

Table 1. Comaprision of measured peak switch voltages

	Peak voltage in transient state	Peak voltage in steady state
Basic class E	110 V	73 V
Proposed class E	70 V	60 V

5. Conclusion

In this paper, a peak voltage clamp circuit was proposed. This circuit can reduce the peak transient voltage if the class E amplifier with diodes and transformers without consuming significant power loss. This clamping circuit excludes danger of destruction of switching device during operation of plasma load. In the simulation results, the proposed circuit reduced the transient spike of switch voltage at sudden cut off of load impedance by approximately 37%. Further, the peak switch voltage for open circuit load became lower than that of basic class E amplifier. This also reduces switching loss at open circuit load condition. And, it reduces danger of destruction of switching device due to heat by switching loss, too.

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