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Memristor Based Multi-State Shift Register Architecture

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ABSTRACT

Bio-inspiring circuit design attracts a great deal of attention among researchers in the field of electronics. Memristor has emerged not only because of their potential use in neuromorphic circuits but also because of their feasible fabrication using low-cost techniques. This research presents the use of memristors to build multi-state shift registers. Memristors are capable of storing and processing multi-state logic and design of an architecture for their use in shift register have potential applications in bio-inspired integrated circuits, telecommunication systems, cryptology, display technologies, data storage, chaotic circuits, etc. The designed shift register consists of stages with capability to store and transfer multiple bits. The number of stages can be adjusted depending on the requirements of the specific applications. Each stage of the shift register consists of two memristors for a continuous signal generation at the output of each stage. Reading and writing are executed in sequential order so that when reading operation is performed by a memristor, new data is transferred to another for writing. The amplitude of the voltage corresponds to the logic state and voltage levels are classified into logic states using comparators. For n-state logic, 2n-1 comparators are required at each stage. Yakopcic's memristor model is used in the simulations conducted in LTSPICE. The multi-state shift register architecture provided in this research successfully stores and shifts the data in the desired logic state.

Keywords:
Memristor, Resistive Switching, Shift Register, Multi-state Logic, Integrated Circuits

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INTRODUCTION

Developments in nanofabrication and material technologies have a significant impact on the speed, power consumption, cost and stability of electronic systems. In recent years, memristors have been one of the most important junction points where nanomaterials and electronics met. In the 1970s, Chua put forward the idea that there must be a circuit element defining the relationship between flux and charge [1]. Memristor research remained in theory level until the first practical work done by Williams et al. in 2008 [2]. Since then, in the search for new generation electronic systems, memristors have drawn the attention of the industry.

An active memristive layer, mostly metal oxide, sandwiched by two metal electrodes forms a memristor [2,3]. At this point, the active material is deterministic to obtain the bow-tie I-V hysteresis from the electrical measurements. Since the fabrication of the first memristor by Williams et al., TiO_2 represents one of the most worked out active materials in the literature [4]. The oxygen vacancies drift in TiO_2 thin films in the same direction with the current flow. Due to the drift of oxygen vacancies in the active layer, the resistance of the memristor (also known as memristance) varies as a function of the voltage applied across its terminals. The memristor stores the last resistance value on it even after the power source is disconnected. All these properties indicate the non-volatility and voltage-dependent resistance characteristics of memristors. Memristors have been subject to various studies including non-volatile resistive memory devices (ReRAM, NVRAM, etc.), bio-inspired and chaotic circuits [5-7]. Additionally, electrical properties of memristors resemble the synapses in the human body since the conduction through the memristor also depends on the strength of the signal passing through it. Artificial neural network applications and multistate data storage represent some of the futuristic properties of memristors. Conventional computation relies on the binary logic where all logical operations, as well as data storage, are done using 1s and 0s. In the case of multi-state (non-binary or multi-valued) logic as in analog and

quantum computer architectures, data is processed and stored in states not limited by 1 and 0. For instance, in a 3-state logic, 000, 001, 010, 011, 100, 101, 110, and 111 are used for logical operations and data storage. Multi-state data storage property of the memristors using crossbar array architectures has been subject to some studies in the literature [8-11].

Shift registers, commonly used in counter and memory devices, are composed of a number of flip-flops, which has been one of the essential components used for data storage in conventional binary logic systems. Shift registers scroll the binary data in a specific direction and the number of the bits stored in the shift registers is the same as the number of the flip flops used in the system. Prior to the development of modern memory architectures, shift registers were used as the primary memory structures in computation. Currently, the applications of the shift registers can be found in displays, communication systems, parallel and serial interface conversion and filters [12]. Unlike conventional shift registers using the Boolean systems, memristor-based shift registers can handle multi-state register operations. With the increasing demand on the research of memristor-based computation, the design of a multi-state shift register architecture becomes a necessity for modern data registers, noble communication protocols, and analog computation systems [8-11].

Several research groups elaborated Memristor-based logic gates. Memristor-based material implication (IMPLY) [13], memristor threshold logic [14], memristor-aided logic (MAGIC) [15] and memristors-as-drivers (MAD) [16] represent some of the proposed configurations in the literature executing logic operations using memristors. Likewise research on memristor-based logic gates, there are some memristor-based shift register studies in the literature counting on the single-bit logic [17, 18]. In addition to studies covering single bit operations, memristors have also been investigated in the literature to demonstrate their multi-state data storage capability in ReRAM architecture for multithreaded processors [8]. Due to the non-volatility of memristors, ReRAM can store multistate data even when the power is off. Low power consumption is another advantage of memristor-based memory systems since the power is not supposed to be on all the time. Furthermore, memristors potentially occupy less space in the circuit layout since multiple bits can be stored in a single memristor, rather than sparing a different cell for each bit as in conventional RAM architectures. This study provides an architecture for multi-state shift registers enabling the sequential scrolling of multistate data. Rather than using flip-flops or latches as in binary shift registers, the design, demonstrated herein, shifts the multi-state logic signals from one memristor to another. For validation of the designed architecture, simulations are performed for 4-state shift register operations. Jakopcic's memristor model is utilized in the simulations while designing a universal shift register relying on the multistate data storage ability of memristors as the primary objective of this research, various memristor models are evaluated throughout the design to extract writing and reading parameters resembling the real device.

BACKGROUND

R_M, the resistance of the memristor (also known as memristance), defines the relation between charge (q) and magnetic flux (ϕ) as given in Eq. 1 [1,2].

$$R_M = \frac{d\varphi}{dq} \tag{1}$$

where $\frac{d\varphi}{dt} = v(t) and \frac{dq}{dt} = i(t)$. Therefore the voltage $(v(t))$ across the terminals of a memristor is given by Eq. 2

$$v(t) = i(t).R_M(x) \tag{2}$$

R_M is the resistance of the memristor and $i(t)$ represents the current value. Williams et al. proposed a linear model to express the change in the resistance depending on the ionic drift in the active layer of the memristor [2]. Accordingly, the resistance of the memristor (R_M) is expressed by Eq. 3.

$$R_M(x) = R_{ON}x + R_{OFF}(1-x) \tag{3}$$

Here x is the state variable and given as $x = \frac{w}{D}$, where w is the width of the region with oxygen vacancies (doped region) and D is the total length of the memristor. The state variable value ranges between 0 and 1. R_{ON} and R_{OFF} refer to the maximum and minimum resistances obtained depending on the voltage applied. In a binary logic system, R_{ON} and R_{OFF} correspond to logic 1 and 0 respectively. The shift register architecture given in this research is designed for a memristor with R_{ON} and R_{OFF} values of $120\,\Omega$ and $1.1k\,\Omega$, respectively. In the later studies, several non-linear ionic drift models were worked out to completely define the memristive characteristics of materials. Most of these models were successful at physical boundary conditions of the device, but Pickett's model relying on Simmons tunneling barrier model provides a more realistic approach to the time domain operations [19]. Mathematical expressions are complex and there are a variety of parameters that needs to be determined experimentally. There are some alternative methods proposed due to the complexity of this model. Among these, the device models proposed by Yakopcic et al. [20] and Kvatinsky et al. [21] (threshold adaptive memristor model (TEAM)) may be the most preferred ones due to the less complexity for simulations.

As mentioned before, this study utilizes Yakopcic's model to simulate working conditions of memristors. According to the model, the motion of state variable is given by Eq. 4 [20].

$$\frac{d(x)}{d(t)} = \eta g(V(t)) f(x(t)) \tag{4}$$

η represents the direction of the motion, $g(V(t))$ defines the threshold to change the state variable, and $f(x(t))$ describes the points (x_n and x_p) at which the state variable do not change. Eq. 5 expresses $g(V(t))$ for possible conditions of $V(t)$

$$g(V(t)) = \begin{cases} A_p\left(e^{V(t)} - e^{V_p}\right), if\ V(t) > V_p \\ -A_n\left(e^{-V(t)} - e^{V_n}\right), if\ V(t) < -V_n \\ 0, if\ -V_n \le V(t) \le V_p \end{cases} \tag{5}$$

Here, V_p and V_n stands for the positive and negative threshold voltages, respectively, whereas A_p and A_n are the multipliers used to adjust how fast state variable changes. $f(x(t))$ is given by Eq. 6.

$$f(x(t)) = \begin{cases} \begin{cases} e^{-\alpha_p (x - x_p) w_p (x, x_p)} & \text{, if } x \ge x_p \\ 1, \ if\ x < x_p \end{cases} \\ \begin{cases} e^{\alpha_n (x + x_n - 1) w_n (x, x_n)} & \text{, if } x \le 1 - x_n \\ 1, \ if\ x > 1 - x_n \end{cases} \end{cases} \tag{6}$$

Window functions for positive and negative regimes are respectively given as w_p and w_n. α_p and α_n are the parameters defining the constraining factors in the motion of the state variable. Eventually, current change as a function of state variable (x(t)) and applied voltage (V(t)) can be expressed by hyperbolic functions (Eq. 7).

$$f(x) = \begin{cases} a_1 x(t) sinh(bV(t)), \ V(t) \ge 0 \\ a_2 x(t) sinh(bV(t)), \ V(t) < 0 \end{cases} \tag{7}$$

a_1, a_2, and b are the fitting parameters depending on the design and structure of the memristor. For the simulations conducted in this work, the fitting parameters are taken as a_1=a_2=0.17, b=0.05, η =1, A_n =A_p =4000, V_n=0.56, V_p=0.65, α_n=5, α_p=1, x_0 =0.11 (initial value of the state variable), x_n =0.5 and x_p =0.3. Shift registers are classified under sequential circuits where circuits work with the clock pulses. The device model and parameters must coincide with the practical working conditions of the modern memory devices and electronics systems to ensure the implementation of the proposed architecture for contemporary technologies.

METHODOLOGY

Writing Operation

In a binary logic system, if R_M approaches to the minimum resistance value of the memristor (R_{ON}), the memristor is set to logic 1. $R_M = R_{ON}$ condition is satisfied when the state variable (x) is 1. On the contrary, if R_M is close to the maximum resistance value of the memristor (R_{OFF}), the memristor is set to logic 0. Fig. 1 demonstrates the voltage, current and resistance waveforms obtained throughout the writing operation at which the resistance changes with the applied voltage. The graphs are plotted by using Yakopcic's model for the memristor. As mentioned before, using Yakopcic's model simplifies the mathematical load of the simulation. It is important to note that the writing process must not consume massive time to ensure that the design is compatible with clocking trend of modern memory devices and electronic systems. The speed of the writing process is determined by several parameters including the applied voltage, mobility of the ions in the active layer, maximum and minimum resistances of the memristor [20,22]. The proposed circuit model works at ±1.8V. As +1.8V is applied for 200 μs, the state variable increases from 0 to 1, meaning that logic state also switches from 0 to 1. On the contrary, when the voltage source is reverse biased with -1.8V, the state variable decreases in the reverse direction within about 200 μs. Consequently, reverse polarities of the applied voltage drive opposite logic conditions. To make the memristor working as a multi-state logic and memory device, knowing the precise values of the state variable are critical. For example, in a 4-state logic device, the ranges of x between 0-0.25, 0.26-0.5, 0.51-0.75, and 0.76-1 refer to 00, 01, 10, and 11 in a 2-bit complimentary system. As given in Figure 2, the x value changes in a logarithmic fashion and 00, 01, 10, and 11 logic states are respectively obtained within 12 μs (for 125mV), 30 μs (for 375mV), 72 μs (for 625mV) and 180 μs (for 880mV) when +1.8V applied. If the initial state is known, switching one state to another is possible by applying voltage for specific times. However, the initial state (or resistance) of the memristor may not be known before the writing operation, therefore it is crucial to design an automated writing circuit which accurately works no matter what the initial state (resistance) is. In the proposed design, for a reliable writing operation, the memristor state variable is first set to 0 or 1 by applying a constant voltage of -1.8V or +1.8V for 200 μs. Via this technique, without knowing its initial state, the memristor can be set to any value of the state variable by applying negative voltage (e.g. -1.8V for a certain time interval) after preconditioning at +1.8V. There are two convenient ways to set the desired value of the state variable: (1) applying varying voltage values for a certain time,

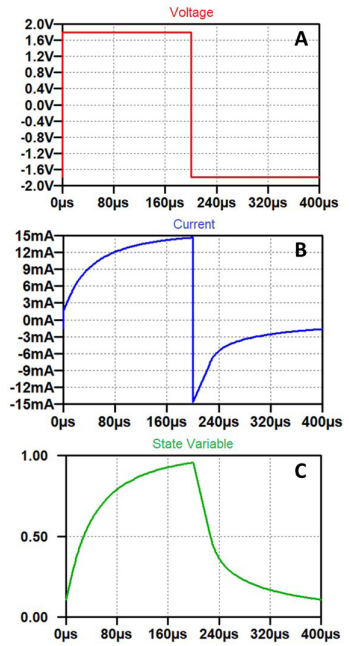

Figure 1. A) Voltage applied across the terminals of the memristor for 400 μs (+1.8V for 200 μs, -1.8V for 200 μs), B) Current change recorded over the memristor, C) Variations at the state variable (x) during the writing process.

(2) applying a constant voltage of -1.8V for varying time periods. As an example of the first case, applying -1.8V and -1.2V for a constant time of 30 μs yields different state variables. In the second case, the state variables are at different values when a constant voltage of -1.8V is applied for 20 μs and 30 μs. The universal shift register design given in this study is capable of running both scenarios.

Reading Operation

The reading of the memristor state is done by applying the zero-net flux condition at which the applied voltage is in square waveform and maximum and minimum voltage values are at the same amplitude but in opposite directions [22]. The stored data on the memristor is not supposed to be affected adversely throughout the readout process. Fig. 2 shows the change at the resistance value of the memristor during the readout process based on the applied voltage. Before the readout process, the initial resistance value is 269 Ω and after applying +1.8V for 1 μs and sequentially -1.8V for 1 μs, the same resistance is observed. This indicates the readout condition does not change the resistance and so the state variable of the memristor, if the zero-net flux condition is satisfied. Reading the state of the memristor can be done via operational amplifier based current or voltage reading process [22, 23]. The readout circuit used in this design is given in Section 4. Simply, the amplified voltage amplitude at the output of the opamp corresponds to a state variable. The maximum absolute voltage value must be normalized to the state variable 1, whereas the minimum absolute voltage must be also normalized to the state variable 0. As mentioned earlier, the voltage applied to the input of the opamp is in the form of a square wave, therefore the output voltage appears to be in the triangular waveform and root mean square (RMS) converter or an averaging circuit can be embedded to the system for the simplification in the quantization. An averaging circuit with the bypassing capacitor at the input is a feasible way for implementation. As compared to the writing operation, reading consumes less time, however, for the synchronization purpose, the period is taken the same as the writing process.

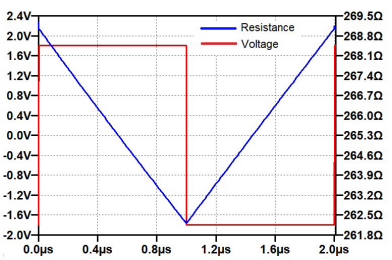

Figure 2. Resistance change during the reading operation (Applied voltage: +1.8V for 1 μs, -1.8V for 1 μs).

RESULTS AND DISCUSSION

The foremost principle that has to be considered at the design of the memristor-based multi-state shift register architecture is that reading and writing operations need to be performed in a sequence. Writing and reading cannot be done at the same time on a single memristor. The sequence can be achieved using two memristors in a stage. While the writing operation is in progress on a memristor, the reading operation is conducted in another one. Unlike the binary systems, one stage stores more than 1 bit. The sequential processes observed at the memristors

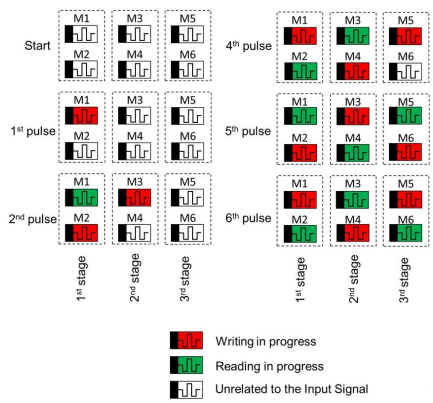

Figure 3. Representation of the initial reading and writing sequences for a three-stage multi-state shift register. Red-colored memristors represent the writing process in the particular memristor, whereas green colored ones indicate the reading process. Non-colored ones symbolize the memristors unrelated to the input signal (this condition is only observable in the initial pulses).

are illustrated in Fig. 3 for a three-stage shift register configuration. The first data package is written to the M1 at the first clock pulse. Here, the term "data package" is used to define random multi-state data. With the second clock pulse, the stored data at M1 is sent to the M3 at the second stage via read-out circuitry. While this read-out process is in progress on M1, the writing operation is performed on M2 for the second data package. The first data transferred to the M3 during the read-out process of M1. Sequentially, the writing at M4 of the second stage continues while the data stored at M3 can be observed at the output of the second stage. Proper clocking and switch connections are vital to achieving a sequential order for the writing and reading processes. At each clock pulse, the read line (RL) switch connected to one of the memristors must be on, whereas write line (WL) switch must be on for the other one. The shift register configuration given in this study is universal and the number of the stages can be extended to any desired level.

Fig. 4 shows the circuit diagram of a 2-stage memristor-based multi-state shift register. This circuit is specifically designed for a 2-bit operation in a single memristor. As discussed before, clock connections of the transmission gates that are used to establish the sequence in the reading and writing are connected with reverse polarities for the same memristor. To maintain a sequential order in the shift register, clock pulses of M1-M3 and M2-M4 must be paired. The input of the first stage is the writing signal for M1 and M2. The input signals are separated in equal time periods to separate the writing times for M1 and M2. When M1 is being written, the M2 is read out and vice versa. The readout connections shown in Figure 4A are connected to the circuitry shown in Fig. 4B. As illustrated in Fig. 4B, each stage has a single readout circuit at which the signal amplified using an opamp. Both inverting and non-inverting configurations can be used in the opamp. Signal transferred per clock pulse classified into voltage levels by using comparators after the amplification. Comparators connected to the decoders determine the logic carried out by the signal. The preferred option to convert the voltage to the state variable is to use a comparator configuration. By this method, the incoming signal from the readout circuit can be segmented into state variables according to the voltage levels. Likewise the comparator stage of the flash ADC architecture, comparators can be supplied by reference voltages determined by voltage divider configuration. Using a comparator, the voltage at the output of the readout opamp is compared with a reference voltage (V_{ref}). Simply, state variables between 0-0.25, 0.26-0.5, 0.51-0.75, and 0.76-1 are classified into logic 00, 01, 10, and 11. Three comparators are required for a 2-bit system because 0.25, 0.5 and 0.75 are supposed to determine the threshold for classification. For instance, in a 2-state readout operation, 0.2V at the output of the opamp refers to logic 00 because when it is compared with V_{ref} values of 0.25V, 0.5V and 0.75V and the output of the comparators give 0V. In case of 0.8V coming from the readout circuit, the outputs of all comparators are 1, so the logic corresponding to 0.8V is 11.

The working principle and combination of the comparators resemble the flash ADC configuration, but there is no encoder in this case. As the number of states increase, the number of comparators is supposed to be also increased. While three comparators are sufficient to conduct a 2-state operation, n-state operation requires 2^n-1 comparators.

After the logic state of the memristor is determined, the logic signal is carried to the input of the second stage. As seen in Fig. 4C, each logic state has a corresponding clock connection. In order to transfer the state of a memristor to another one, a voltage must be applied for a certain time interval at the writing circuit. For instance, in order to write logic 11 to M3, CLK_11 is used and the naming of clock inputs is done according to the logic state they should write. As mentioned earlier in the text, altered voltage values can be used instead of varying clocking. Fig. 5 shows the random input (V(in)) and its corresponding outputs of a 5-stage two-state shift register. As seen in the V(in) graph, the voltage value varies while the duty cycle is kept constant. It is important to note that the first output voltage is the signal directly written by the voltage coming from the input. So V(out1) is recorded before it's classified into logic states. For example, the voltage value between 400 μ s and 800 μ s is at around 200mV and since it is lower than 250mV (the boundary between 00 and 01), the corresponding input signal is classified as logic 00. When V(out1) between 1.2ms and

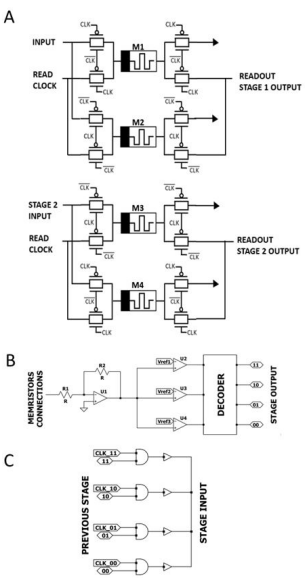

Figure 4. A) Circuit architecture of a two-stage multistate shift register. B) Readout circuitry connected to the outputs of each stage. C) Writing circuitry using voltage or time-varying pulses represented with CLK_00, CLK_01, CLK_10, and CLK_11.

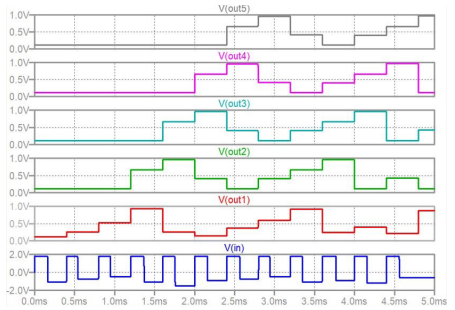

Figure 5. Simulation results demonstrating random 2-state logic shifting in a five-stage shift register. V(in) graph shows the varying applied voltage in a constant clock cycle. V(out1) is the signal observed before the voltage segmentation process in the comparators are completed. V(out2), V(out3), V(out4), and V(out5) are shifted outputs observed in sequential stages. The output voltages are normalized to represent the state variable values.

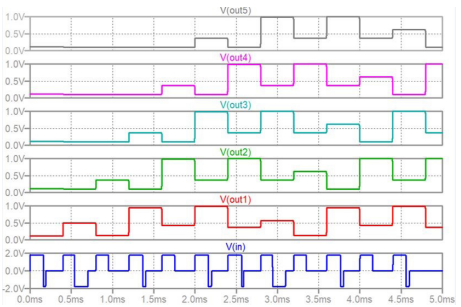

Figure 6. Simulation results demonstrating random 2-state logic shifting in a five- stage shift register. V(in) graph shows the varying duty cycles for the constant applied voltage. V(out1) exhibits the signal waveform observed before the voltage segmentation process in the comparators are completed. V(out2), V(out3), V(out4), and V(out5) are shifted waveforms observed in sequential stages. The output voltages are normalized to represent the state variable values.

1.6ms is checked, it can be seen that the voltage value in that time interval is 900mV and since this value is greater than 750mV (the boundary between 10 and 11), the corresponding input voltage is classified as logic 11. V(out2), V(out3), V(out4) and V(out5) represent the outputs of each state and the graphs demonstrate the shift registering of the V(out1) in sequential order. All output voltage values are normalized to correlate them with the state variable (x). After the readout process at the circuit seen in Fig. 4B, output signals are classified according to the voltage levels. According to the input and the output graphs, the design works properly for the 2-state shift register. Fig. 6 is plotted to exemplify the condition at which V(in) is maintained at a constant voltage and time for pulsing -1.8V varies. Consequently, 2-state memristor-based shift register behavior is successfully observed for a different writing scenario. The state variables are subject to changes depending on the duration of the applied voltage. For some applications, it may be more preferred to vary the duration rather than the voltage and the proposed architecture can be utilized for both scenarios.

CONCLUSION

Memristor-based logic and data storage systems have the potential to be implemented in advanced electronic devices not as an alternative method, but as a fundamental building block. As an architectural model for a multi-state shift register, the designed memristor-based circuit works with high accuracy. Yakopcic's memristor model is utilized in the simulations due to its accuracy and applicability. Each stage of the shift register has two memristors so that when one is being written the other one is being read. Reading and writing scenarios are designed for the flow of the data in sequential order. A pre-conditioning technique is applied during the writing process to operate the memristor accurately without knowing its initial state. Writing process using both altered clock and voltage values are achieved with the architecture given in the study. The use of memristors in shift-registers to control the clock-based flow of the data represents a crucial task in memristor-based computing and communication systems for future applications. The architecture and the circuit design covered in this study have the potential to be utilized in analog and multi-bit digital computations, as well as chaotic and neuromorphic circuits.

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