Hittite Journal of Science and Engineering, 2018, 5 (1) 25-29
ISSN NUMBER: 2148-4171
DOI: 10.17350/HJSE19030000074

A New Demodulator For Inverse Pulse Position Modulation Technique

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ABSTRACT

Inverse pulse position modulation is one of the modulation techniques for Visible Light Communication (VLC) systems. In this paper, a new demodulator scheme, which is named as Slot Period Detector (SPD), is proposed by using frequency detection technique. The proposed architecture computes the period time for each slot. Thanks to SPD technique, the complexity of I-PPM receiver is dramatically reduced. However, the traditional receiver has better Bit Error Rate (BER) performance than that of proposed SPD structure. The important issue is that whether the proposed receiver is practicable for real-time systems hence, the SPD is implemented on Field Programmable Gate Arrays (FPGA) board to demonstrate an applicable receiver.

Article History:
Received: 2017/05/05
Accepted: 2017/09/30
Online: 2018/03/28

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Keywords:
I-PPM, Demodulator, Visible light communication

INTRODUCTION

To provide data transmission in indoor communication systems, Visible Light Communication (VLC) is a promising technique which uses Light Emitted Diode technology. On the contrary wireless RF communication systems, VLC systems are generally operated at short distance due to light power of LED. However, VLC can serve with different systems since VLC doesn't affect any electromagnetic interference compared with RF communication systems. The receiver side uses a photodiode to obtain electrical signal from light energy. Therefore, the line of sight is very important issue for VLC systems.

In order to achieve data transmission in the VLC systems, pulse based modulation techniques were proposed in the literature. The On-Off Keying (OOK) is the simplest modulation method in the communication systems. Another modulation technique is the Pulse Position Modulation (PPM) scheme. The PPM scheme has very advantage with respect of BER performance, complexity and bandwidth efficiency. A new PPM scheme, which is named as Variable Pulse Position Modulation (VPPM), was proposed to control brightness of LED by using variable pulse width technique [1]. I-PPM that is one of the PPM types was proposed in [2]. This modulation method was improved by inversing the traditional PPM technique. Therefore, I-PPM scheme consumes further energy compared with traditional PPM technique.

In [3], the overlapping PPM (OPPM) that is integrated with trellis coded modulation was compared with I-PPM and PPM techniques with respect of data transmission rate. That study is theoretically analyzed to performance of modulation schemes. However, a few papers focused on practical design for implementation of PPM technique. The dimming level is very important issue in the V-PPM (Variable-PPM) scheme. A VPPM transmitter architecture was proposed to reduce resource utilization of VPPM technique for adjustable dimming level [4]. A VPPM demodulator scheme was designed without knowledge dimming level. The proposed architecture was implemented on real-time FPGA board [5]. The demodulator was improved to provide a rapid dimming environment in the paper [6]. The target dimming level is determined by step-step to accomplish synchronization hence target dimming level can't be suddenly obtained. In this paper, we propose a new PPM demodulator architecture to reduce complexity of traditional PPM receiver. The proposed scheme is based on period detector. The empty slot is determined by using a slot period detector. Additionally, the demodulator is implemented on real-time FPGA board. The advantages of proposed receiver are explained as follows:

1. In traditional receiver, the signal generator is used to multiply received signal. Hence, the signal generator must be designed for traditional receiver. However, the proposed architecture doesn't consist of signal generator block.
2. In order to determine empty slot, decision block must use the output values of integrators. The input values of integrators are obtained at the output of multipliers' blocks. The multiplier block must be operated at the traditional receiver side. There isn't any multiplication unit in the proposed receiver.

I-PPM TECHNIQUE

This section gives the traditional I-PPM transmitter and receiver schemes. I-PPM signal is obtained by changing position of empty slot. The empty slot is situated on appropriate locate considering to data bits' condition. In order to generate I-PPM signal, one of the most widely used modulator structures is mux-based techniques because mux-based architectures operates using codeword table. In this scheme, the code that matches with the value of data bit is activated at the output of modulator structure. If i can be expressed as the decimal equivalent of data bit, an explanation of I-PPM technique can be written as

$$IPPM_i(t) = \begin{pmatrix} 0 & for\, t \in \left[\frac{i}{2^n}T_b, \frac{i+1}{2^n}T_b\right] \\ V & elsewhere \end{pmatrix} \quad (1)$$

where, T_b and n represent one symbol period and bit number in one symbol, respectively. The i value signifies decimal equivalent of data bit. As shown in the Fig. 1, the location of empty slot is determined by using decimal equivalent of data bit.

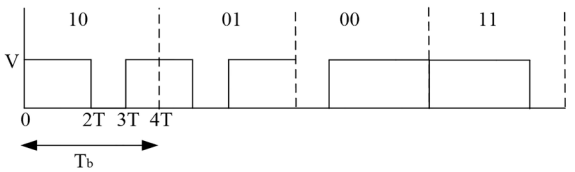


Figure 1. I-PPM signal

In Fig. 2-a, it is shown that traditional I-PPM receiver. As shown in the figure, multiplier and integrator blocks are used to provide correlator-based receiver system. Moreover, signal generator blocks, which are presented as SG-1, SG-2, SG-3 and SG-4, are used to multiply received modulated signal with carrier signal. Firstly, modulated signal is multiplied by carrier signal. Then, the output of multiplication is applied on integrator block which accumulates to received signal through one symbol period. Fig. 2-b gives an example of signal generator architecture. The counter block is used as common block for all SG blocks. The Th-2 and Th-3 are presented as 2T and 3T in Fig. 1, respectively. For interval between 2T and 3T, the algorithm provides that output is being '0'.

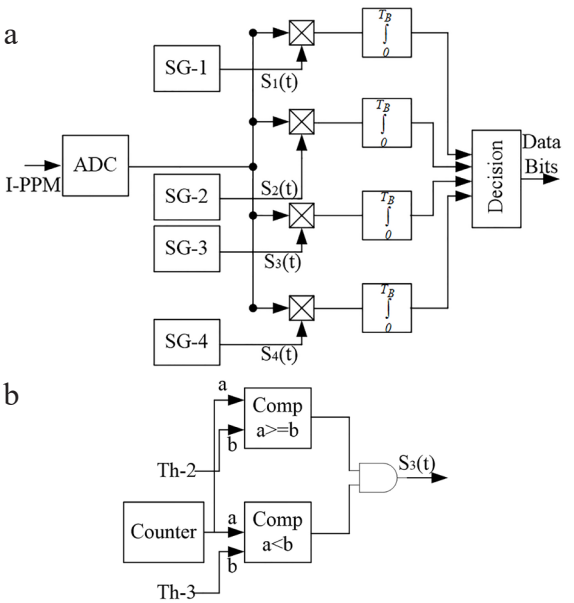


Figure 2. The I-PPM receiver, a. The traditional I-PPM receiver, b. The signal generator architecture.

PROPOSED SLOT PERIOD DETECTOR SCHEME

In this section, we present the proposed demodulator architecture which is referred to as slot period detector (SPD). We count high frequency pulse when amplitude of modulated signal is lower than that of the threshold value which is equal to V/2. The Fig. 3 emphasizes to this situation. As shown in the Fig. 3, empty slot is filled by high frequency pulses because high frequency pulses and the output of comparator block are passed through AND gate. If the amplitude of I-PPM signal is higher than V/2, one of input signals of AND gate is being '1'. This input signal is the output of comparator block. Therefore, the output of AND gate is obtained a square wave. The proposed receiver can be expressed as follows:

$$e = \begin{pmatrix} 0 & for\, IPPM => Th \\ 1 & for\, IPPM < Th \end{pmatrix} \quad (2)$$

$$C_k = \sum_{i=1}^{T/4} e_i \quad (3)$$

where, Th and e present threshold value and output of comp (comparator) as shown in Fig. 4. For k ∈ {1, 2, 3, 4}, the output of the counter is presented as Ck. The one symbol period is expressed as T. As shown in the Eq. (2) and (3), the counter computes binary '1' level time during

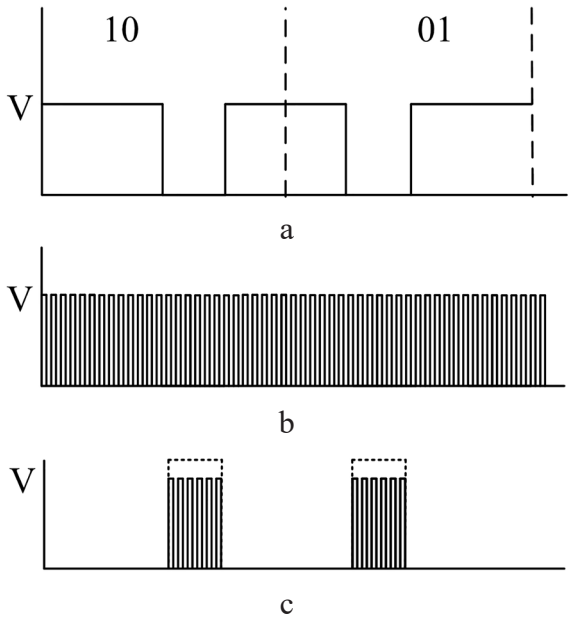


Figure 3. I-PPM demodulation process. (a) I-PPM signal according to data bits. (b) High frequency pulses. (c) AND gate output

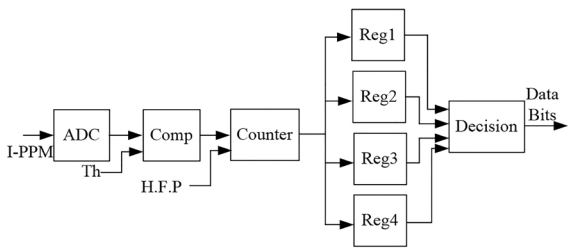


Figure 4. Proposed I-PPM Structure

quarter symbol period. Our aim is to find the maximum Ck among C1, C2, C3 and C4.

In experimental application, the optical I-PPM signal is converted to electrical I-PPM signal by using a photodetector. The electrical I-PPM signal is received by ADC (Analog to Digital Converter). The received modulated signal is compared with a threshold value (Th). This stage determines the structure of received I-PPM signal. The output of comparator block (Comp) acts as an enable signal for counter block. The clock signal of counter block is H.F.P (High Frequency Pulse) hence the output of counter increases when en and H.F.P. is logical '1'. Register (Reg) blocks are used to hold sum value of counter block during quarter symbol period. The decision block determines data bits according to output of register blocks. The filled slot given in the Fig. 3.a is determined by decision block.

SIMULATION AND EXPERIMENTAL RESULTS

In this section, we give simulation and experimental results for proposed demodulator architecture. From experimental and simulation results, we show that proposed serial scheme is suitable for demodulation of I-PPM signal.

The Fig. 5 and Fig. 6 give simulation results of proposed receiver. In the Fig. 5, H.F.P signal is represented as high frequency pulse. The *data*, *g.data* and *d.data* are defined as input data, grouped data and detected data, respectively. The *data* signal is applied on input of I-PPM modulator. In order to generate I-PPM signal, data signal is grouped by two bits because the one symbol consists of two bits. In output of our receiver, the *d.data* is obtained at the output of decision block. The modulated I-PPM signal is successfully demodulated at the receiver side because it is shown from the Fig. 5 that the data and *d.data* bits are same. The *e* signal is generated by comparator block. According to comparison result of I-PPM signal with threshold value, the *e* signal gets '1' or '0'. If threshold value is greater than I-PPM signal, the *e* signal will be '1'; otherwise the *e* signal becomes logic '0'. In the Fig.6, simulation results illustrate BER performance of the traditional (T.D.) and proposed (P.D.) demodulator.

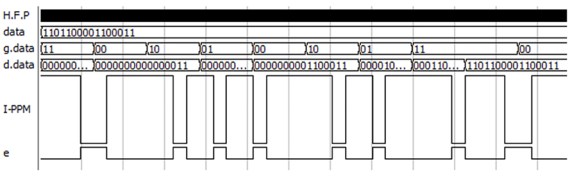


Figure 5. Simulation results of the proposed SPD.

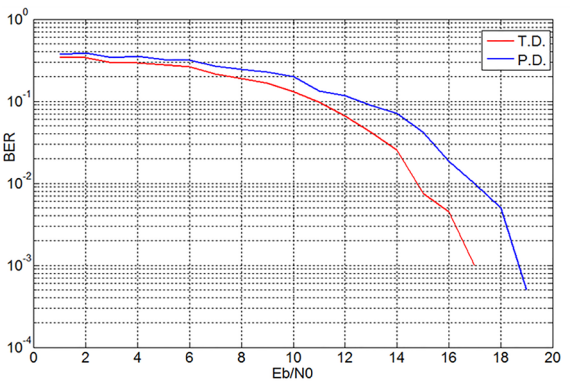


Figure 6. BER performance of the receiver architectures.

As shown in the figure, traditional demodulator has better BER performance than that of proposed demodulator. This is because that the location of empty slot is determined by correlation based receiver.

The Fig. 7 gives the receiver architecture implemented on FPGA board. We obtain experimental results by oscilloscope. Firstly, we designed modulator and demodulator by using FPGA complier. The designed demodulator is shown in the Fig. 7. Then, we operated on real-time FPGA and observed experimental results on output of the oscilloscope. In Fig. 8 and Fig. 9, we give

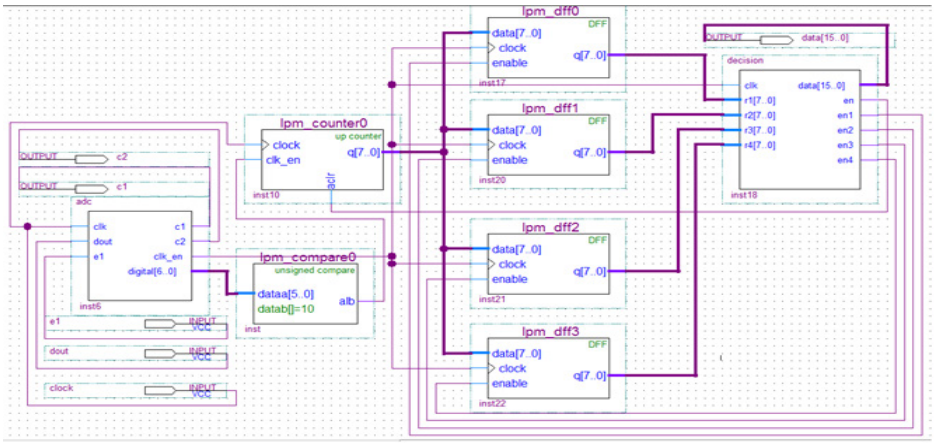


Figure 7. The receiver scheme implemented on FPGA board.

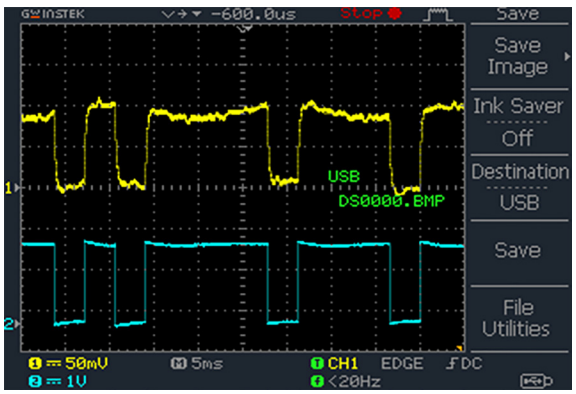


Figure 8. Modulated (blue line) and received (yellow line) signals for low frequency.

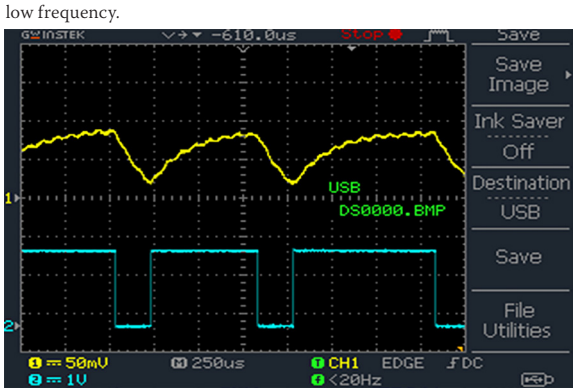


Figure 9. Modulated (blue line) and received (yellow line) signals for higher frequency.

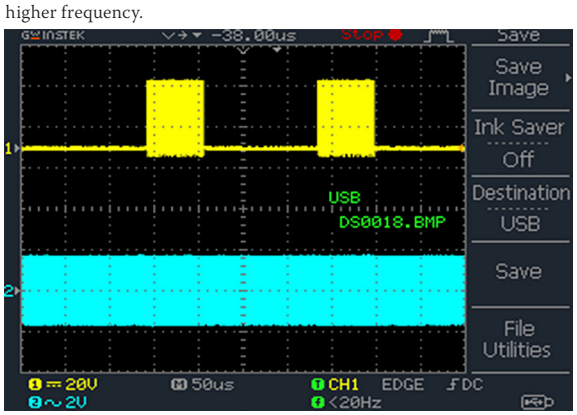
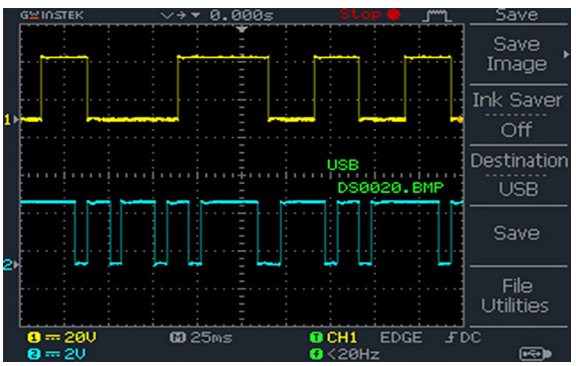


Figure 10. H.F.P (blue line) and clock signal of counter (yellow line).

a



b

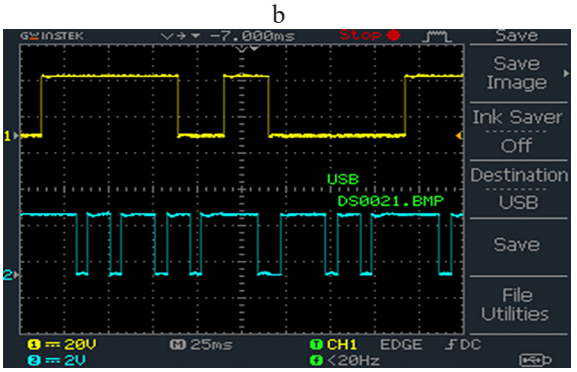


Figure 11. Modulated signals according to data bits. (a) LSB (Yellow Line) and I-PPM (Blue Line) signal. (b) MSB (Yellow Line) and I-PPM (Blue Line) signal.

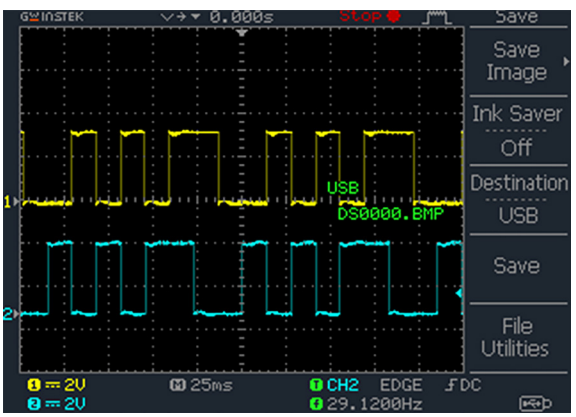


Figure 12. Transmitted (blue line) and received (yellow line) data bits.

modulated signal (blue line) and received signal (yellow line).

In Fig. 8 and Fig. 9, data rate is different hence received signal with higher frequency has further distortion than that of received signal with lower frequency. Fig. 10 shows H.F.P signal (blue line) and clock signal (yellow line) of counter block. The output of counter is increased depending on yellow line signal.

In Fig. 11, we give modulated signal according to data bits. The Fig. 11 (a) illustrates LSB (Least Significant Bit) bit and modulated signal while MSB (Most Significant Bit) and I-PPM signal are shown in Fig. 11 (b).

The Fig. 12 shows received (yellow line) and transmitted (blue line) bits. As shown the figure, transmitted bits are successfully estimated at receiver side.

CONCLUSION

In this paper, we propose a new receiver to demodulate I-PPM signals. The proposed architecture, which is referred to as Slot Period Detector (SPD), has lower complexity structure than that of the traditional scheme. However, the traditional scheme gives further BER performance compared with proposed structure. It can be shown the difference between the traditional and proposed architectures from the Fig. 2 and the Fig. 4. The proposed scheme is applied on real-time FPGA board. From experimental and simulation results, we prove that the proposed architecture is suitable for visible light communication systems.

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