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# THE EFFECT OF THE SURFACE STATES ON THE CURRENT-VOLTAGE CHARACTERISTIC OF Au / a-Si:H / a-Si:H ($n^+$- type) /Cr SCHOTTKY DIODES

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ABSTRACT

In this study it was aimed to investigate the effect of surface states on the current-voltage characteristics of the Schottky diodes prepared by an r.f. magnetron suputtering technique. In order to fabricate Au / a-Si: H / a-SiH ($n^+$-type) structure $n^+$-type doped and intrincsic hydrogenated amorphous silicon films were deposited on glass substrate coated with chromium respectively. The rectifier gold metal contact was applied on the top of intrinsic layer under the vacuum of $1 \times 10^{-7}$ Torr. The current-voltage characteristics were measured with respect to time. The density of surface states $D_S$ were determined The change in the rectification ratio was explained by means of surface states.

## INTRODUCTION

In the device technology it is expected to fabricate the Schottky diodes in which their current-voltage characteristics do not change with time and their rectification ratio is large as much as possible. The surface states are the most restrictive parameters which prevent the Schottky diodes to have ideal characteristics. These effects of the surface states were first observed by Thanailakis in 1971. It was tried to bring a physical understanding by means of charge exchange between the slow oxide states and the semiconductor (Thanailakis 1972). The same problems were also noticed by Thompson (1981) and Singh (1983). But these workers could not give sound theoretical explanations to their experimental curves to interprete the changes in current-voltage characteristics of the Schottky diodes. Masuyama (1983) and Serin et al (1987) gave some reasonable explanations for the current-voltage changes with annealing in the Schottky diodes prepared by means of amorphous silicon. They stated that these changes could be attributed to the surface states.

Here it was aimed to investigate the effect of surface states on the current–voltage characteristics of the Schottky diodes in the Au / a–Si: H / a–Si: H ($n^{\pm}$–type) / Cr sandwich structure prepared by means of r.f. magnetron sputtering technique. In order to realize this goal, the current–voltage characteristics were measured in dark and at different times.

## EXPERIMENT

The glass substrages cleaned in Trichlorethylene ($C_2HCl_3$) were coated with chromium metal under a vacuum of 1 x $10^{-7}$ Torr. In order to fabricate the structure of Au / a–Si: H / a–Si: H ($n^+$–type) / Cr highly $n^+$–type doped amorphous silicon (thickneess 400 nm) and hydrogenated amorphous silicon thin film (thickness 1000 nm) were deposited on the chromium metal. The deposition processes were maintained in Argon. During the deposition the pressure of gases, temperature of substrate and r.f. magnetron power were as follows; $Pp_{H_3}$ = 2 x $10^{-4}$ Torr., $p_{H2}$ = 5.4 x $10^{-4}$ Torr., $p_{tot}$ = 5.5 x $10^{-3}$ Torr., T = 550 K, $p_{rf}$ = 650 Watt. These were the optimum conditions for the production of a sample with ideal diode characteristics. The sample of dimensions 3mm x 3mm was stuck on the holder with Araldite. The gold sontact of area 7.8 x $10^{-3}$ $cm^2$ was applied to the amorphous films as shown in figure 1. The samples were kept in the sealed, evaculated and darkened glass tubes at a constant temperature of 20 °C in an oven. The measurements were carried out in the dark.

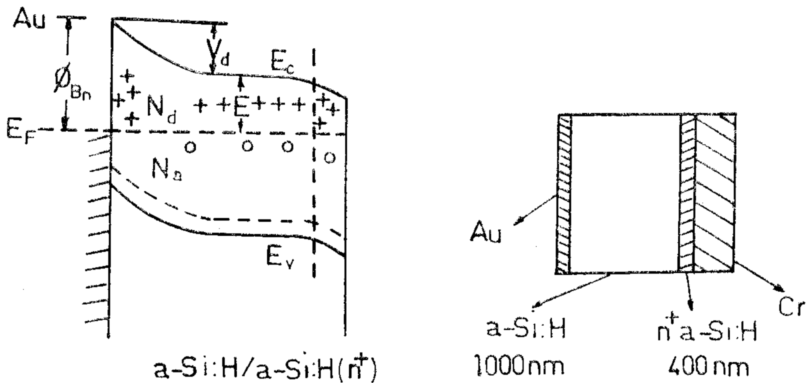


Figure 1. The structure of Au / a–Si: H / a–Si: H ($n^+$–type) / Cr.

## RESULT AND DISCUSSION

First it was checked that whether or not the chromium metal made ohmic contact to the $n^{\pm}$–type amorphous film. It was found that chromium made a good Ohmic contact. The dependence of the current on the polarity of the voltage, showed that rectification occured in Au / a–Si: H / a–Si: H ($n^+$–type) / Cr structure as it was expected from metal / semiconductor theory. When the gold electrode was positive, the so–called forward bias condition it was seen that current increased exponentially with increasing voltage; under reverse bias condition the current approached saturation. When the current–voltage characteristics were measured at different period of time at room temperature (23 °C) after device fabrication the great modifications, at both forward and reverse bias, were obtained (Figure 2). The rectification ratio increased with time and ideality factor decreased. Since there is no the annealing effect on the potential barrier up to temperature to 70 °C (Masuyama 1983) the current–measurement was carried out over a small temperature range of 23, 30, 40, 50 °C in order to determine po-potential barrier haight $\varnothing_{Bn}$ in which corresponds to each different time by helps of the equation $\varnothing_{Bn} = (kT / e) \ \ln(eN_C\mu E / J_o)$. The result was summarized in Table 1.

It was also observed that the current–voltage characteristics of the structure followed the equation (Sharma 1984)

$$J = J_o \exp(eV / nkT) \left[1 - \exp(-eV / kT)\right] \tag{1}$$

When graphs of lnJ versus V were plotted, the straight lines that correspond to the different times were obtained. The diode ideality factor n was determined from the slope of the line drawn at forward bias for different time.

In ideal case, the barrier height $\varnothing_{Bn}$ is defined by electron affinitiy $\chi$ of the semiconductor and metal work function $\varnothing_m$ and has not any time–dependence. The surface states, when the exist, play an important role in the affecting the values of $\varnothing_{Bn}$, the dependence of $\varnothing_{Bn}$ on $\varnothing_m$ and on the density of surface states is given by (Cowley and Sze 1965, Wronski and Carlson 1977, Crowell 1974)

$$\varnothing_{Bn} = \frac{\varepsilon_i}{\varepsilon_i + e\delta D_s} \varnothing_m + C_2 \tag{2}$$

where $\delta$, $\varepsilon_i$, $D_s$ and $C_2$ are the thickness, the dielectric constant of the interface layer, density of surface states and a constant which is related

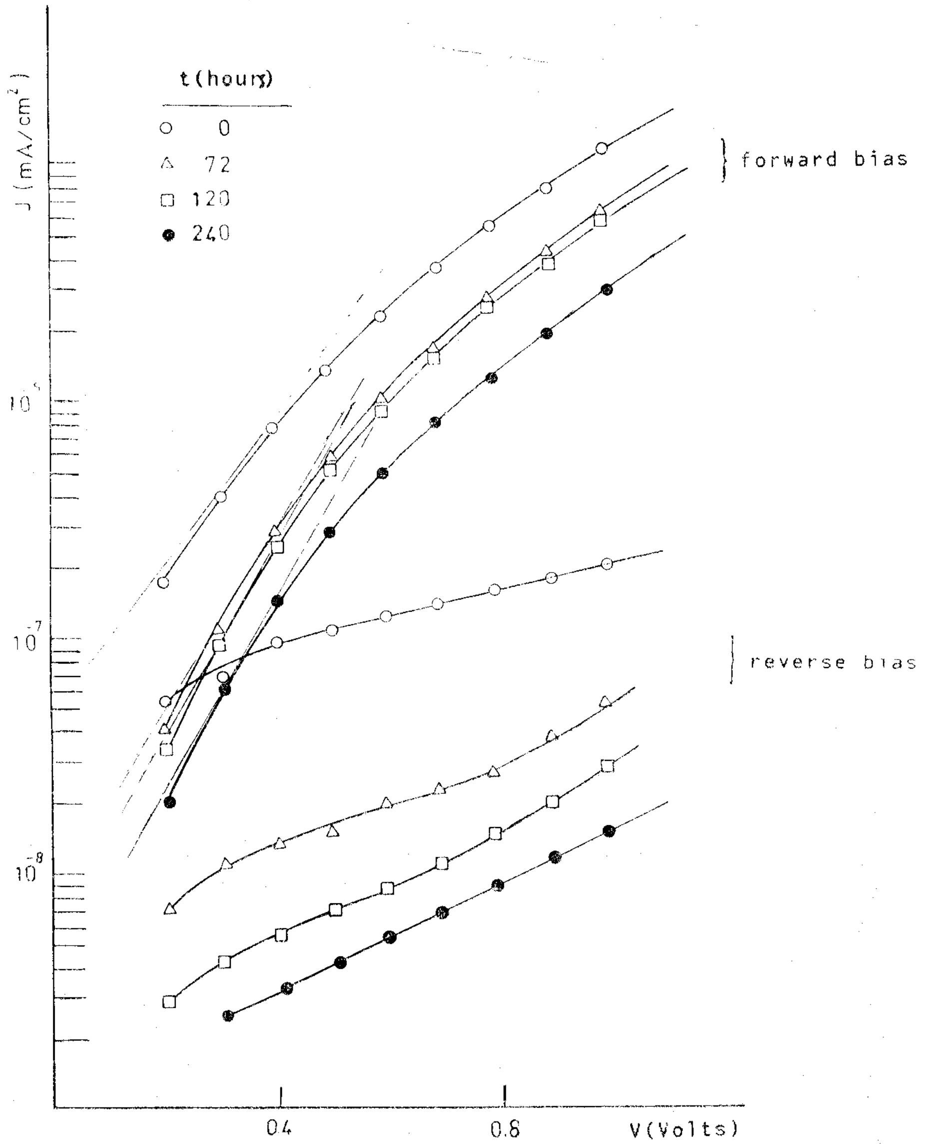


Figure 2. The values of lnJ measured for 23°C at forward and reverse biases versus V for Au / a–Si: H / a–Si: H (n+–type) / Cr structure at the different time.

to the density of surface states and their energy distribution respectively. In order to calculate the density of surface states $D_S$, equation (2) was used with the following assumption; (i), contact between the metal and the semiconductor has an interfacial layer of atomic dimensions; (ii), the interfacial layer is transparent to electrons with energy greater than the potential barrier; (iii), the density of the surface states at the interface is a property of the semiconductor surface only, and is independent of the metal. The term $C_2$, the thickness of the interface and dielectrical permittivity of the interface $\varepsilon_i$ were taken to be 0.44, 5 Å and $5 \times 8.85 \times 10^{-14}$ F / cm respectively as in the calculation of Wronski and Carlson (1977). It was observed that the surface density of states, $D_S$, decreased with the time as shown in Table 1.

Table 1. Potential barrier height $\varnothing_{Bn}$, density of surface states $D_s$, rectification ratio r and ideality factor n of Au / a-Si: H / a-SiH (n-type) / Cr structure in the different time.

| t (hours) | 0 | 72 | 120 | 240 |
|---|---|---|---|---|
| $\varnothing_{Bn}$ (eV) | 0.640 | 0.716 | 0.722 | 0.735 |
| $D_s$ ($10^{13}$ sta. $cm^{-2}eV^{-2}$ | 4.30 | 3.94 | 3.92 | 3.86 |
| r (at 0.8V) | 36 | 112 | 160 | 170 |
| n | 9.6 | 8.4 | 8.2 | 7.7 |

All the experimental results showed that significiant modification in the current–voltage characteristics were generated by the time. In other words, the diode characteristics improved with time. It was also seen that the value of $\varnothing_{Bn}$ was enclosed agreement with those of Serin (1983, 1984, 1987) and Jousse et al (1979). The reason of the modifications current–voltage characteristics with the time were attributed to the surface states at the gold / amorphous silicon interface. (Thompson et al 1983, Tsai et al 1981).

When the experimental results of present work are compared with those of Thompson, Singh (1981, 1983) it can be said that the observation are approximately the same even though the preparation techniques are quite different. The major similarities of these observations can be emphasized as (i), the Schottky barriers developes within the time; (ii), the ideality factor decreases, the rectification ratio increases; (iii) $LnJ_0$ varies as $t^{-1/2}$.

The Fermi level (near to interface) caused by the surface states is no longer flat. It is bend down to compansate the surface states by electrons, as is shown in figure 3. The amount of bending is said to be roughly proportional to the number of states. The surface states are thermaly excited in to the conduction band the means the number of surface states decreased and therefore some of the electrons can not return back to their original states and this causes a change in the electrical conductivity of the interface since the number of surface states decreases, the diode ideality factor, n, also decreases and the rectification ratio of the structure increases with time.

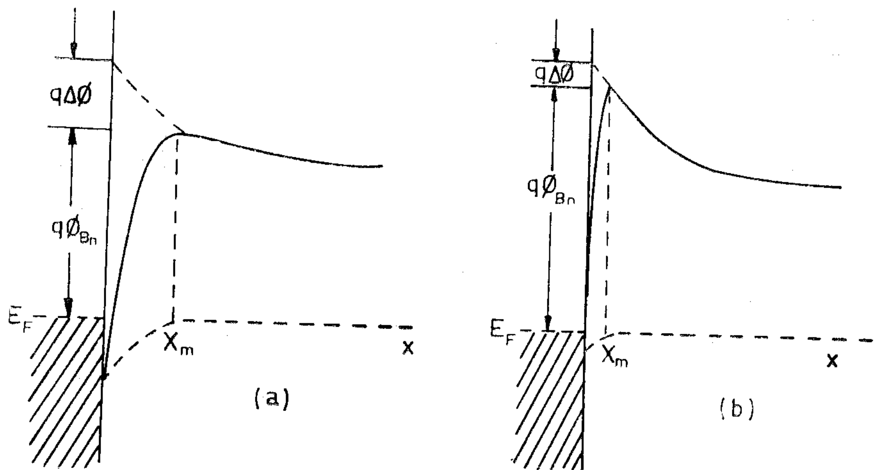


Figure 3. Potential energy distribution versus distance for Au / a–Si: H ($n^+$–type) / Cr structure (a), after the device fabrication, (b), after 240 hours.

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