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State-Of-The-Art On Reversible Multiplier Architectures and Its Comparison for Future Quantum Computing

Hemalatha K N[1,*], Sangeetha B G[2]

[1]*Dr. Ambedkar Institute of Technology, Visvesvaraya Technological University, Bangalore-560056, India*
[2]*RNS Institute of Technology, Visvesvaraya Technological University, Bangalore-560098, India*

Highlights

- Focuses on design of multiplier circuits using reversible logic.
- Approach is done to compare the different multiplier architectures using reversible logic.
- Analysis & Comparison of reversible multiplier architecture with design constraints.

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Abstract

Multiplication is the key crucial operation in realizing digital signal processing (DSP) functions. It is accomplished by using diverse multiplier architectures. Multiplication operation is furthermost basic and normally used action in the central processing unit (CPU). The multiplication operation is the most fundamental and commonly performed activity in the central processing unit (CPU). An efficient multiplier design should have a high speed, small area, and a low power consumption. Compact, efficient multipliers with minimal power dissipation are needed. The proposed paper provides a thorough inspection of multipliers such as the Array multiplier, Booth multiplier, column bypass multiplier, Baugh-Wooley multiplier, and Vedic multiplier based on their operational activities and working, as well as their benefits and limits. A comparison of these multipliers' performance parameters such as speed, area, power consumption, quantum cost, garbage generation and circuit complexity.

1. INTRODUCTION

Future computation is heavily reliant on reversible logic since it consumes less power than traditional logic. All circuits are expected to be designed in such a way that they use minimum power while providing great performance. The use of reversible logic in current designs will minimize power dissipation. Under ideal conditions, reversible logic dissipates no power [1,2]. Reversible logic is employed in low-power applications, quantum computing, and nanotechnology.

Multipliers are very crucial for the formation of abundant computational blocks of a computer. The multiplier is a significant block that is very much in need of future computing. Multiplication is one of the furthermost vital operations in the arithmetic & logic unit (ALU) block, implementing DSP functions. Among all arithmetic operations, the primary arithmetic operation, multiplication, consumes the majority of a processor's time and hardware resources. As a result, it necessitates the development of a fast multiplier in order to improve system performance. The paper proposed presents a comprehensive study on different multipliers designed using reversible logic specifically, Array multiplier, Booth multiplier, column bypass multiplier, Vedic multiplier, and Baugh-Wooley multiplier based on their operating techniques and functioning principles, as well as the benefits and drawbacks. Analysis is done on many performance constraints comparable to constant input, gate count, garbage output, and quantum cost. Multipliers are classified into serial and parallel multipliers; Figure 1 shows the classification of multipliers.

*Corresponding author, e-mail: knhemalatha@gmail.com

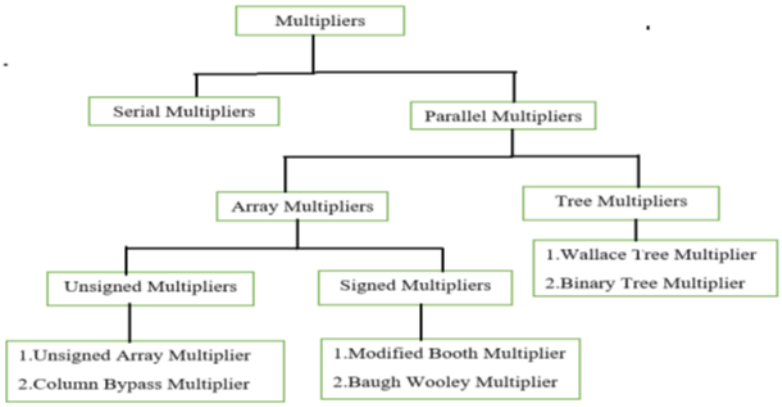

Figure 1. *Classification of multipliers*

There are numerous methods, as such to decrease the delay, decrease the partial products and to improve the complete speed of the computation, which directly improves the device's performance while also advancing multiplication efficiency [3]. As a result, array multipliers are huge, have a longer delay time, and consume more power, making them less efficient and sophisticated structured multipliers [4,5].

The goal of a compact multiplier design is to provide a physically compacted, low power consumption block with a high-speed block. The primary component of the processing unit is multipliers, which are in high demand for high-speed, low-power consumption applications. Power consumption in multiplier systems may be lowered by limiting the number of operations [6].

2. ARRAY MULTIPLIER

Array multiplier uses an array of full adders to multiply two 4-bit binary values. In array method, the different product terms are added at the same time. A large number of AND gates are used to generate the partial product terms. Following the array of AND gates, the adder array is used. To boost the multiplier's performance, different adder circuits are used. Carry skip adders, carry bypass adders, and carry select adders are examples of carry adders.

Array multiplier is recognized for its systematic assembly in multipliers. The design of the array multiplier is done in two portions as in Figure 2: partial product generation (PPG) and Multioperand addition (MOA) [7-11]. Every bit of the partial product is generated by multiplying each bit multiplicand with the one-bit multiplier. The Computation of partial product in array multiplier is in radix-2 method [12].

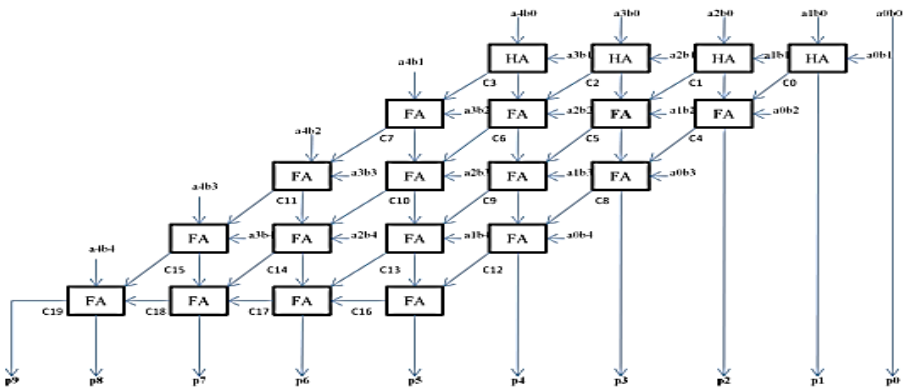

Figure 2*. Array multiplier architecture*

2.1. Literature Survey on Unsigned Array Multiplier Using Reversible Logic

Poornima, M. et al. [13] surveyed an overview of the recent developments in the reversible logic practices on fault-tolerant circuits. The multiplier is employed using Fredkin and IG gates. Fredkin gates are used for product generation. Partial products are produced in parallel by 16 Fredkin gates. Fredkin gate possesses parity-preserving logic which is used for the design of fault-tolerant circuits in reversible logic.
Rangaraju, H.G., et al. [14] proposed a reversible 4-bit multiplier by designing a new reversible RAM gate. RAM gate is primarily used for copying the signal since reversible circuits are having a fan-out of one. partial product is generated using RAM and Peres gate. DPG & Peres gates are used for multi-operand addition. The multiplier is designed by 32 gates. Mojtaba, V., [15] proposed reversible array multipliers through error detection using parity-preserving gates. Proposed 4-bit multipliers achieve up to 28 and 46% drop in the quantum cost and gate count respectively.

Radha, N. et al. [16] proposed an effective high-speed multiplier using Verilog code for functional verification and implementation by using Cadence tools. HNG gate is used for multiplier design. The proposed multiplier consumes less power, 28 gates, area, power consumption is calculated. Hemalatha, K. N., et al. [17] proposes, 4-bit and 8-bit reversible unsigned array multiplier using HNG, Peres & BME gates. The 4-bit design utilizes 20 reversible logic gates, 28 garbage outputs, and 104 quantum cost. The result shows a 50% reduction in constant inputs and garbage outputs, 30% reduction in the number of gates, and 20 % reduction in quantum cost.

Table 1. *Survey on unsigned array multiplier*

Author	Methodology	Design Constraints
Poornima, M., et al. [13]	Fredkin (FRG) & IG gates are used in the design of multiplier. FRG is used to generate product term by forcing one of the inputs to logic low.	Gates=16+12 Garbage=32 Cont. inputs=16+21
Rangaraju, H.G., et al. [14]	PG & DPG gates are used in the design of 4-bit array multiplier.PG gate is used for product generation and DPG gate is used for multibit addition. For fan out RAM gate is used.	Gates=32 Garbage=40 Cont. inputs=40 Quantum cost=140
Mojtaba, V., et al. [15]	4-bit parity preserving unsigned array multiplier is designed by using FRG & LMH gate. Fault detection is added along with the multiplication by using fault tolerant gates.	Gates=24 Garbage=24 Cont. inputs=32 Quantum cost=96
Radha, N., et al. [16]	HNG gate is used for product generation & multibit addition. HNG gate is used for 1-bit full adder realization.	Gates=28 Garbage=72 Cont. inputs=44
Hemalatha, K.N., et al. [17]	Design uses BME gate for partial product generation. Peres and HNG gates are used as half and full adder for multibit addition.	Gates=20 Garbage=28 Cont. inputs=20 Quantum cost=104

Various papers are analyzed as in Table 1 on the designs of various array multiplier using reversible logic gates. Functional verification of most of the designs is verified using EDA tools like Xilinx software or Cadence. Array multipliers are realized by straight mapping of the physical multiplication in terms of hardware. The relative examination is carried out for existing array multipliers in terms of reversible logic design constraints.

3. BAUGH - WOOLEY MULTIPLIER

The Baugh - Wooley multiplication method is a fast approach to deal with sign bits. This approach was created in order to provide regular multiplication for 2's complement numbers. Multiplication using the signed method is very important in today's world. Baugh- Wooley multiplication works on 2's complement of the operands. Multiplier using two's complement at initial might seem more complex since few partial products are negative and have to be subtracted. The most significant bit of a two's complement number has a negative weight [18-21]. Henceforth, the signed multiplication product is computed as shown in Equation (1)

$$P = \left(-y_{M-1}\,2^{M-1} + \sum_{j=0}^{M-2} y_j\,2^j\right)\left(-x_{N-1}\,2^{N-1} + \sum_{i=0}^{N-2} x_i\,2^i\right)$$
$$= \sum_{i=0}^{N-2}\sum_{j=0}^{M-2} x_i\,y_j\,2^{i+j} + x_{N-1}\,y_{M-1}\,2^{M+N-2} - \left(\sum_{i=0}^{N-2} x_i\,y_{M-1}\,2^{i+M-1} + \sum_{j=0}^{M-2} x_{N-1}\,y_j\,2^{j+N-1}\right) \quad (1)$$

Baugh- Wooley multiplier as shown in Figure 3 handles subtraction by 2's complement of the terms to be subtracted. The upper parallelogram rows denote the unsigned multiplication of all bits of the inputs. The next row corresponds to a single product of the most significant bits. The next two rows are the inversions of the bit terms to be subtracted [22-25].

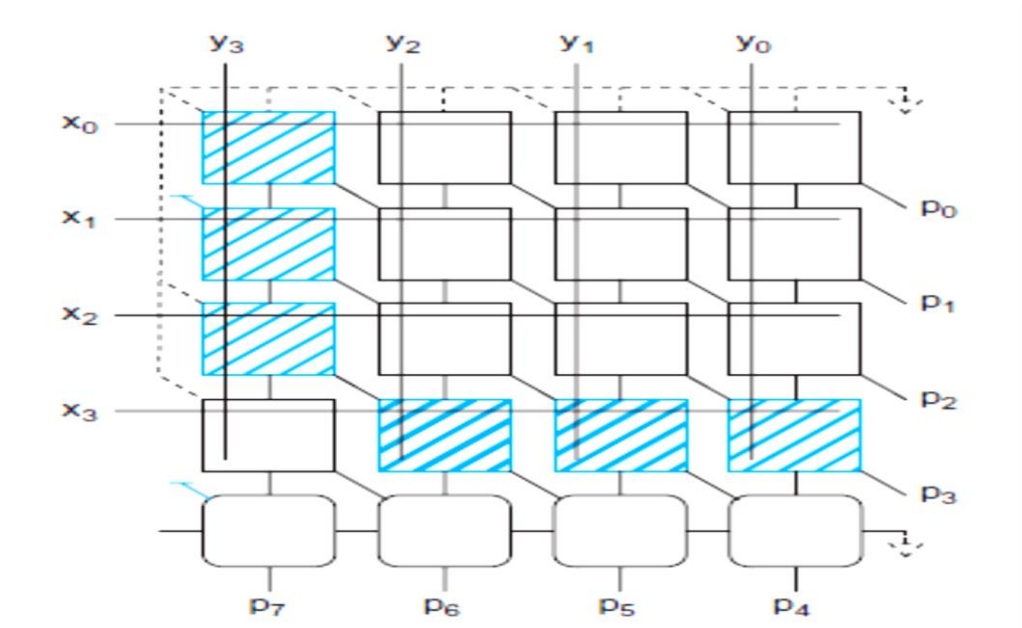

Figure 3. *Baugh-Wooley multiplier architecture*

3.1. Literature Survey on Baugh - Wooley Multiplier Circuits

Ratnababu, Y., et al. [18] proposed 4-bit Baugh - Wooley signed multiplier circuits for multiplication using reversible logic. Reversible RS gate is designed to gain benefit from the gate count using the existing counterparts. Rajmohan, V. et al. [19] proposed 5-bit reversible multiplier cell to be used in designing the Baugh - Wooley multiplier. A single multiplier cell is capable of performing the addition of a 1-bit product with sum and carry from the earlier cell.

Table 2. *Survey on Baugh- Wooley multiplier*

Sl. No	Author	Methodology	Design Constraints
1	Ratnababu, Y., et al. [18]	Reversible signed & unsigned multiplier is designed. Partial product is generated by using RS gate and DPG gate is used for multibit addition & subtraction by changing the control input.	Gates =27 Garbage =31 Cont. inputs =29 Quantum cost = 150
2	Rajmohan, V., et al. [19]	Signed multiplier is designed by using two new multiplier cells called gray & black cells, having 5 inputs and 5 outputs capable of multiplying signed 2-bit numbers.	Gates =20 Garbage =32 Cont. inputs =16

On analyzing the research carried on the Baugh-Wooley multiplier (signed multiplier) as discussed in Table 2 very little work has been done on the signed multiplier. Since the design of signed multiplier is complex compared to array multiplier because generation of the partial product involves AND & NAND operation between bits of multiplier and multiplicand, adder and subtractor in the multi-operand addition.

4. COLUMN BYPASS MULTIPLIER

Multiplier speed of operation depends on the generation of partial products. Numerous algorithms & architectures are developed to reduce the area, power, and propagation delay. Design of multiplier for low power applications is too good to decrease the switching action [26] and existing analysis also provides a straight approach for designing a low power multiplier.

Bypassing through multiplier is turning off a few rows or columns or both in the array multiplier when a certain multiplicand or multiplier or both bits are zero. The first column bypass method eliminates the additional correcting blocks that are needed. Second, the improved full adder in column bypassing as shown in Figure 4 is simpler than what is used in the row bypassing technique [27].

Array multiplier has a collection of Full Adders. One of the inputs is zero then the sum of the adder is nothing but the sum of the other two inputs. Instead of using the same redundant bit for addition, skip the addition and offer inputs from the subsequent level [28]. The power is saved due to a redundant addition with zeros in the inputs. If the bit Ai in the multiplicand is zero in a column bypassing multiplier, then addition operations in the ith column can be avoided for power savings. As a result, the actions in the (i+1) th column are skipped. All of the partial product inputs in that column have no effect on the carry at any point in time. As a result, one 2:1 multiplexer is spared here that is not required at the carry output. The partial product unit, the complete adder unit, and the column bypass unit are the three computing blocks of the reversible column bypass multiplier.

Product Unit (PU): The partial products are computed using the Product Unit (PU). There are two inputs and one output on this device.

Full Adder Unit (FAU): The total and carry are calculated using the Full Adder Unit (FAU). Three inputs and two outputs are available.

Column Bypass Unit (CBU): The column bypass multiplier's carry saves adder stages employ this unit. CBU is a column bypass unit comprises of half adder/full adder and a 2:1 multiplexer with three inputs and three outputs.

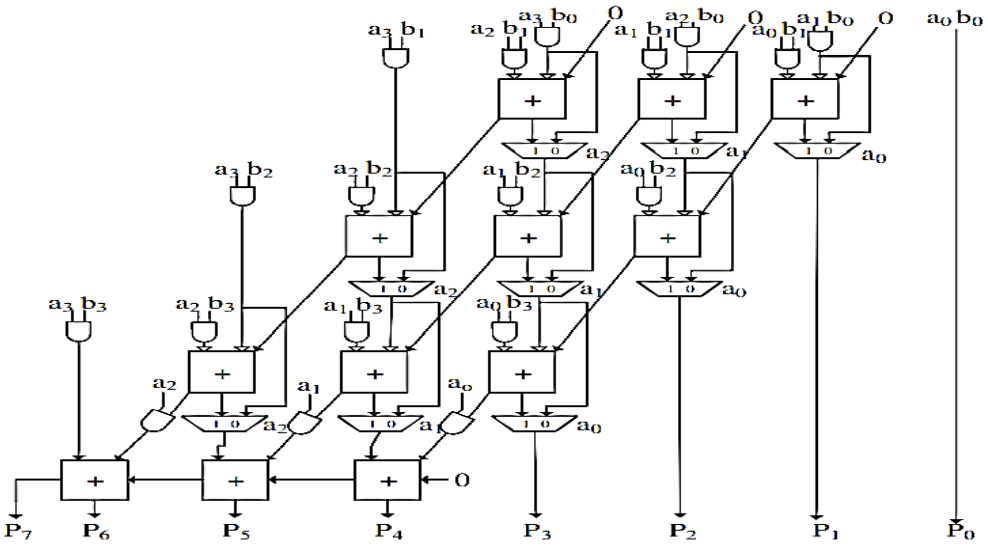

Figure 4*. Column Bypass multiplier architecture*

4.1. Literature Survey on Column -Bypass Multiplier Circuits

Kumar, P., et al. [26] present a multiplier that consists of new adder cells. Results are compared with different multiplier architectures. Multipliers are designed for 8-bit & 16-bit operation. At different operating frequencies starting from 1 MHz to 333.3 MHz results are calculated for power consumption. Jigalur, V., [27] proposed a competent 4-bit reversible multiplier utilizing the column bypass method by which the switching action is reduced.

Saligram, R., et al. [28] proposed column- Bypass multiplier design using reversible logic. Bypassing technique is the competent way to lessen power. A bit in the multiplicand and/or multiplier is zero then the complete array of the column is bypassed. Bypass design reduces the number of switching actions and power consumption.

Table 3*. Survey on column bypass multiplier*

Sl.no	Author	Methodology	Design Constraints
1	Jigalur, V., et al. [27]	4x4 column bypass multiplier is designed to reduce the switching activity when the binary input consists of more number zeros. Design uses two new gates MHA and MFA by which design parameters are reduced.	Gates =31 Garbage =31 Cont. input=31
2	Saligram, R., et al. [28]	Column bypass multiplier does not require correction circuit as related with row bypassing scheme. Two-dimensional column bypassing method is realized using reversible logic.	Gates =40 Garbage =80 Cont. input=31 Quantum cost=193

In column bypassing multiplication operation as discussed in Table 3, few columns of adders in the multiplier design are disabled during bypassing operation to reduce power dissipation. In column bypassing multiplier, if multiplicand bit in the column bypass multiplier is zero then addition operation can be bypassed in that column for power reduction. Then the operation performed in the (i+1) column is bypassed.

5. BOOTH MULTIPLIERS

The operation of the multiplier is enhanced by reducing the number of operations performed. Booth multiplier as shown in Figure 5 is introduced to reduce the number of iterations based on the radix -x method. Booth multiplier is fast compared to other multiplier algorithms [29]. Many encoding approaches are existing in modified Booth multiplier depending on the number of bits in each group as radix-2, radix-4, etc. [30]. In the radix-4 modified Booth algorithm, multiply X and Y using the grouping of multiplicand bits into a group of 3 bits and encoding {–2, –1, 0, 1, 2} into one among them. The total number of groups formed is dependent on the number of multiplier bits. Using the radix-4 modified Booth algorithm the number of partial product rows is reduced to N/2 from N in the case of the radix-2 method.

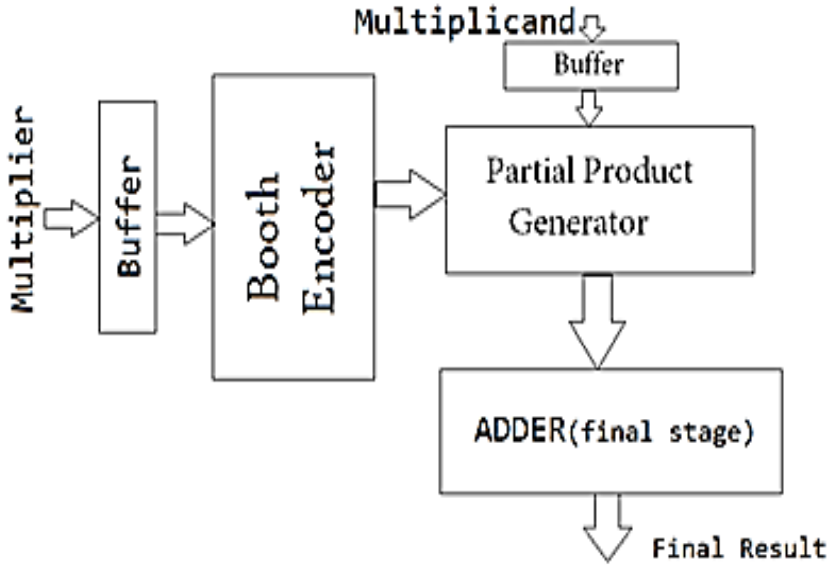

Figure 5*. Booth multiplier architecture*

5.1. Literature Survey on Booth Multiplier Circuits

Sultana, J., et al. [31] presented multiplication of both unsigned & signed number multiplication without taking feedbacks. N-bit reversible Booth's multiplier is designed by using B cell & C cell for performing operations. Nandal, A., et al. [32] presented a multiplier design based on the modified Booth algorithm to fast-track the multiplication speed with power reduction. The resultant multiplier design has improved performance with others multipliers in the literature. Booth multiplier designed exhibits reduced logical complexity by 12% with 10% reduced power consumption.

Talawar, K., et al. [33] proposed an ultra-area efficient reversible multiplier on Radix-2 Booth's recoding manner which is designed and improved with garbage output & quantum cost. Md. Rahman, M., et al. [34] proposed the fault-tolerant reversible Booth multiplier. N-bit booth multiplier uses n number of C cells, 2n-1 number of B cells. Nagamani, A.N., et al. [35] proposed a reversible Radix-4 Booth Multiplier using reversible logic that is enhanced in optimization parameters. The multiplier is added with an addition of logic 0 to the LSB. The bits are grouped into 3-bits each with the overlapping of the last MBB bit as the LSB of the next group. The multiplicand bits are sent to the first 4 AU blocks and the sign bit is sent through the remaining AU block of the 1st row. Hari Sai Ram Vamsi et al. [36] proposed Booth encoded Radix-16 Wallace tree multiplier. Various kinds of adders are considered and all combinations of the designs are compared.

Table 4. *Survey on Booth multipliers*

	Author	Methodology	Design Constraints
1	Sultana, J., et al. [31]	4-bit Booth multiplier treats both sign & unsigned numbers for multiplication. Booth multiplication is explained by using array multiplication. Reversible is designed to perform multifunction operation like addition, subtraction & no operation.	Not mentioned
2	Nandal, A., et al. [32]	4-bit Booth algorithm is used to speed up the process of multiplication by power reduction. New reversible gate NTG is proposed which is capable of performing any Boolean operation.	12% drop in logical complexity, 10% condensed consumption of power
3	Talawar, K., et al. [33]	Booth recoding technique is used for radix-2 multiplication. 8-bit shift register is designed using PG gate,4-bit multiplexer by FRG gate,4-bit XOR gate by Feyman gate & 4-bit full adder using HNG gate.	Gates =27, Garbage =19, Quantum cost=87
4	Rahman, M., et al. [34]	Fault tolerant reversible Booth multiplier is designed using B & C cell for 2,4,8,16 & N-bit.	Gates =105 Garbage =157 Quantum cost=480
5	Nagamani, A.N., et al. [35]	Radix-4 reversible Booth multiplier is designed using 3 blocks Control block, arithmetic block and multiplexer block. Control block takes care of partial product, arithmetic unit takes care of addition/subtraction and multiplexer is used for shifting operation.	Garbage =11 Cont. inputs=30 Quantum cost=364
6	Vamsi, H.S.R., et al. [36]	Radix-16 reversible Booth encoded multiplier using Wallace tree approach & testable reversible 64-bit PIPO is designed.	Gates =1311 Garbage =1123 Quantum cost=2871

To improve the performance efficiency of the Booth multiplier, several changes have been done as mentioned in Table 4, such as the Booth encoder technique and decrease partial products by different radix grouping. Booth multiplier is considered as the better option since it consumes less power, area and computes at a faster rate compared to other multipliers if Modified Booth multiplying techniques are used.

6. VEDIC MULTIPLIERS

Vedic Mathematics is a structure of mathematical working and reasoning based on Indian ancient teachings called Veda. Vedic mathematics is originated from Vedas such as Atharva Vedic mathematics, make simpler algebraic & arithmetic operations as shown in Figure 6 is used to implement both in binary & decimal systems [37]. The Urdhva Tiryakbhayam (UM) is a technique of multiplying integers built on ancient Vedic mathematics that can handle hexadecimal, decimal, and binary values. Urdhva and Tiryakbhayam are Sanskrit terms that mean vertical and crossed respectively. This procedure is used to multiply two operations that are "vertical" and "crossed." This approach is built on the idea of producing partial products and summations concurrently, which boosts the speed of multiplication.

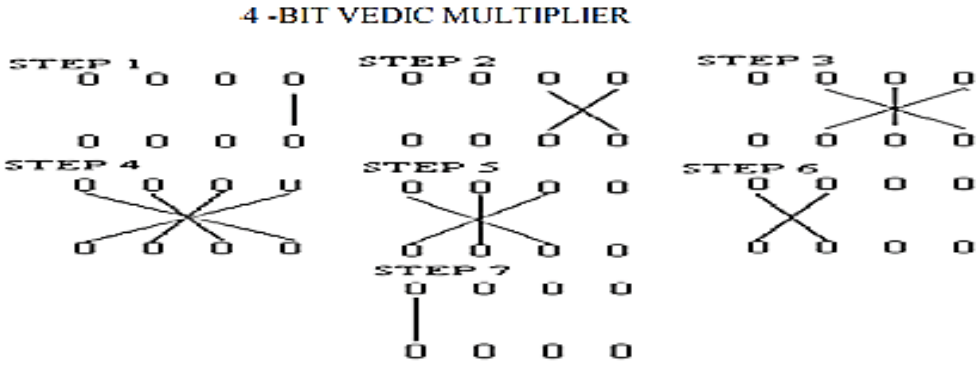

Figure 6*. Line diagram for 4-bit Vedic multiplier*

6.1. Literature Survey on Vedic Multipliers

Ariafar, Z., et al. [38], proposed 4-bit efficient reversible multipliers using Vedic mathematics. The first design does not have parity-preserving, while the second design has the capability of parity preserving [39]. Rashno, M., et al. [40] introduced four 2-bit r Vedic multiplier blocks using reversible logic, partial products are generated over vertical and cross multiplication. Lakshmi, G.S., et al. [41] proposed a new design using a 4:2 Compressor based reversible 8-bit Vedic Multiplier. Ravi, J.N., et al. [42] presented the design using the Peres gate as the main block for the Vedic multiplier. Lakshmi, P.K., et al. [43] introduced the Urdhva Tiryagbhyam algorithm using reversible logic by addressing two problems – speed and power consumption of multipliers. Analysis of Vedic multiplier with design constraints is done in Table 5.

Table 5*. Survey on Vedic multipliers*

Sl.no	Author	Methodology	Design Constraints
1.	Gowthami, P., et al. [37]	2-bit multiplier designed using Urdhva Tiryakbhayam sutra based on four basic equations.	Garbage =5 Cont. inputs=5 Quantum cost=17
2.	Ariafar, Z., et al. [38]	4-bit Vedic multiplier is designed using reversible logic with two methods, with parity preserving & without parity preserving.	Gates =44 Garbage =73 Cont. inputs=72 Quantum cost=226
3.	Radha, N., et al. [39]	4-bit reversible multiplier is designed using carry look ahead adder using propagate & generate signal. Design is extended using parity preserving gates.	Gates =28
4.	Rashno, M., et al. [40]	4-bit reversible Vedic multiplier is designed by avoiding branching between various circuit stages and every variable is treated as input once in the design.	Garbage =36 Cont. inputs=32 Quantum cost=160
5.	Lakshmi, G.S., et al. [41]	8-bit reversible Vedic multiplier is implemented by using 4-bit Vedic multiplier.4:2 compressor is used in the design. Design combines both reversible logic & compressor logic.	Gate =68 Power=0.397mw Delay=7944ps
6.	Ravi, J.N., et al. [42]	4-bit reversible Vedic multiplier is designed using 2-bit reversible Vedic multiplier.	Delay=13.839ns Power=60mw
7.	Lakshmi, P.K., et al. [43]	4-bit reversible Vedic multiplier is designed using Urdhva Tiryagbhyam sutra thus addressing speed & power issues. Additionally, Vedic multiplier is designed to perform signed multiplication.	Gate =31 Cont. input=31 Garbage =40 Quantum cost=156

7. CONCLUSION

High-efficiency multipliers are critical for improving the performance of today's communication setup. In the case of multipliers, the major characteristics to consider are delayed time, power consumption, circuitry complexity, and area required.

Table 6. *Comparison of different multiplier architecture*

Sl. No	Architecture	Structure/Complexity	Area	Speed
1	Array Multiplier	Linear	Medium	Medium
2	Baugh Wooley Multiplier	Linear	Medium	Medium
3	Column Bypass Multiplier	Nonlinear	High	High
4	Booth	Nonlinear	Low	Highest
5	Vedic Multiplier	Nonlinear	Medium	Medium

Table 6 shows the comparison for different multipliers in terms of delay, structure and speed. The multiplier architecture is chosen according on the requirement/application. Array multiplier, however, has a poor speed and a high-power consumption. The modified Booth multiplier is the quickest multiplier of all since it makes use of both multipliers: Wallace multiplier & the modified booth multiplier. Total number of partial products in this multiplier is condensed to one-third or half the number of multipliers bit by utilizing the radix 4 and radix-8 techniques, respectively. By reducing the number of partial products and examining more than one partial product at the same time, the system's speed is increased. Vedic multipliers, which are based on Vedic mathematical formulas, are among the quickest and least power-consuming multipliers.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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