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A Configurable Interface for Analog Sensor Outputs

Baran DEMİRER[1], Faik BAŞKAYA*[1]

Abstract

Reading out analog sensor outputs can be a challenging task at low frequencies because of the low frequency noise. To obtain a sensor signal clearly, special interface circuits are required. By using such circuits, analog signals are cleaned from offset, drift and 1/f noise. Besides, if the interface circuitry is configurable, it can be possible to interface to inputs at different frequency ranges. At the interface block, analog sensor output signal is moved to a frequency band where low frequency noise effects are not dominant by using chopping modulation technique. The frequency-shifted signal is then filtered using various filter types. To remove the low frequency noise before moving the signal back to the original band, G_m-C filter is used. The entire topology can be configured by a 5-bit digital to analog converter (DAC) called Biasing DAC (BDAC). This allows us to digitally change the biasing current of operational transconductance amplifiers (OTA), so that OTA based amplifiers and filters can operate at different frequency ranges. As conclusion, a configurable analog sensor interface has been designed. The design and layouts have been realized and simulated in Cadence Virtuoso using UMC 130nm CMOS technology.

Keywords: Sensor, sensor interface, analog

1. INTRODUCTION

Importance of sensors and sensing devices has increased dramatically recently. As a definition, a sensor is an electronic device that detects or responds to changes and events in its environment. These events can be changes in temperature, pressure, illumination resistance or capacitance values etc. Thus, different types of sensors are needed. Measuring blood sugar, temperature [1], and reading biomedical signals [2], seismic signals [3], accelerometer data [4] are common examples of sensors used in our lives. Yet, it is not enough only to measure or sense but also important to transmit these signals faithfully to a circuit where they will be processed. To achieve this, interface circuits are needed to read, evaluate, modulate, clean, and amplify the output of analog sensors. They are also used to eliminate low frequency noise such as 1/f noise and DC offset of components. Otherwise, noise and offset interfere with the real signal and decrease the signal to noise ratio (SNR), resulting in false sensing or incorrect measurement. Today's technology has enabled us to measure a plethora of physical quantities utilizing as many sensors. These sensors have different requirements when it comes to their interfaces due to the fact that the underlying sensing mechanisms are quite

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different. Designing a new interface for each sensor type and application is an unnecessarily difficult and expensive task.

In this paper, we propose a configurable interface topology that can be used for a wide range of analog sensor outputs without requiring a new design. The proposed configurable interface circuit uses a variable frequency chopping modulation technique to eliminate the DC offset contributions of the amplifier, while a configurable Gm-C filter removes the high frequency artifacts added by the chopper to the signal. In addition, a fully differential design approach improves common mode signal and noise rejection. Although these techniques are known to be useful for reducing the low frequency noise as well, the main focus in this paper has been demonstrating the elimination of the offset voltage. The next section describes how chopping technique eliminates low frequency noise, drift, and offset. In section 3, the design and operation of each individual block has been explained. Section 4 presents the simulation results of the entire design, while section 5 concludes this paper.

2. BACKGROUND

Analog sensor interfaces may perform with various sensor outputs such as data from biological signals, accelerometers, seismic sensors, shock sensors, ultrasonic sensors, acoustic sensors, etc. However, noise, offset, and drift are major problems while reading out these sensor outputs. the most significant achievement of this sensor interface is reading and cleaning the outputs of different types of sensors up to 15kHz frequency effectively.

Threshold voltage (V_{TH}) of a transistor depends on various factors such as body effect, operating temperature, oxide thickness and dopant concentration in the channel region [5]. Since oxide thickness and dopant concentration cannot be uniform throughout the entire IC because of process variations, V_{TH} values deviate from typical values, resulting in unbalanced differential pairs. Offset voltage at the input of a differential pair can go up to 10mV in CMOS technology because of the mismatches in transistor V_{TH} values [6]. Increasing device dimensions might alleviate the offset problem at the cost of increased chip area and input capacitance [5].

Upper limit for offset voltage at the input of a differential pair can be 10mV in CMOS technology because of the mismatches in transistor threshold voltage values manufacturing variations or uncertainty [6]. Threshold voltage V_{TH} is a function of doping amount in the channel and gates in MOS devices. The reason why there might be mismatch in the V_{TH} is that these parameters may have different values depending on the device [5]. Besides, during fabrication of MOS transistors, mismatch might occur in micron level that result in the offset. Increasing device dimensions might solve offset problem but that occupies too much chip area [5].

1/f noise stems from the defects in the gate oxide and silicon substrate. Thus, 1/f noise depends on the purity of oxide-silicon interface. At low frequencies, 1/f noise is the dominant noise factor in CMOS technology, and it is modeled as in equation (1) below:

$$V_n^2 = \frac{K}{W.L.C_{ox}.f} \quad (1)$$

In the equation, K is a constant depending on process and it is in the order of 10^{-25} V^2F, W and L are the width and length of the MOS transistor, C_{ox} is the capacitance per unit area, and f is the frequency. 1/f noise performance of PMOS is better than NMOS in most technologies [5].

Drift is caused by the cross-sensitivity of some error sources to temperature or time. For high precision temperature measurement, it is very important that the drift has to be detected at the component level and must be kept low. Gain and offset drifts are the two main types of drift and have to be eliminated to decrease the overall drift level.

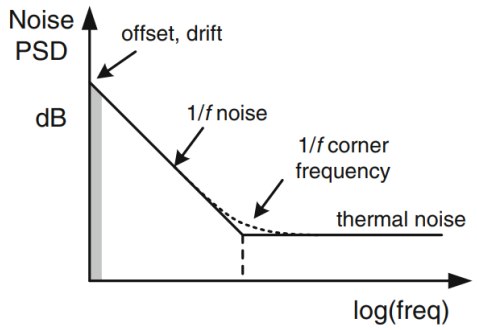

Figure 1 Low frequency noise spectrum of CMOS and 1/f noise [5]

To summarize, at low frequencies non-idealities are mainly caused by 1/f noise, offset, and drift in CMOS technology as illustrated in Figure 1. To eliminate these errors, some of the precision techniques that can be applied to the output signal of sensors are autozeroing, correlated double sampling, dynamic element matching, and chopping [5]. In this work, chopping technique is the preferred approach to eliminate the low frequency effects mentioned above.

2.1. Chopping Technique

Chopping is a continuous time modulation and precision technique which is used to obtain high precision signals from the analog sensor outputs, introduced with the vacuum tube amplifiers.

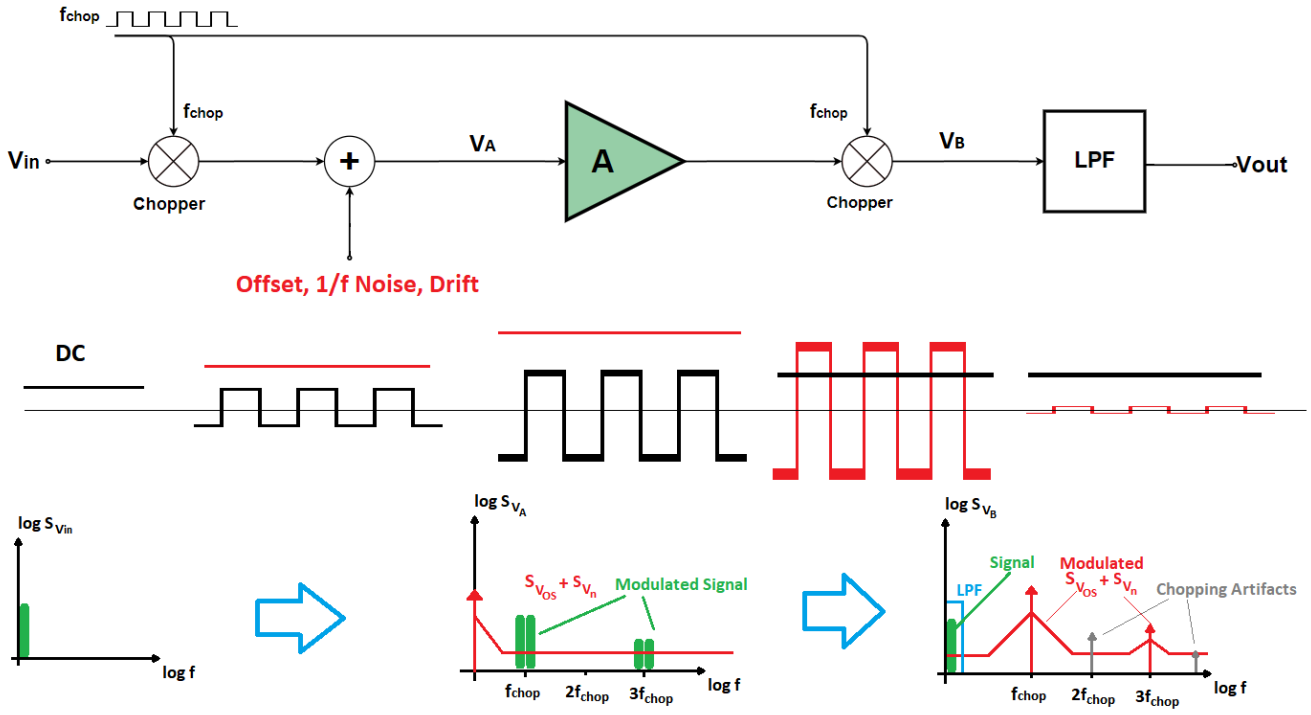

Figure 2 General scheme of chopping topology [5]

As depicted in Figure 2, input signal V_{in} is first modulated (chopped) at f_{chop} frequency, effectively shifting low frequency components of the sensor output signal to higher frequencies. When the modulated signal is amplified, DC offset and low frequency noise contributions from the amplifier will not affect the actual signal components since they remain at a higher frequency at this stage. Then the amplified signal is demodulated to DC level by another identical chopper. In the meantime, the low frequency components such as DC offset, the dominant low frequency components of 1/f noise and drift are shifted to odd harmonics of f_{chop}. Finally, the demodulated signal is filtered by a low-pass filter, which separates the input signal from low frequency non-idealities [5]. The remaining signal components from modulated offset and

noise as well as chopping artifacts appear as ripples in Figure 2. The amplitude of these ripples can be reduced by increasing the chopping frequency f_{chop}. To remove 1/f noise effectively, f_{chop} should be set to a frequency much higher than the noise corner frequency. The upper limit for f_{chop} is determined by the 3dB point of amplifier bandwidth.

3. DESIGN OF BLOCKS

In this section, circuit design for each block in the paper will be presented. Design properties and explanations are provided with references. The entire design has been implemented in UMC 130nm technology using Cadence Virtuoso CAD tool.

3.1. Biasing Circuit

The biasing circuit generates reference voltage and current values to bias OTAs and OPAMPs. All biasing voltages or currents are generated internally using a digital input value, making the whole design self-biased. The biasing circuitry of the interface system is a bandgap reference circuit which has complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) circuits as depicted in Figure 3 [7].

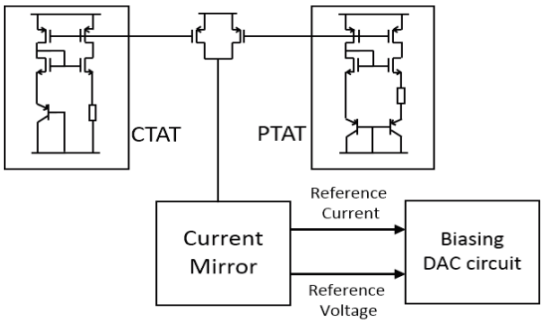

Figure 3 Biasing scheme of overall design [7]

3.1.1. Bandgap Reference Circuit

Bandgap reference circuit provides the constant voltage and current (V_R, V_B, and I_{bias}) required to bias various blocks independent from the variations in temperature [8]. The bandgap reference circuit consists of a CTAT circuit, a PTAT circuit, and a pair of transistors that mirror and add the currents from CTAT and PTAT. The currents obtained from CTAT and PTAT are mirrored to generate reference voltages and currents. As the temperature increases, the voltage and current values generated by CTAT circuit decreases while in the PTAT circuit, current and voltage values increase to compensate the loss from CTAT.

Figure 4 depicts the details of the bandgap reference circuit used in the proposed system. In CTAT, base-emitter voltage (V_{BE}) of the BJT, which is equal to the voltage on the resistor, decreases as the temperature increases, forcing the current through the resistor to decrease as well. In the PTAT part on the other hand, there are two BJT transistors, one of which is 5 times larger than the other one. The difference between the V_{BE} voltages of these two BJT transistors, which is equal to the voltage on the resistor used in the PTAT circuit (V_{Res}), varies proportionally to the temperature as shown in equation 2, forcing the current through the resistor to increase:

$$V_{Res} = V_{EB2} - V_{EB1} = \frac{kT}{q} \ln\left(\frac{I_2.A_{E1}}{I_1.A_{E2}}\right) \quad (2)$$

The currents flowing through CTAT and PTAT resistors are mirrored and summed to obtain a current that does not vary with temperature changes. The summed current then flows into a cascode current mirror to generate the reference and biasing voltages V_r and V_b. The bandgap reference circuit also generates the biasing current at I_{out} port with 1μA value. At the V_r and V_b nodes, voltage values of 623mV and 903mV are generated respectively.

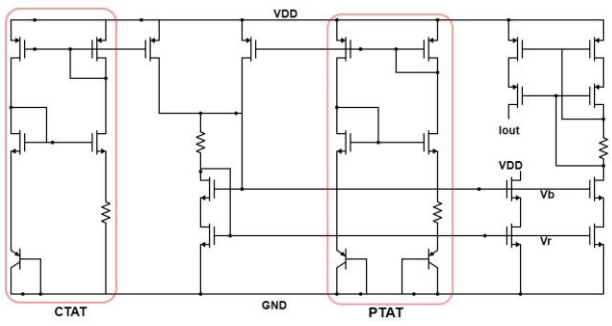

Figure 4 Bandgap reference circuit with CTAT and PTAT circuits

3.1.2. Biasing Digital to Analog Converter (BDAC)

BDAC is a digital to analog converter that is based on current steering topology and is used to bias OTAs and OPAMPs used in the system. Since voltage level at the output of BDAC will be used for only biasing and is not expected to change frequently while operating, conversion speed is not a priority.

Schematic of the BDAC is depicted in Figure 5. Switches are connected to 5-bit digital control word to set output current to desired value. The digital input word n determines the number of turned on cells that results in the output current $I_{out} = n.I_{ref}$. The value of I_{out} changes from 0 to 31μA. The 5-bit digital input is connected to BDAC via 5 transmission gate switches. Figure 6 displays the output characteristics of I_{out} current. Current values vary from 0 to 31μA and each bit combination corresponds to a current value. Differential non-linearity (DNL) error values of the used design vary between 0.01 and 0.03 LSB. Integral non-linearity (INL) is less than +/-1 LSB.

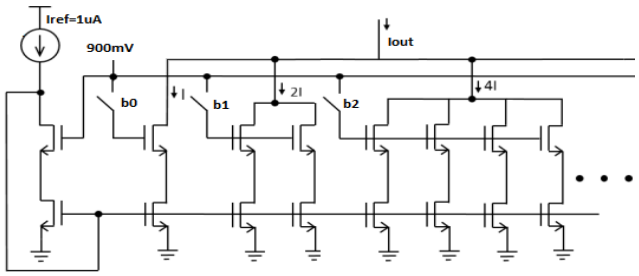

Figure 5 5-bit current mirror based BDAC [13]

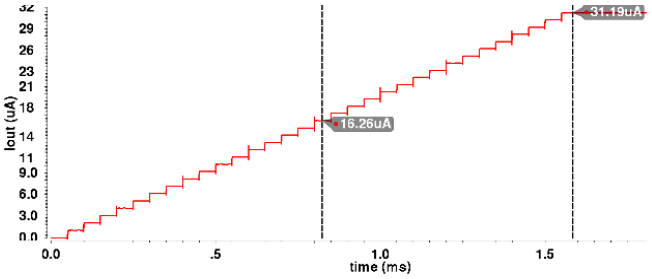

Figure 6 Output current of BDAC

3.2. Chopping Amplifier

3.2.1. Chopper

To make a chopping amplifier, choppers are connected to both input and output of an Operational Transconductance Amplifier (OTA). Each chopper has four switches driven by the complementary periodic signals CLK and $\overline{CLK}$ at chopping frequency f_{chop} as depicted in Figure 7. To prevent V_{TH} drop during switching, transmission gate switches are preferred rather than NMOS switches. Transmission gate switches also have better characteristics in terms of noise margin, less switching resistance, and less power dissipation [9].

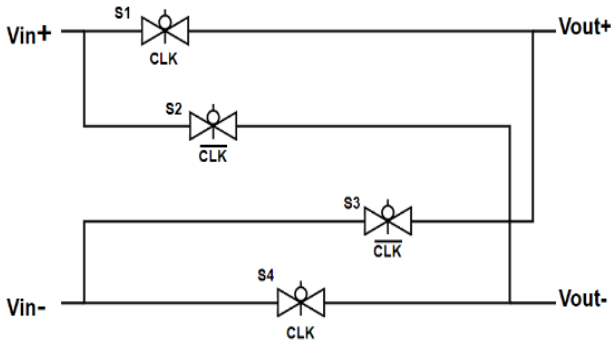

Figure 7 Chopper circuit schematic

3.2.2. Amplifier

In this part, amplifier of chopping topology and its operation with modulator chopper and demodulator chopper are explained. Amplifier block of chopping topology consists of a fully differential folded cascode OTA and it is depicted in Figure 8. The reason for preferring the folded cascode topology is its better output swing and common mode input range in comparison to the telescopic counterpart [10]. At the input of the folded cascode topology, PMOS differential pair is chosen due to its better noise performance than the NMOS pair.

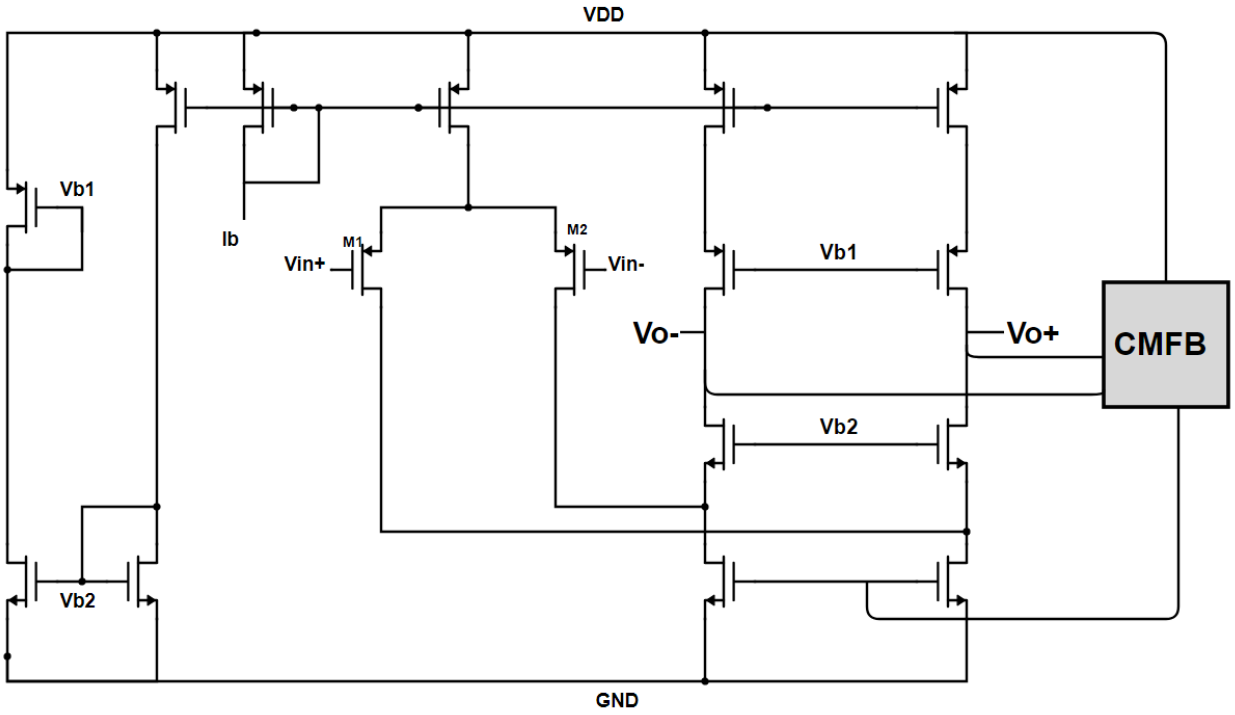

Figure 8 Amplifier of chopping topology with common mode feedback

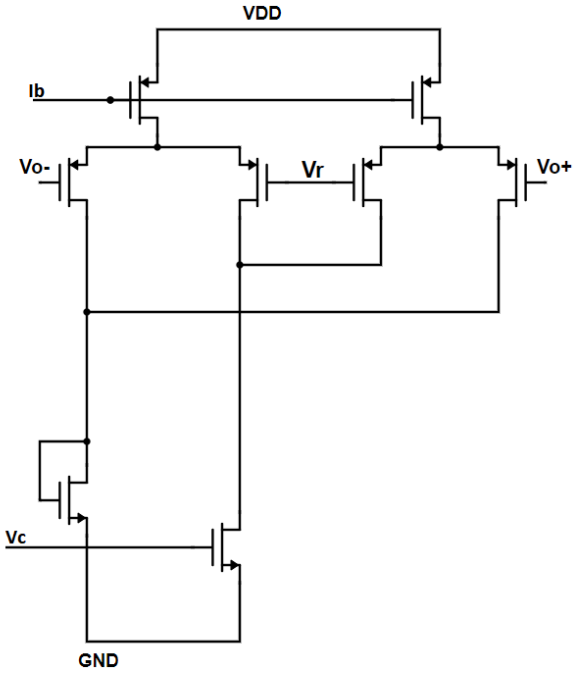

Figure 9 Common mode feedback circuit

Common mode feedback (CMFB) is used in order to control the output common mode voltage level and reject the common-mode activity of some components. To achieve these, CMFB with two differential pairs has been applied as depicted in Figure 9. As depicted in Figure 10, differential gain of the amplifier varies from 28dB to 32dB while its phase margin varies from 60 to 90 degrees when the biasing current is swept from 1µA to 31µA.

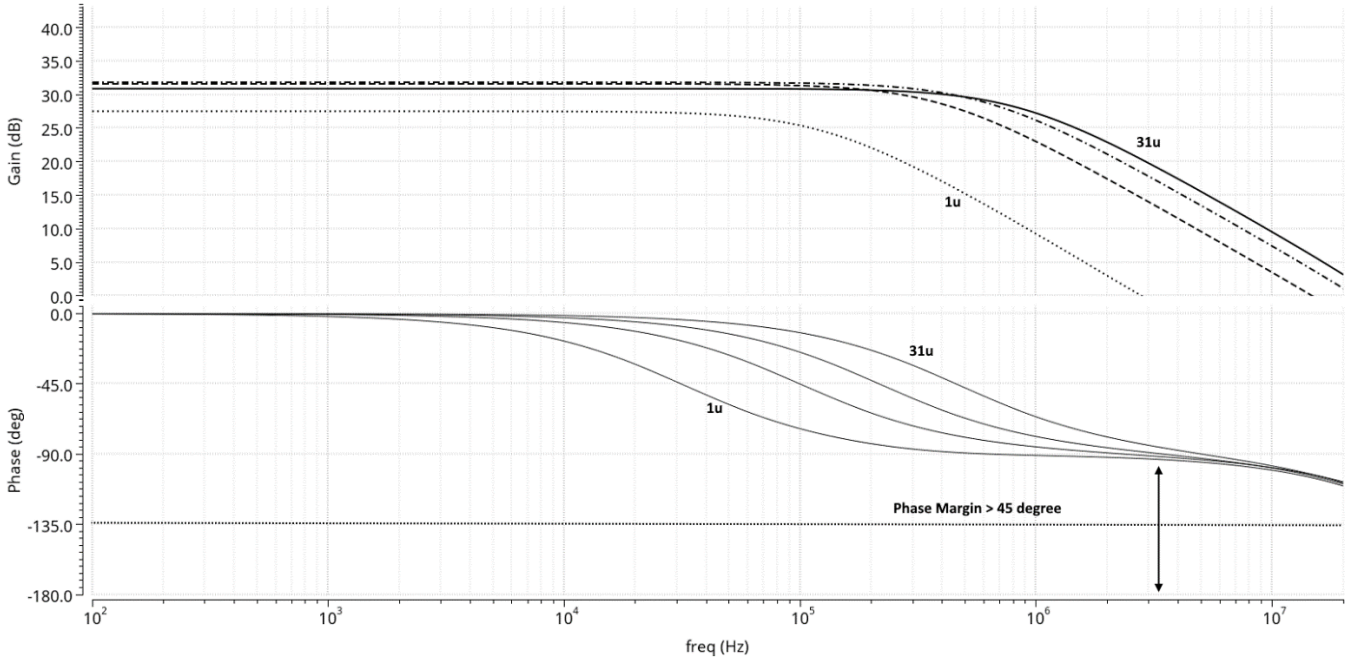

Figure 10 Amplifier gain and phase plots for bias currents of 1, 11, 21, and 31 µA

3.2.3. Low Pass Filter

In both industry and academic designs, G_m-C filters are the most tunable filter topology because G_m-c filters or OTA-C filters are easy to tune via the biasing current of OTAs. Besides, their power consumption is low and they have less phase shift than other filter types. Tuning the overall transconductance value of OTAs provides flexibility during filter design. However, in filter design, transconductance characteristics of the OTAs used in amplifiers are not as linear as desired. In order to achieve linear transconductance or G_m characteristics, linearization techniques such as current division [11] and source degeneration [12] are required. Transconductance of the OTA is the same as the transconductance of the differential PMOS transistors $g_{m1,2}$, which is equal to $\sqrt{2.K_{1,2}.I_b}$. The relationship between input differential voltage V_{id}, G_m, and output current I_o in the linear operating region of OTA is given in equation 3

$$I_o = G_m.V_{id}\sqrt{1-\left(\frac{V_{id}}{2V_{ov}}\right)^2} \quad (3)$$

The transconductance of OTAs can be tuned via biasing current I_{bias} under a vital constraint which is $V_{id} < 2V_{ov}$ for low voltage operations. To obtain more tunable and linear transconductance characteristics and to remove second harmonics, linearization techniques have been applied. So, the source degeneration resistors have been replaced by transistors which are operating in sub-threshold region [13]. Besides, current division method has been applied to linearize the transconductance characteristics of the OTA by adding two input pair transistors to the differential input of the OTA as shown in Figure 11.

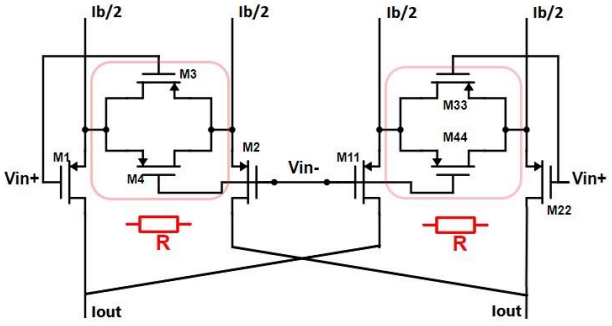

Figure 11 Current division and source degeneration method scheme [13]

$$\frac{G_{m1}}{(V_{ov1})^2} = \frac{G_{m2}}{(V_{ov2})^2} \quad (4)$$

The most important point in this step is to eliminate the third harmonic term of I_o. To achieve this, the transistors $M_{1,2,11,22}$ in Figure 11

have to satisfy the condition in Equation 4. This equation states that these particular transistors have to be matched as much as possible. Therefore, source degeneration method has also been applied to the OTAs because current division method alone is not sufficient to remove the third harmonic term. Unlike in the conventional approach, source degeneration method uses resistors; however, they are replaced by transistors operating in triode region because resistors add parasitics, cause thermal noise, occupy large area, and decrease individual and overall transconductance of OTAs [12]. As shown in Figure 11, when degeneration transistors M_3, M_4, M_{33}, and M_{44} are matched well, it is possible to obtain higher transconductance. The third harmonic term is further decreased after applying both current division and source degeneration methods [13].

The output current and transconductance characteristics of the linearized OTA have been simulated in Cadence and the results are shown in Figure 12. The biasing current from BDAC is tuned from 1 µA to 31 µA, V_{id} is tuned from -0.3 V to 0.3 V, and overall G_m of the linearized OTA varies from 330 µS to 690 µS. Similarly, simulation results for the output current I_{out} is shown in Figure 13. Between -0.3 V and 0.3 V V_{id}, the output current I_{out} has linear characteristics.

The designed OTAs are connected to implement fully differential 5th order Butterworth G_m-C filter as shown in Figure 14. 10 identical OTAs are used in G_m-C filter. All g_{mi} values are equal to each other and C = C_1 = C_2. The cut-off frequency of G_m-C filter can be found as $f = \frac{g_{mi}}{C}$ and the quality factor Q can be calculated as $Q = \frac{g_{mi}}{g_{mi2}}$. The transfer function of the filter is presented in Equation 5, which is the multiplication of a first order transfer function as in Equation 6 and two biquad sections as in Equations 7 and 8.

$$H(s) = H_{1st}(s).H_{2nd_1}(s).H_{2nd_2}(s) \quad (5)$$

$$H_{1st}(s) = \frac{G_{m1}}{G_{m2}+C_s} \quad (6)$$

$$H_{2nd_1}(s) = \frac{\frac{g_{m11}g_{m13}g_{m14}}{g_{m14}\quad C_1C_2}}{s^2+s\left(\frac{g_{m12}}{C_1}\right)+\frac{g_{m13}g_{m14}}{C_1C_2}} \quad (7)$$

$$H_{2nd_2}(s) = \frac{\frac{g_{m21}g_{m23}g_{m24}}{g_{m24}\quad C_1C_2}}{s^2+s\left(\frac{g_{m22}}{C_1}\right)+\frac{g_{m23}g_{m24}}{C_1C_2}} \quad (8)$$

This filter has been implemented and simulated in Cadence. In order to show its tunability, the biasing current from BDAC is swept from 1µA to 31µA to observe various cut-off frequencies. The 1µA biasing current corresponds to the cut-off frequency 15.6 kHz, 31µA bias current corresponds to cut-off frequency 56.7 kHz as shown in Figure 15.

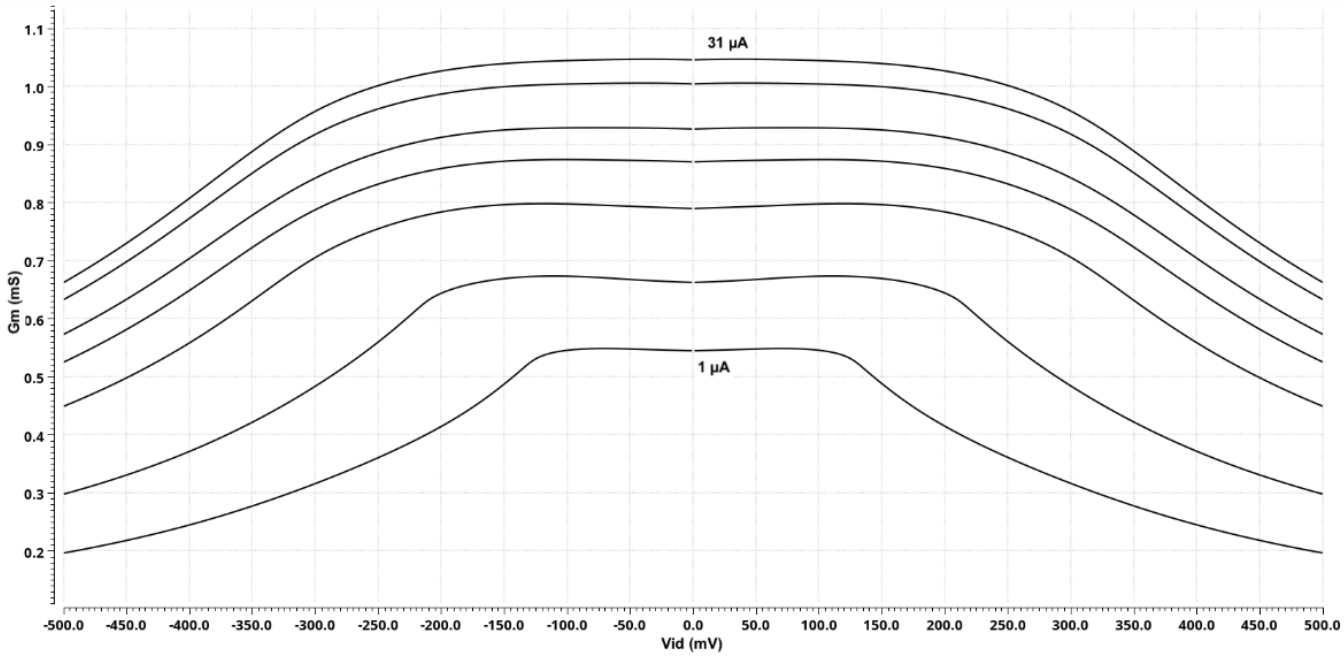

Figure 12 Overall transconductance G_m characteristics of the linearized OTA for bias currents 1, 6, 11, 16, 21, 26, and 31 µA

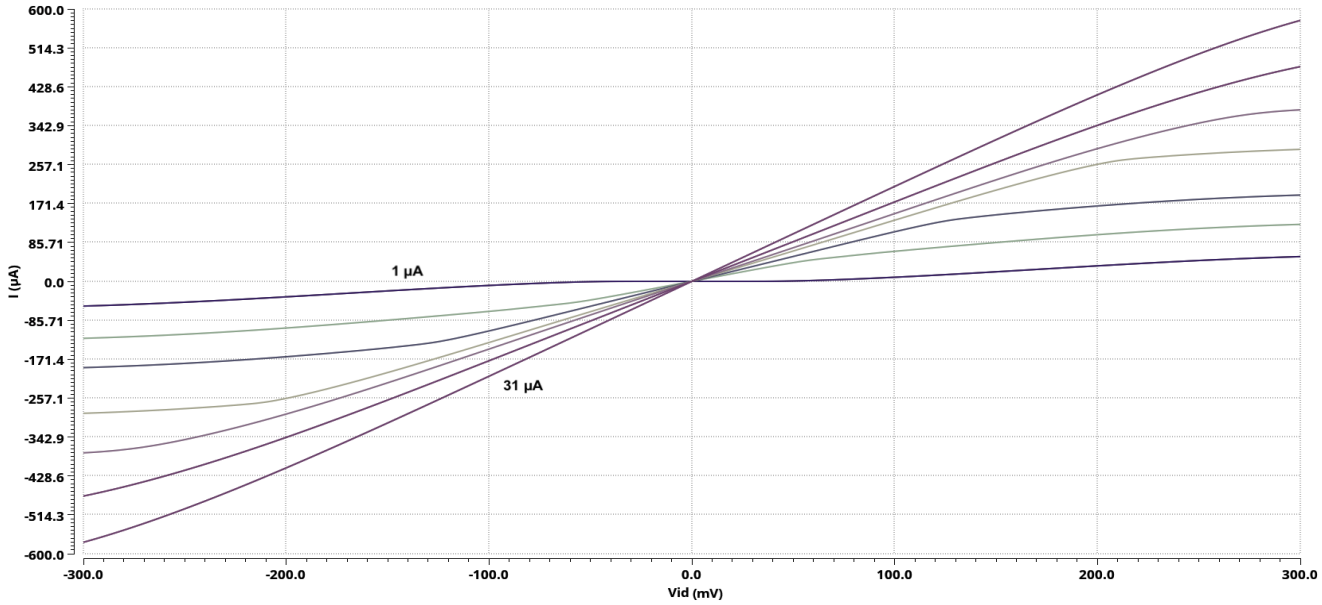

Figure 13 Output current I_{out} characteristic of the linearized OTA for bias currents 1, 6, 11, 16, 21, 26, and 31 µA

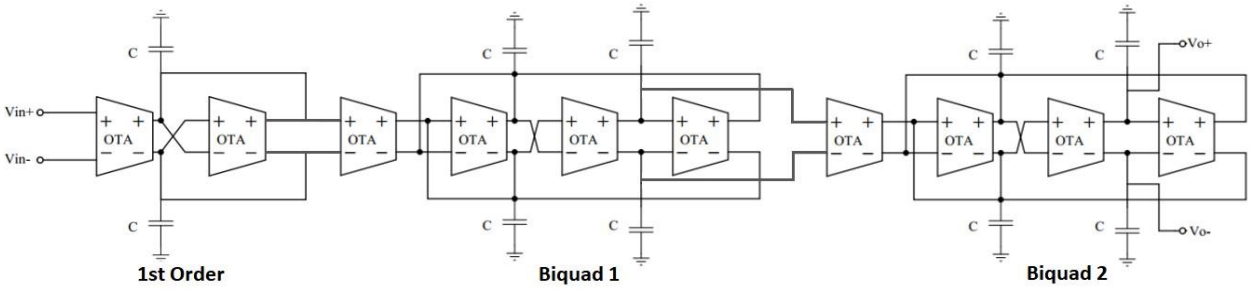

Figure 14 Fully differential 5th order Butterworth G_m-C filter

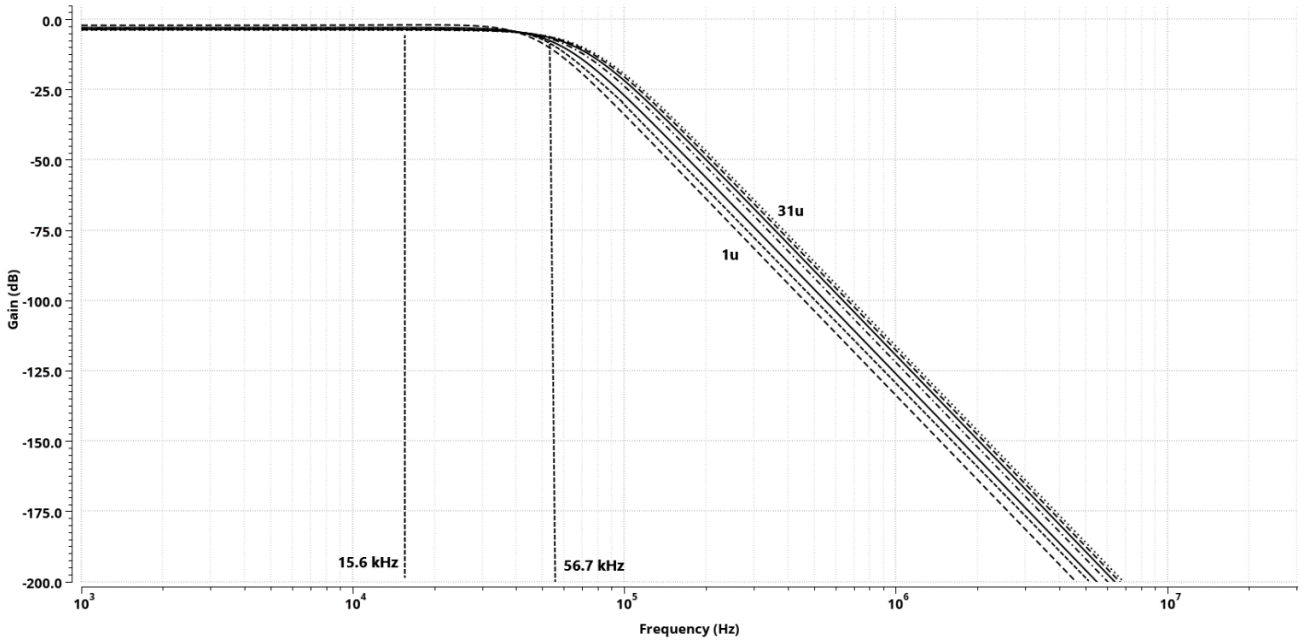

Figure 15 Fully differential 5th order Butterworth G_m-C filter after tuning I_{bias} at 1, 6, 11, 16, 21, 26, and 31 μA

4. SIMULATIONS AND RESULTS

A complete system is depicted in Figure 16, where the chopping amplifier and the fifth order G_m-C low-pass filter is at the center, and a clock signal generator for the choppers is placed to the left. To demonstrate the offset effects, a 1mV DC supply was added as V_{offset} to the positive input terminal of the OPAMP used in the amplifier. The bandgap reference circuit at the bottom left supplies biasing voltages and currents to the entire design via several digitally programmable BDACs. The BDAC below the amplifier generates biasing current for the amplifier, while the remaining 10 BDACs supply biasing currents for the OTAs in the G_m-C filter.

The chopping amplifier topology depicted in Figure 16 has been configured and simulated for three different frequencies, where the applied input signal frequencies are 10 Hz, 100 Hz, and 1 kHz as presented in Figures 17, 18, and 19, respectively; and chopper frequencies (f_{chop}) are selected as 100 times the signal frequencies. Filter cut-off frequencies (f_c) are selected as 500 Hz, 1 kHz, and 25 kHz for the configurations of simulation results in Figures 17, 18, and 19, respectively. The applied input signal is a 1 mV amplitude sine wave for each differential input, the overall signal gain is 25, and the input offset voltage is 1 mV DC in all configurations. All plots presented in Figures 17, 18, and 19 are differential voltages. In these figures, input signal V_{in} is plotted on the top, followed by the first chopper output, which is the input to the amplifier. The third, fourth and fifth plots present the amplifier output, the filter input (i.e., the second chopper output), and the filter output, respectively. This topology eliminates the offset contribution from the amplifier significantly as demonstrated by the fifth plot (i.e., filter output). Without the choppers in the system, the amplifier alone would amplify the input offset as well as the input signal, resulting in a significant DC level shift with respect to the signal amplitude, as demonstrated in the sixth plot. The difference between the fifth (i.e., filter output) and sixth (i.e., V_{out} without chopper) plots proves that the chopper helps amplification of a weak input signal without any DC offset, making the output signal ready for conversion to digital. The filter required by the chopper topology also serves as the anti-aliasing filter required by the analog to digital converters (ADC); thus, it is not really an additional cost to the system.

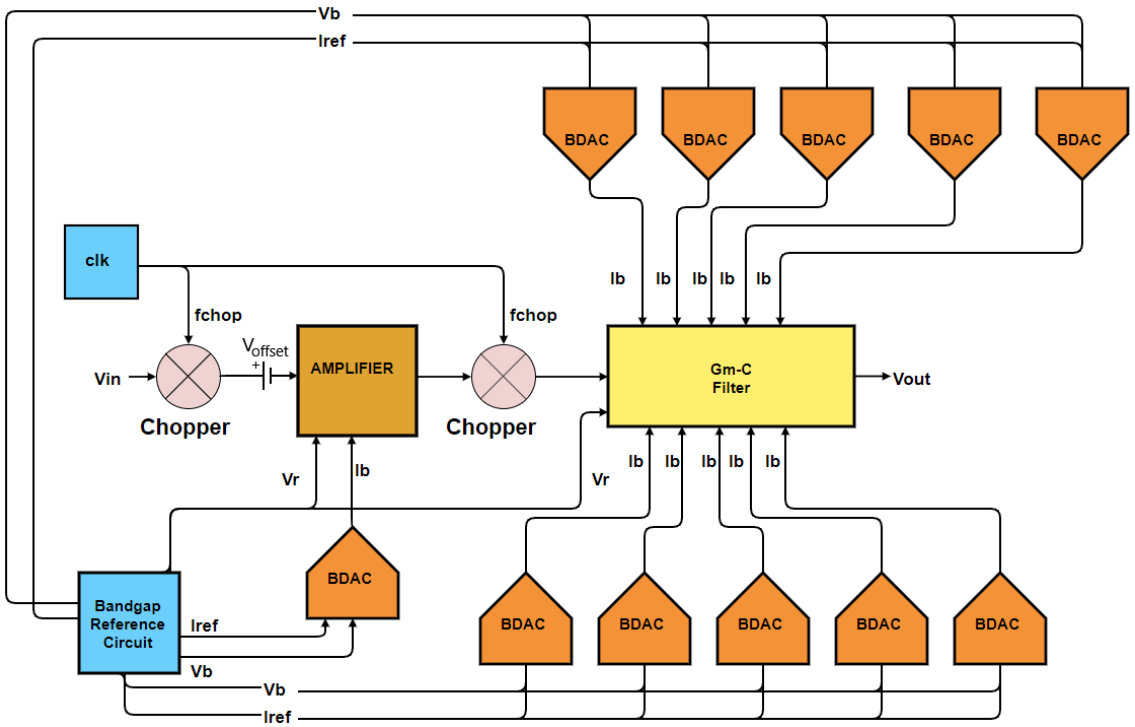

Figure 16 Chopping amplifier topology with tunable G_m-C filter

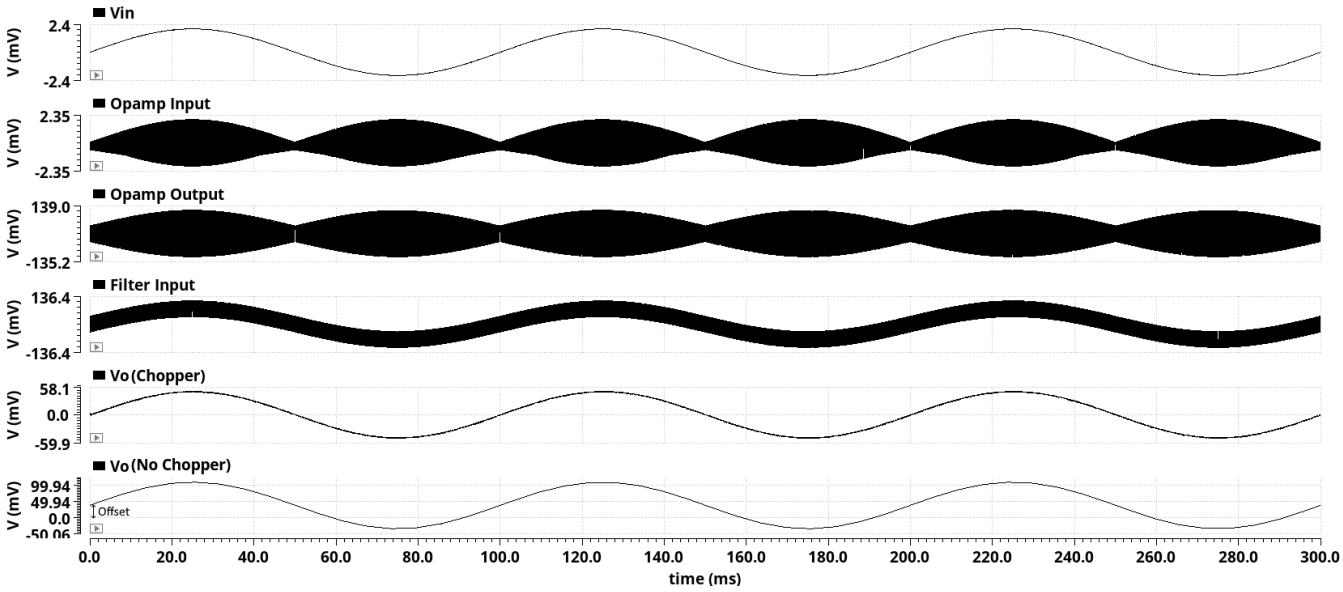

Figure 17 Simulation result of chopping topology with tunable G_m-C filter, f_{input}=10Hz, f_{chop}=1kHz and f_c=500Hz

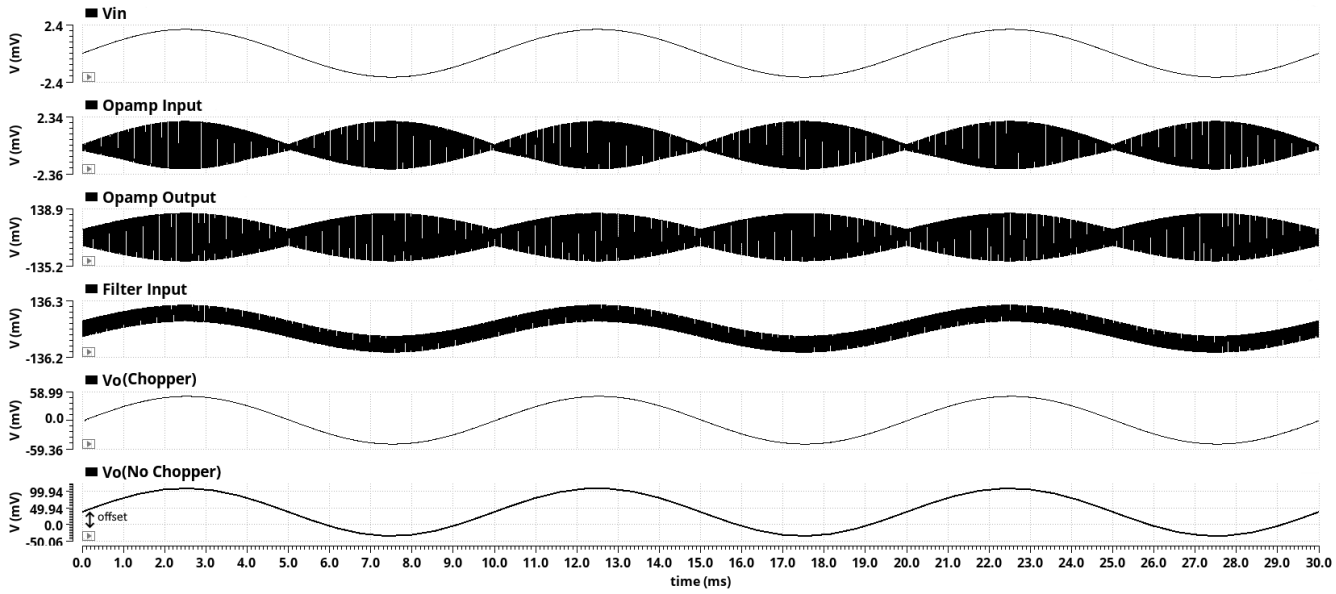

Figure 18 Simulation result of chopping topology with tunable G_m-C filter, f_{input}=100Hz, f_{chop}=10kHz and f_c=1kHz

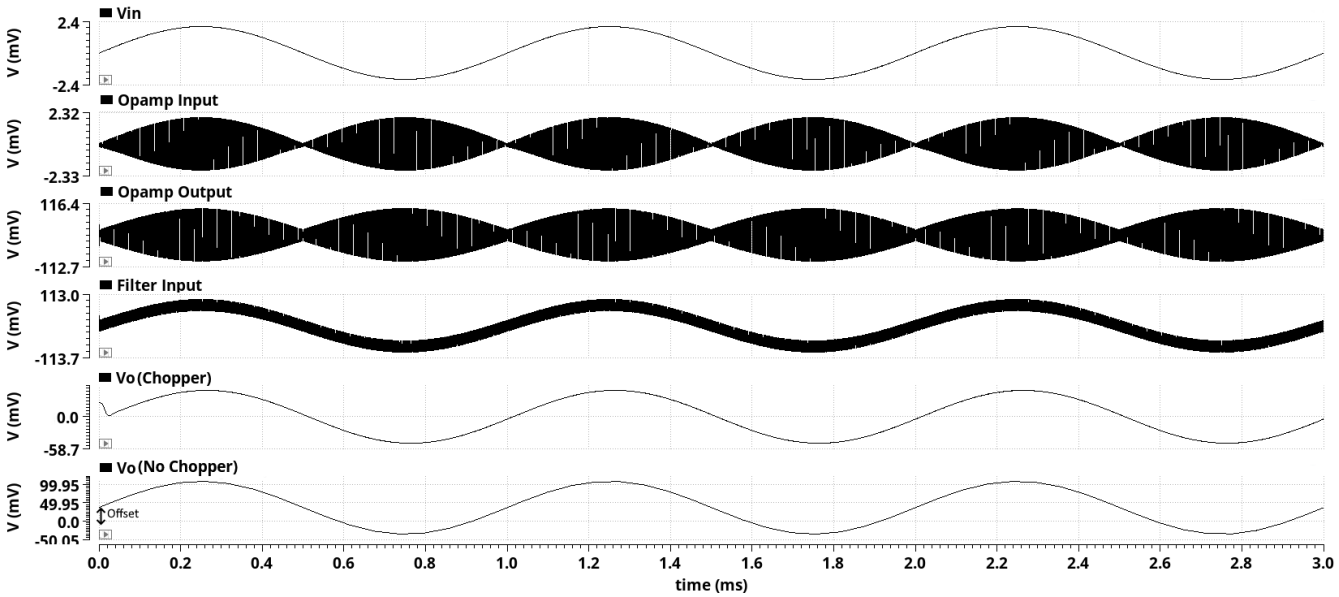

Figure 19 Simulation result of chopping topology with tunable G_m-C filter, f_{input}=1kHz, f_{chop}=100kHz and f_c=25kHz

5. CONCLUSION

There are many physical quantities to measure and as many sensors, which have different interfacing requirements. Designing a new interface for each sensor type and application is an unnecessarily difficult and expensive task. A configurable interface to be used for a wide range of analog sensor outputs has been designed and simulated in UMC 130nm CMOS technology. Chopping amplifier topology has been used as a precision technique to remove the DC offset, which can be a major problem in the processing of low frequency signals. As filter, a fully differential 5th order low pass Butterworth G_m-C filter has been designed from configurable OTAs and connected to the output of the chopping amplifier to obtain a clean signal. Both filter and amplifier are tunable via biasing current supplied from BDAC. The proposed design is self-biased so that all biasing voltages and currents are generated by a bandgap reference circuit. Operating frequency is up to 100 kHz while designed filters are able to operate in a wider range.

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The Declaration of Conflict of Interest/ Common Interest

No conflict of interest or common interest has been declared by the authors.

Authors' Contribution

The first author contributed 40%, the second author 60%.

The Declaration of Ethics Committee Approval

This study does not require ethics committee permission or any special permission.

The Declaration of Research and Publication Ethics

The authors of the paper declare that they comply with the scientific, ethical and quotation rules of SAUJS in all processes of the paper and that they do not make any falsification on the data collected. In addition, they declare that Sakarya University Journal of Science and its editorial board have no responsibility for any ethical violations that may be encountered, and that this study has not been evaluated in any academic publication environment other than Sakarya University Journal of Science.

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