JOURNAL OF ENERGY SYSTEMS

2022, 6(1)

2602-2052 DOI: 10.30521/jes.952692 Research Article

Analysis of positive output buck-boost topology with extended conversion ratio

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Submitted: 15.06.2021
Accepted: 21.01.2022
Published: 31.03.2022

Abstract: In this paper, a new non-isolated buck-boost converter with positive output is designed. This buck-boost converter contains two active switches which operates synchronously. Hence, the control circuit for the given converter is simple. Compared with the conventional buck-boost converter, the newly designed topology has few advantages such as positive output voltage and quadratic voltage gain. Due to the quadratic voltage gain, this converter can achieve wide voltage conversion ratios without the use of extreme (very low or high) duty ratios. The output voltage of this proposed converter is common ground with the input voltage and its polarity is positive. The continuous conduction mode operation (CCM) of the converter is deeply analyzed in steady state conditions. The necessary component design equations are also obtained along with the switching stresses. The MATLAB/Simulink software is used to design and simulate the proposed converter. The simulated results as well as the comparisons are provided to evaluate the effectiveness of the proposed buck-boost converter.

Keywords: *Buck-Boost, Continuous Conduction Mode (CCM), Positive output voltage, Quadratic voltage gain*

Cite this paper as: Bandi, N.R., Kosika, S.P., Gadam, M.P., Banoth, J., Banoth, A., & Goud, B.S., Analysis of positive output buck-boost topology with extended conversion ratio. *Journal of Energy Systems* 2022; 6(1): 62-83, DOI: 10.30521/jes.952692

1. INTRODUCTION

As is well known, in this sophisticated era switching mode power supply is the essence of power conversion technology. Number of converter configurations have been anticipated based on the switching mode power supply. Fields like aviation, railways, communication system, household appliances, industrial devices, electric power run on the origin of switching mode power supply [1-4]. Buck converter and Boost converter have importance due to its unsophisticated structure and elevated efficiency, but are left out due to their restricted applications in conditions of low or high output voltages [5-7].To overcome these applications few basic converters like Luo converter, Cuk converter, Sepic converter, Quadratic type converters have commenced.

Quadratic topologies can overcome the desired voltage gain with limited no. of switches but has bad efficiency [8-11]. By engaging the voltage lift process converters such luo converters and interleaved converters can obtain high voltage gain, but there will be a progressive increase in cost, complexity, losses [12-13]. By inclusion of various-switched networks to basic converters, substantial voltage gains can be gained at the price of complicating the control techniques and the cost of the converter [14-16]. Compared with the previous converters there are bucking and boosting converters which not only reduce voltages but also govern output voltages or load changes which function in well-known applications like vehicle electronic devices, portable electronic devices, etc. The routinely utilized buck-boost topology with simple structure and great efficiency has limitations of inadequate voltage gain, negative output voltage, floating power switches and discontinuous currents in input and output.

There are 3 other rudimentary non-isolated topologies Cuk, Sepic, Zeta converters which have the capacity to buck or boost the voltages. However, these downsides are non-ignorable. Meanwhile, the quadratic converter which was proposed by Maksimovic may attain voltage gain $D^2/(1-D)^2$ but could only work in buck condition due to clamping of output voltage to input voltage of D_1 and D_2 diodes and duty cycle being larger than 0.5[17]. On the foundation of Cuk converter, a novel buck-boost topology, with the smaller number of ripples in the output voltage, a negligible radio frequency incursion with the shared ground power switch is projected [18]. But it has its shortcomings like the seventh order convoluted circuit configuration, limited voltage gain and both input and output terminals not sharing the common ground [19].

Hwu and Peng anticipated a new buck-boost configuration by amalgamating the basic synchronous converter with the KY converter which gives substantial outcomes like positive output voltage, continuous output current and operates in Continuous Conduction Mode and has no right-half plane zero. Tactlessly, the converter desires to execute in the inclusive range of output voltage and the duty cycle isn't adequate. For thermoelectric generator a cascade connected buck-boost converter with the current source and current sink is put in where the voltage power is however confined [20]. The duty cycles need to be run at extremely low or high in the edict to reach high voltage step-up or step-down gains this condition is too firm to reach due to practical constraints. Henceforth, to overcome all the constraints of buck-boost converter new topologies are to be inherited to satisfy the rapid growth and increasingly needs in industrial applications.

As renewable systems generate a low number of voltages they need to be stepped up when they are fed to the dc-ac inverter. Hence, there is the surge in utilization of high voltage gain converters which are used in applications like fuel cells, Solar and Wind energy systems [21]. Furthermore, the Voltage lift circuit technique may also be employed by the converters which may produce the high voltage conversion ratios for converters like luo converters and it has its non-ignorable limits. It influences

capacitors, the load resistance and the current start increasing which results in the disruptions in the output voltages of the system. They also disrupt the borders of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) margins which consequently impacting the efficiency of converters [22].

Conventional n-cell cascade connections can also be developed to achieve higher voltage ratios for dc-dc converters, which includes adding transformers to the circuits, which has adverse implications by increasing the structure's complexity and cost. It triggers a slew of energy-related issues, and power switching generates voltage spikes [23]. A novel proposed buck-boost topology is being discussed in order to overcome all of these difficulties or to reduce the majority of them to zero.

In this study, by the cascade combination of two traditional synchronous buck-boost converters a newfangled non-isolated buck-boost converter is recommended. The great eminence of the proposed buck-boost converter is that it has the quadratic voltage gain than the customary buck-boost configuration so that it can set off in a wide range of output voltage achieving a high or low voltage gain deprived of the extreme duty cycle. Furthermore, it has positive polarity and has a zero ground with input voltage.

2. STRUCTURE AND CONFIGURATION OF PROPOSED BUCK-BOOST CONVERTER

The circuit configuration of our proposed buck-boost converter is shown in Fig. 1. The converter has 2 power switches S_a and S_b which are synchronously operated, twain diodes D_a and D_b, twain inductors L_1 and L_2, twain capacitors C_1 and C_0 and single load resistance *R*.

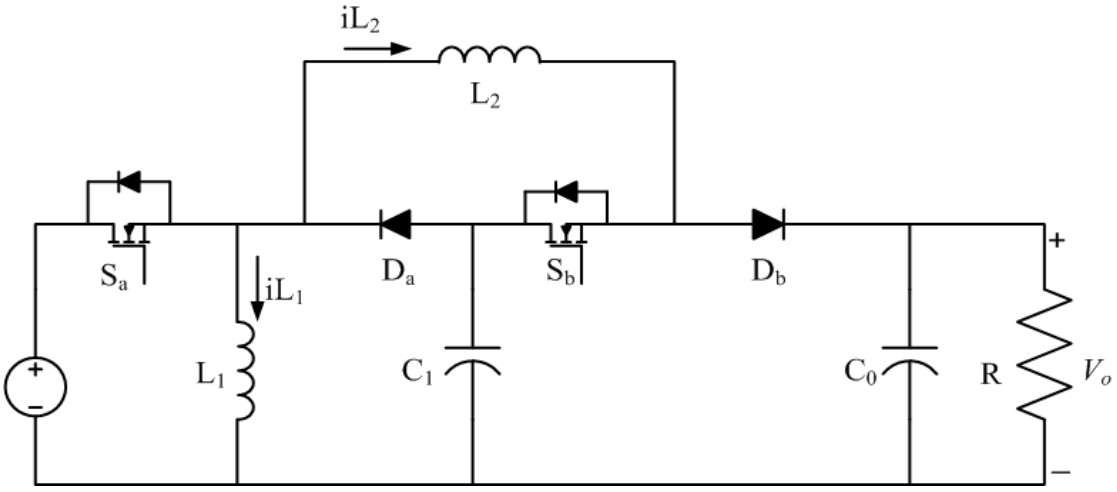

Figure 1. Newly Proposed buck-boost converter.

Figs. 2(a,b) show the possible states of the proposed buck-boost converter when operated in continuous conduction mode (CCM).

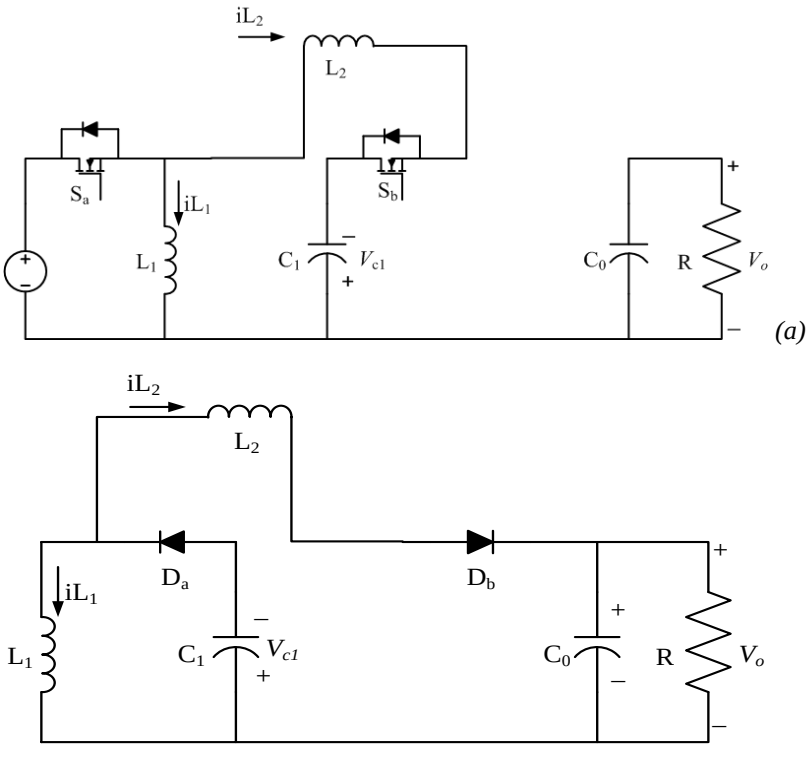

Figure 2. Equivalent circuit of proposed buck-boost converter in (a) mode 1 and (b) mode 2.

Fig. 2(a) gives the mode1 operation that is, switches S_a and S_b are turned on and diodes D_a and D_b are turned off. Simultaneously, affecting the inductors L_1 and L_2 to magnetize and the capacitors C_1 and C_0 to discharge and here R is considered as the resistive load or the output voltage of the newly proposed buck-boost converter.

Fig. 2(b). shows the second mode of operation where the switches S_a and S_b are turned off and diodes D_a and D_b conducting resulting the inductors L_1 and L_2 to demagnetize and the capacitors C_1 and C_0 to get charged of the newly proposed buck-boost topology.

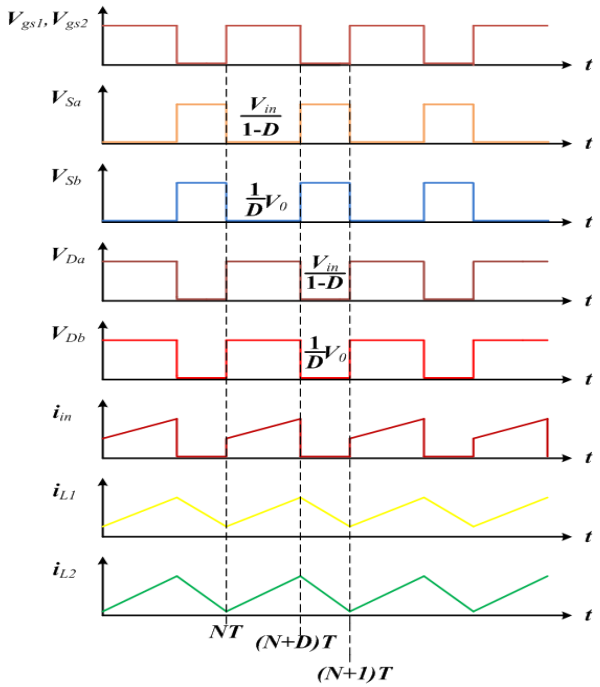

Figure 3. CCM time-domain waveforms of proposed buck-boost converter.

Fig. 3 indicates the typical time-domain waveforms of our proposed buck-boost converter. In order to deflate the circuit deduction and analysis, we suppose the converter is operated in the steady state mode. Sufficiently large capacitors are used to maintain a constant voltage among the components.

3. OPERATING PRINCIPLES

When our non-isolated buck-boost converter is operated in Continuous Conduction Mode (CCM) there are 2 possible modes that are, mode 1 and mode 2.

3.1. Mode 1 Operation of Proposed Buck-Boost Converter

Through the time interlude (NT<t, (N+D) T), the power switches S_a and S_b are turned on and the diodes D_a and D_b are reverse biased i.e.; turned off. As shown in Fig. 2(a) the input voltage (V_{in}) magnetizes the L_1 inductor and input voltage (V_{in}) and the charge pump capacitor (C_1) magnetizes the L_2 inductor.

The obtained equations are given as:

$$V_{L1} = V_{in} \tag{1}$$

$$V_{L2} = V_{in} + V_{C1} \tag{2}$$

3.2. Mode 2 Operation of Proposed Buck-Boost Converter

The switches S_a and S_b are turned off through the interlude ((N+D) T<t<(N+1) T) and diodes D_a and D_b are turned on i.e., forward biased. From Fig. 2(b). Due to diode D_a the L_1 releases the stored energy to capacitor C_1. Simultaneously the L_2 inductor energy is transferred to capacitor C_1, output capacitor C_0 and resistive load R through the diodes D_a and D_b.

Thus, the corresponding equations are given as:

$$V_{L1} = -V_{C1} \tag{3}$$

$$V_{L2} = -(V_{C1} + V_0) \tag{4}$$

From Eqs. 1,3 by applying voltage second balance principle. The voltage across the pump capacitor C_1 is given as:

$$V_{C1} = \frac{D}{1-D} V_{in} \tag{5}$$

By making use of voltage second balance principle, an inductor L_2, from Eqs. 2,4,5. The voltage gain M(D) is given as:

$$M = \frac{V_0}{V_{in}} = \frac{D^2}{(1-D)^2} \tag{6}$$

Here, D is the duty cycle, the proportion of switch turn on time to the whole switching cycle. The propounded buck-boost converter can step up and step down the input voltage with a duty cycle greater than and less than 0.5, respectively with the better theoretical and the practical values than other conventional converter topologies.

4. VOLTAGE STRESSES

In stepdown, V_{C1} is less than V_{in} and in step up mode V_{C1} is less than V_0. Voltage stress on C_1 is small and small sized capacitor is chosen in order to reduce the power losses.

$$V_{C1} = \frac{D}{1-D} V_{in} = \frac{1-D}{D} V_0 \tag{7}$$

The voltage stresses on switches and diodes are given as:

$$V_{S1} = \frac{1}{1-D} V_{in} = \frac{1-D}{D^2} V_0 \tag{8}$$

$$V_{S2} = \frac{D}{(1-D)^2} V_{in} = \frac{1}{D} V_0 \tag{9}$$

$$V_{D1} = \frac{1}{1-D} V_{in} = \frac{1-D}{D^2} V_0 \tag{10}$$

$$V_{D0} = \frac{D}{(1-D)^2} V_{in} = \frac{1}{D} V_0 \tag{11}$$

The voltage stresses of switches on the traditional buck boost converter are identical to the voltage stresses on the switch S_a and diode D_a of the proposed buck boost configuration with the same input voltage and voltage stresses of diodes of conventional buck boost topology matches to the voltage stresses of switch S_b and diode D_b of the proposed buck boost converter with the same input voltage.

5. CURRENT STRESSES

The input power and output power are considered equal i.e.:

$$V_{in} I_{in} = V_0 I_0 \tag{12}$$

The currents are given as,

$$\frac{I_{in}}{I_0} = \frac{(1-D)^2}{D^2} \tag{13}$$

From Ohm's law,

$$V_0 = R I_0 \tag{14}$$

Using the ampere second balance principle on capacitor C_0, we get; $I_{D0} = I_0$ The DC currents I_{L1}, I_{L2}, I_{in} and I_0 are given as

$$I_{in} = D(I_{L1} + I_{L2}) \tag{15}$$

$$I_0 = (1-D)I_{L2} \tag{16}$$

From the obtained Eqs. 6,13-16.

$$I_{L1} = \frac{D^2(2D-1)V_{in}}{(1-D)^4R} \tag{17}$$

$$I_{L2} = \frac{D^2V_{in}}{(1-D)^3R} \tag{18}$$

The current stresses of switches and diodes are given as:

$$I_{Sa} = D(I_{L1} + I_{L2}) = \frac{D^4V_{in}}{(1-D)^4R} \tag{19}$$

$$I_{Sb} = DI_{L2} = \frac{D^3V_{in}}{(1-D)^3R} \tag{20}$$

$$I_{Da} = (1-D)(I_{L1} + I_{L2}) = \frac{D^3V_{in}}{(1-D)^2R} \tag{21}$$

$$I_{Db} = (1-D)I_{L2} = \frac{D^2V_{in}}{(1-D)^2R} \tag{22}$$

From the above Eqs. 19-22 the current stresses of power switch S_b and diode D_a are equal to the power switch currents of customary buck-boost topology with the identical output current and the I_0 matches the diode D_b current ripple values which is identical as the current stress of diode in the customary buck boost converter, considering the current stress of the power switch S_a of propounded buck boost converter is high.

6. INDUCTOR CURRENT RIPPLES

The inductor current ripples, are given as;

$$\Delta i_{L1} = \frac{V_{L1}}{L_1}DT_S = \frac{DV_{in}}{L_1 f_s} \tag{23}$$

$$\Delta i_{L2} = \frac{V_{L1}}{L_2}DT_S = \frac{DV_{in}}{(1-D)L_2 f_s} \tag{24}$$

Here, f_s is switching frequency.

The relevant inductors for practical use can be calculated from Eqs. 23,24 if the inductor current ripples, the input voltage V_{in} , duty cycle D, and f_s are known.

7. CAPACITOR VOLTAGE RIPPLES

The voltage ripples across the pump capacitor C_1 and output capacitor C_0 that is $\Delta V_{C1}, \Delta V_{C0}$ are given as follows:

$$\Delta V_{C1} = \frac{\Delta Q}{C} = \frac{DV_0}{(1-D)RC_1 f_s} \quad (25)$$

$$\Delta V_{C0} = \frac{\Delta Q}{C} = \frac{DV_0}{RC_0 f_s} \quad (26)$$

Based on Eqs. 25,26 the capacitors C_1 and C_0 can be calculated if the capacitor voltage ripples, the output voltage V_0, the duty cycle Resistive load R, switching frequency (f_s) need to be known.

8. COMPARISON TABLE

Table 1 shows the comparison among the different types of converters, Luo converter [24], Cuk converter [15], IB converters [25], KY converter [8], Traditional buck-boost configuration [5] and proposed buck-boost converter. The voltage stresses of diodes and the voltage stresses of switches, the voltage gain and the number of components used are being compared and the corresponding graphs are also plotted among these parametric values.

The graphs of voltage gain and voltage stresses Vs duty cycle are mentioned in Figs. 4-6. Among all the converters the proposed buck-boost converter has high voltage gain and the minimum number of stress which can be operated in divergent values of output voltage with identical input voltage value and the proposed converter shows the better graphical values for the compared components among all other given converter parameters. Figs. 4-6 show the curves of the duty cycle against the voltage gain and voltage stresses of diodes and voltage stresses of switches respectively.

Table 1. Comparison among the converters.

References	**Parameters**						
	No. Switches	No. Diodes	No. Inductors	No. Capacitors	Switch Voltage Stresses (V_S)	Diode Voltage Stresses (V_D)	M(D)
LUO Converter	1	1	2	2	V_0	V_i+V_0	D/1-D
Cuk Converter	1	2	3	4	V_1/1-D	V_1/1-D	1-D/2D
Traditional buck boost Converter	1	1	1	1	1/1-D	1/1-D	D/1-D
IB^2 Converter	1	3	2	2	(1+D) V_{in}	V_{in}	D^2
IB^3 Converter	1	3	2	2	(1+D) V_{in}	V_{in}	D^2
IB^4 Converter	1	3	2	2	V_{in}/1-D	V_{in}	$-D^2$/1-D
KY Converter	2	1	2	3	1	1	2D
Proposed Converter	2	2	2	2	V_{S1}=1/1-D V_{S2}=D/(1-D)^2	V_{D1}=1/1-D V_{D2}=D/(1-D)^2	D^2/(1-D)^2

In Fig. 4, the Voltage gain M(D) of the proposed buck boost converter is far high comparatively with Cuk, Luo, KY, IB, and traditional buck boost converters.

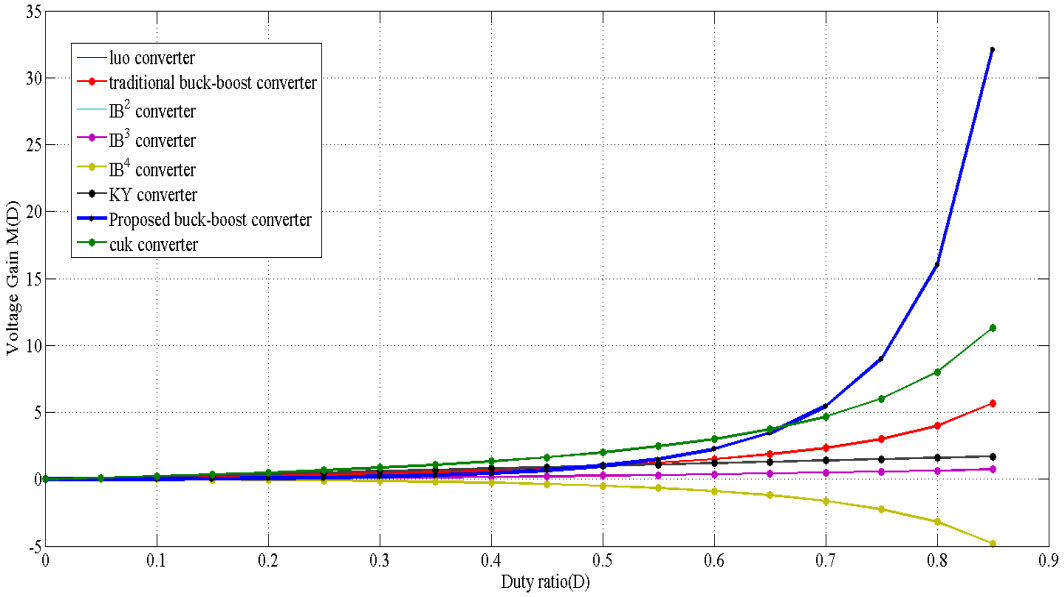

Figure 4. Comparison of Voltage conversion ratios of different converters.

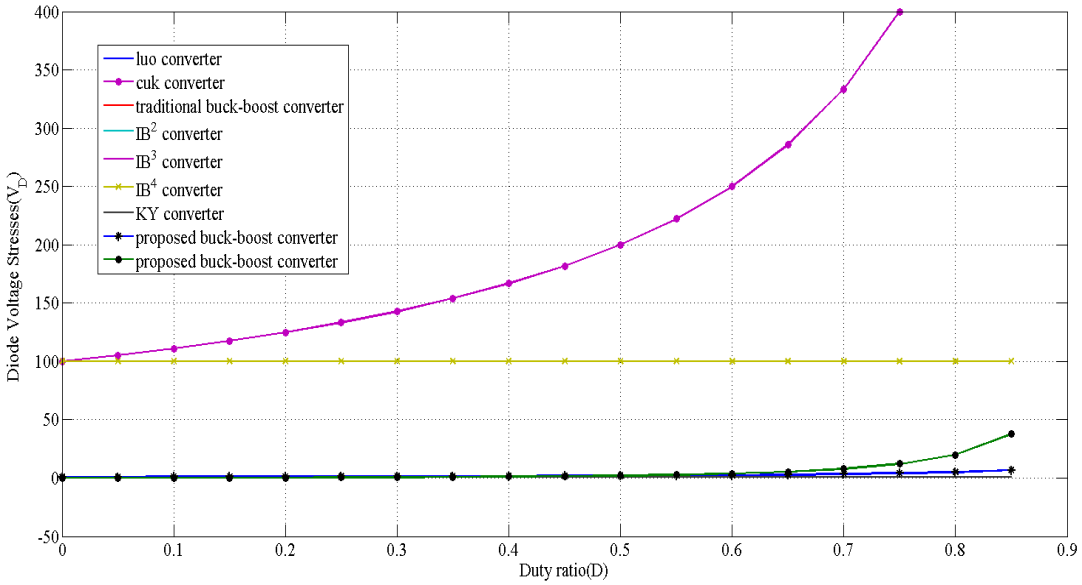

Figure 5. Comparison of Diode Voltage Stresses of different converters.

In Fig. 5, the diode voltage stresses of C_{uk} converter and IB^4 converter are very large, which reduces the outcome of the converter whereas the proposed buck boost converter has a very low diode voltage stresses which shows the less ripple voltage and the better efficient values.

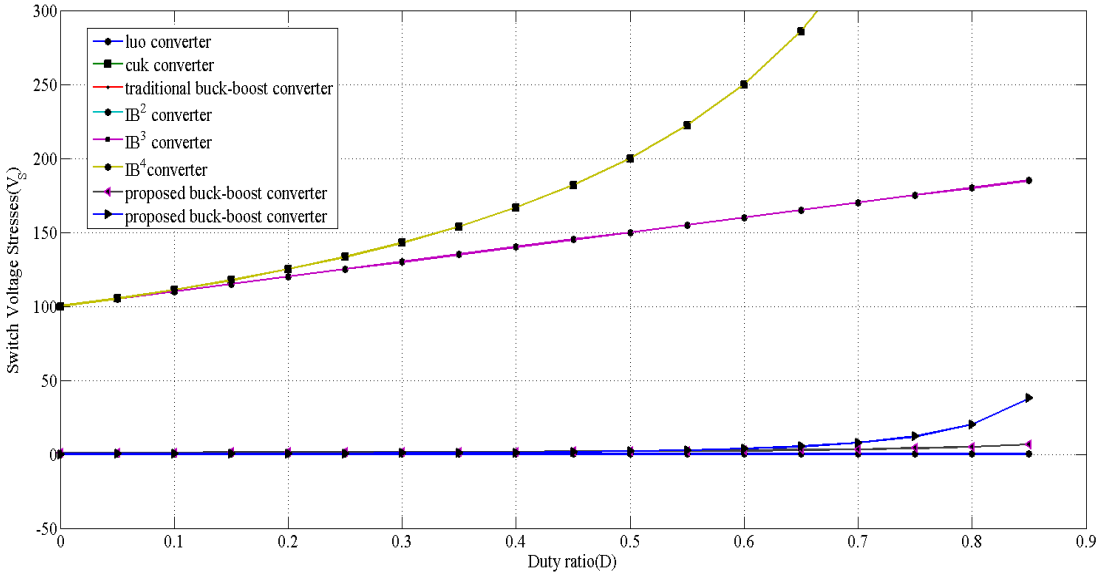

Figure 6. Comparison of Switch voltage stresses of different converters.

Fig. 6 shows the switch voltage stresses where IB converters have a rapid increase of voltage stresses which results in the flash over, spark over of the converters and damages the converter. In general, of all the different converters the proposed buck boost topology has the best performance with high voltage gain and low voltage stresses.

9. MATLAB SIMULATIONS AND RESULTS

The proposed non-isolated buck-boost converter (see Fig. 1) is contrived in the MATLAB Simulink environment. By using the design analysis presented, the components value of input and output voltages, the switching frequency, output load, duty cycle are given in Table 2.

Table 2. Simulated Parameters

Components	Step up mode
Input voltage V_{in}	20 V
Output voltage V_O	200 V
Switching frequency f	50KHZ
Output load R	400 ohms
Duty cycle D	0.759
Inductor $L_1 = DV_{in}/\Delta iL_1 f_s$	303.6µH
Inductor $L_2 = DV_{in}/(1\text{-}D)\ \Delta iL_2 f_s$	1.259mH
Capacitor $C_1 = DV_0/(1\text{-}D)R\Delta V_{c1} f_s$	10.49µF
Capacitor $C_0 = DV_0/R\Delta V_{c0} f_s$	2.53µF
ΔiL_1	1A
ΔiL_2	1A
ΔV_{C1}	3V
ΔV_{C0}	3V

The inductors L_1, L_2 and the capacitors C_1 and C_0 values are considered as L_1=303.6 μH, L_2=1.259 mH, C_1=10.49 μF, C_0=2.53 μF. Similarly, the capacitor voltage ripples are C_1 (ΔV_{C1}) and C_0 (ΔV_{C0}) are considered as 3V each respectively. The current ripples of the L_1 inductor (Δi_{L1}) and L_2 inductor (Δi_{L2}) are given 1A each respectively.

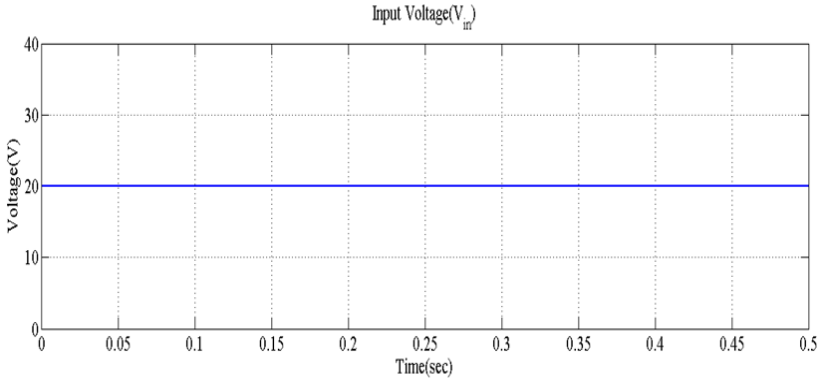

Figure 7. Simulated waveform of input voltage.

Fig. 7 represents the simulated waveform of input voltage for the proposed buck-boost converter which is a constant voltage value of 20V.The waveform is obtained between the input voltage and the time axis.

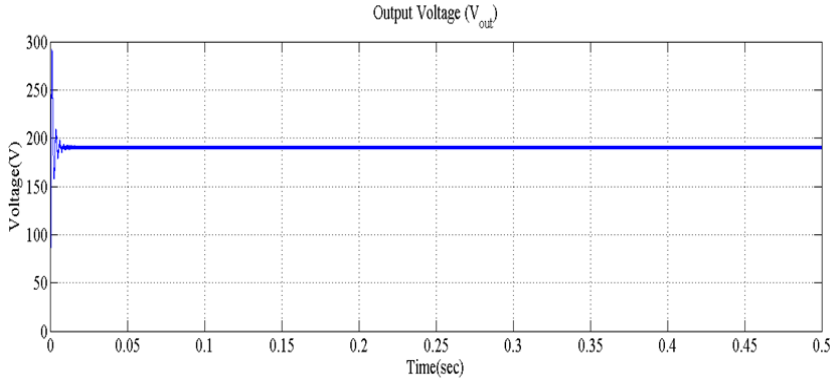

Figure 8. Simulated waveform of output voltage.

Fig. 8 gives the simulated waveform of the output voltage for the proposed buck-boost value converter and the value obtained is 192.3 V which is nearer to the assumed value of 200V. The simulated waveform is considered with time on x-axis and the voltage on y-axis. It reaches the constant value of 192.3 V between 0-0.05 s.

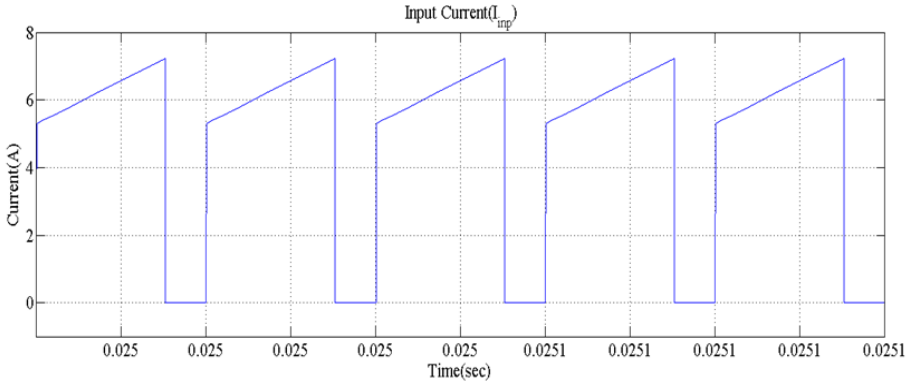

Figure 9. Simulated waveform of input current.

Fig. 9 represents the simulated waveform of input current of the proposed topology. The current value is obtained as 4.84 A and the output current obtained is in discontinuous mode. The y-axis is taken as current and the x-axis is considered as time proportion. The output current has the sawtooth waveform. Upon simulation of two series connected buck-boost converters these waveforms are obtained.

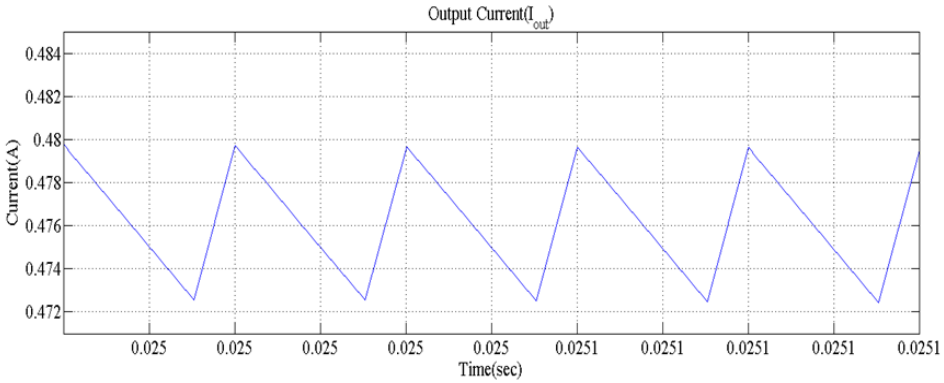

Figure 10. Simulated waveform of output current.

Fig. 10 shows the output current waveform of the newly proposed configuration which was obtained upon the simulation of the circuit. The waveform has the sawtooth formation and the output current obtained for the D value of 0.759 is given as 0.48A and the simulation is done in the continuous conduction mode. Output current values are required for the tabular values.

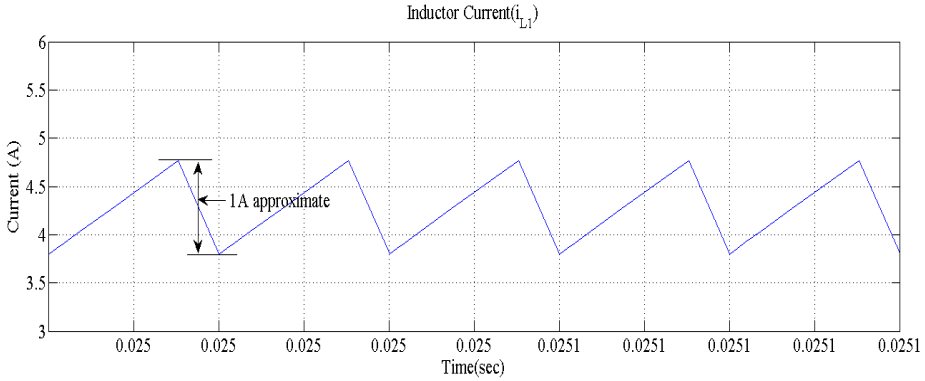

Figure 11. Simulated waveform of first inductor current.

Fig. 11 represents the first inductor current value which is obtained upon the simulation of the newly proposed buck-boost converter and the current ripple factor for the inductor L_1 is taken as 1A.The average current value obtained for the i_{L1} is observed as 4.422A

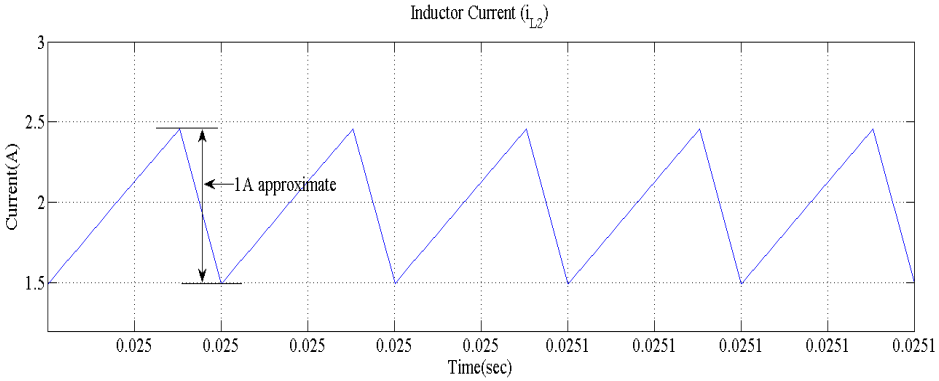

Figure 12. Simulated waveform of second inductor current

Fig. 12 represents the second inductor current value, which is obtained upon the simulation of the newly proposed converter and the current ripple factor for the inductor L_2 is taken as 1A. The average current value obtained for the i_{L2} is observed as 2.48A. For both the inductor the average current values are considered.

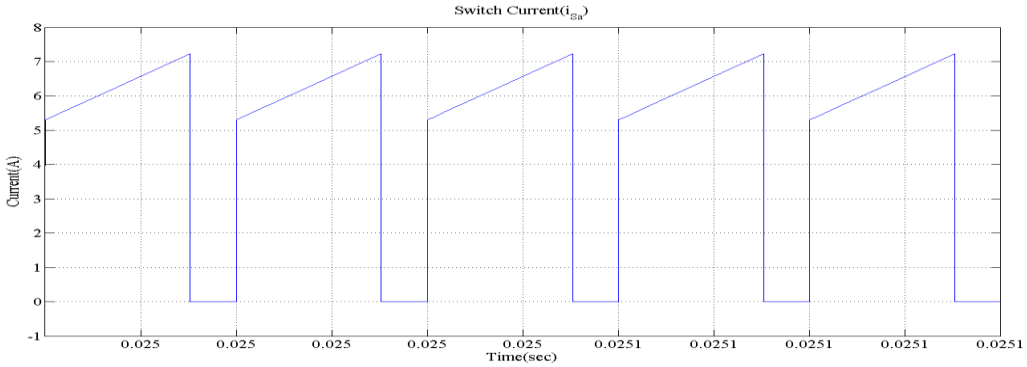

Figure 13. Simulated waveform of first power switch current.

Fig. 13 represents the simulated waveform of the current of the power switch S_a which is obtained upon the simulation of the newly proposed converter and the current values of the switch is given as 5.4A.The y-axis is considered as first switch current and the x-axis is taken as the time proportion of 0.025 s to 0.0251s.

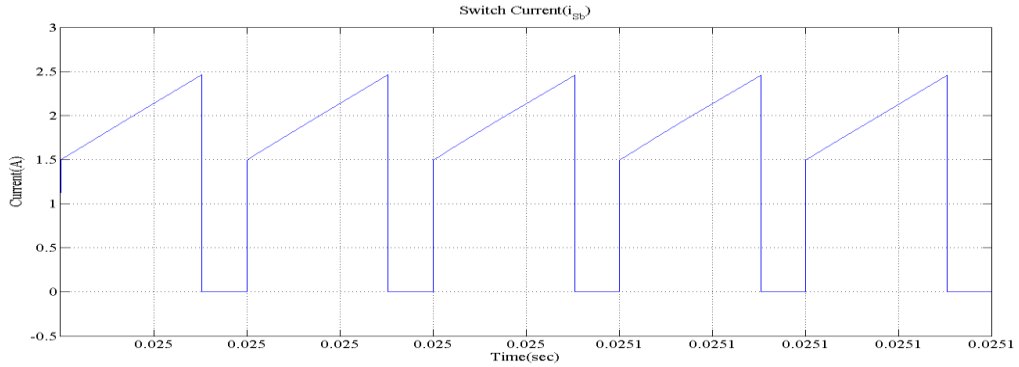

Figure 14. Simulated waveform of second power switch current.

Fig. 14 represents the simulated waveform of the current of the second power switch S_b which is obtained upon the simulation of the newly proposed configuration and the current values of the switch is given as 1.5 - 2.5 A. The y-axis is considered as first switch current and the x-axis is taken as the time proportion of 0.025 s to 0.0251 s.

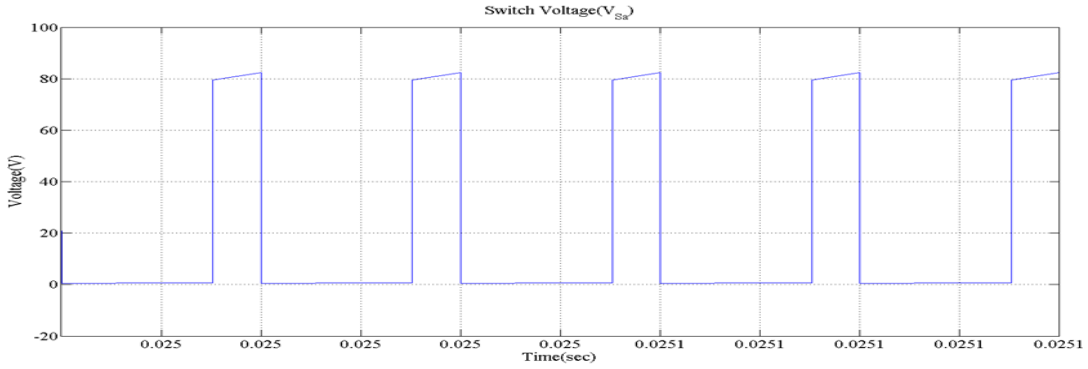

Figure 15. Simulated waveform of first power switch voltage.

Fig. 15 illustrates the simulated waveform first power switch voltage which is 82.5 V obtained upon the simulation of newly proposed topology. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V.

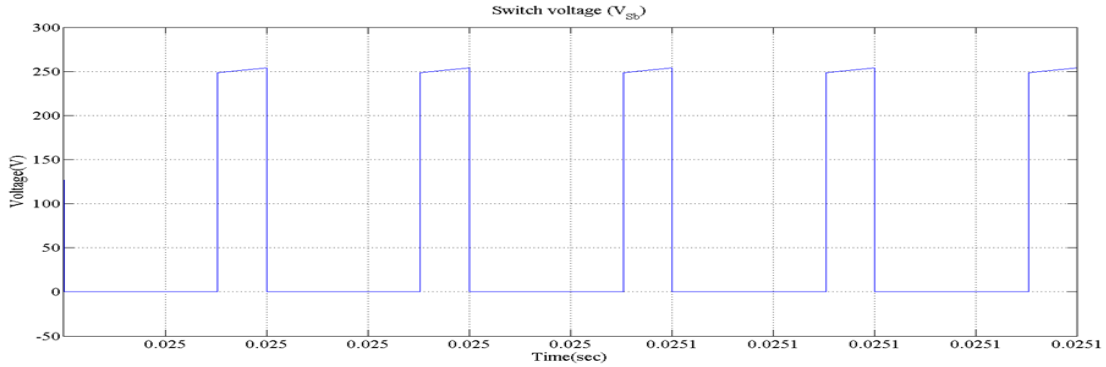

Figure 16. Simulated waveform of second power switch voltage.

Fig. 16 illustrates the simulated waveform of second power switch voltage which is 250.5 V obtained upon the simulation of newly given buck-boost configuration. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis.

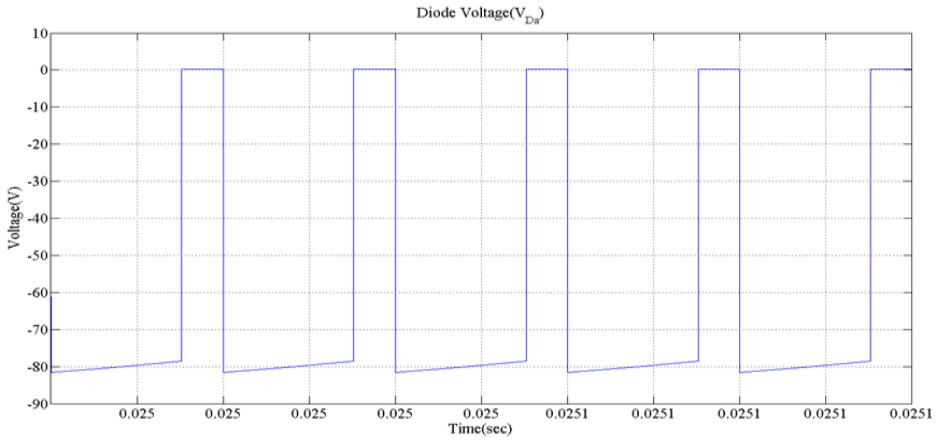

Figure 17. Simulated waveform of first diode voltage

Fig. 17 illustrates the simulated waveform first diode voltage which is 82.5 V obtained upon the simulation of newly proposed topology. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V.

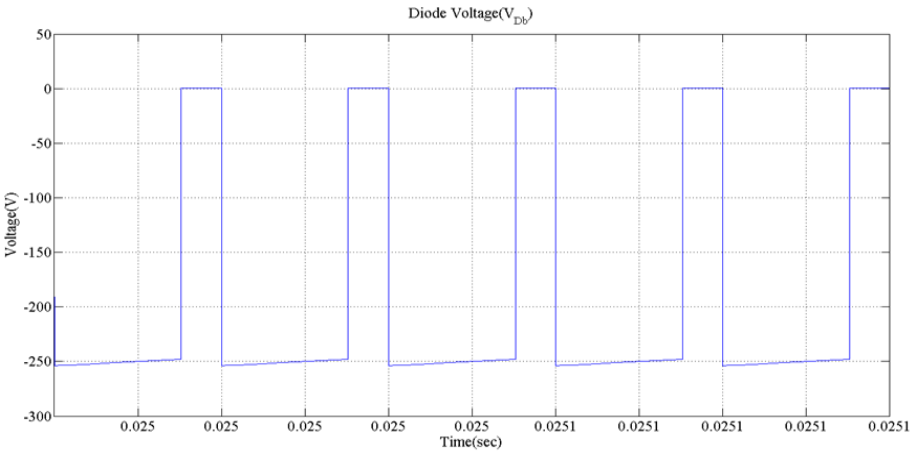

Figure 18. Simulated waveform of second diode voltage.

Fig. 18 illustrates the simulated waveform second diode voltage which is 250.5 V obtained upon the simulation of newly proposed buck-boost configuration. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V.

Fig. 19 illustrates the simulated waveform first diode current, which is 7.2 A obtained upon the simulation of newly proposed converter. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The current is plotted on y-axis with an interval of 1ampere.

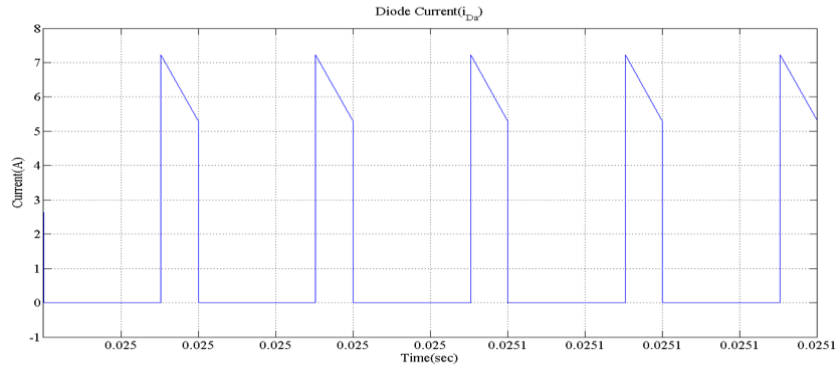

Figure 19. Simulated waveform of first diode current

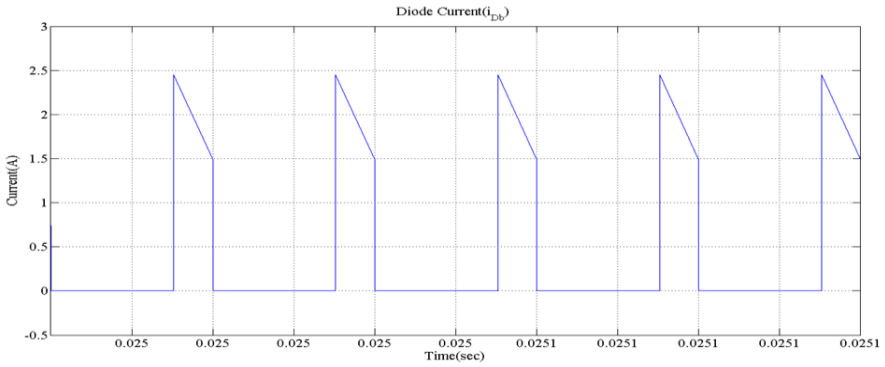

Figure 20. Simulated waveform of second diode current.

Fig. 20 illustrates the simulated waveform second diode current which is 2.4 A obtained upon the simulation of newly proposed buck-boost converter. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The current is plotted on y-axis with an interval of 0.5 A.

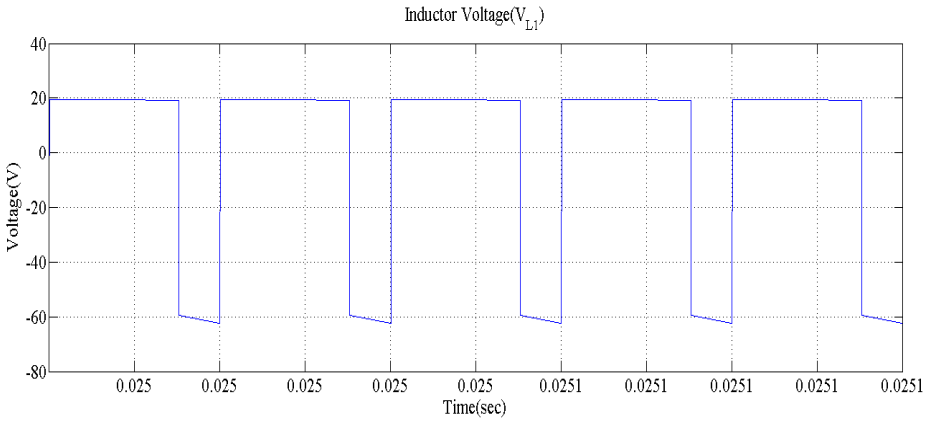

Figure 21. Simulated waveform of first inductor voltage.

Fig. 21 illustrates the simulated waveform first inductor voltage which is 20 V obtained upon the simulation of newly proposed topology. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V.

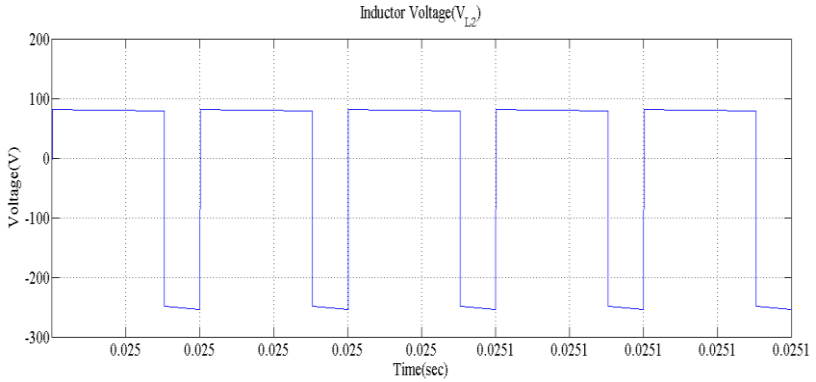

Figure 22. Simulated waveform of second inductor voltage.

Fig. 22 illustrates the simulated waveform second inductor voltage which is 98.5 V obtained upon the simulation of newly proposed configuration. The simulated waveform is of the rectangular type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V.

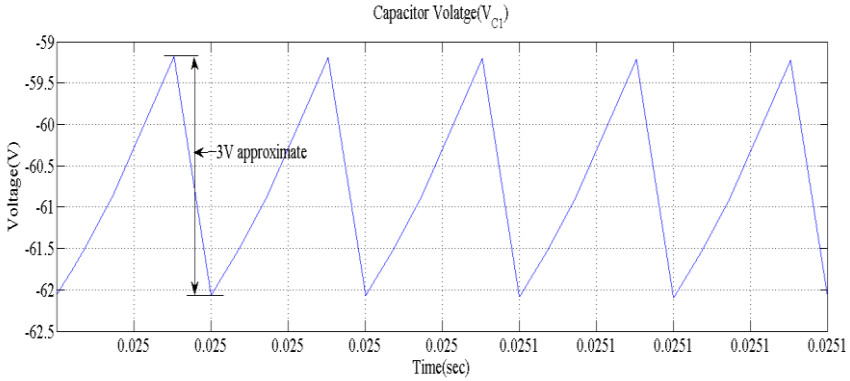

Figure 23. Simulated waveform of pump capacitor voltage.

Fig. 23 illustrates the simulated waveform pump capacitor voltage, which is 59.3 V obtained upon the simulation of newly proposed configuration. The simulated waveform is of the sawtooth type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V. The ripple voltages of the capacitor are taken as 3 V.

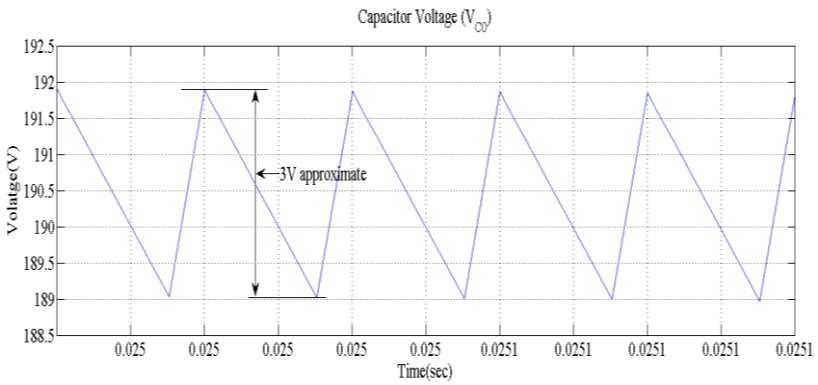

Figure 24. Simulated waveform of output capacitor voltage.

Fig. 24 illustrates the simulated waveform output capacitor voltage, which is 191.8 V obtained upon the simulation of newly proposed configuration. The simulated waveform is of the sawtooth type waveform. The time axis is represented on x-axis which has equal division value of 0.0250 s. The voltage is plotted on y-axis with an interval of 20 V. The ripple voltages of the capacitor are taken as 3 V.

10. PERFORMANCE TABLES

Tables 3,4 show us accurate information regarding efficiency, ripple factor, output voltage, input power, output power and voltage stresses of switches and diodes at various values of duty ratio ranging from 0.1 to 0.8 for the newly proposed converter and the graphs are plotted for all the parametric values mentioned in the above tables.

Table 3. Performance Analysis for Various Duty Ratios

S.no	Duty ratio(D)	Output voltage(V_0)	V_{S1}	V_{S2}	V_{D1}	V_{D2}
1	0.1	8.822	22.22	24.69	22.22	24.69
2	0.15	14.09	23.52	27.68	23.52	27.68
3	0.2	19.24	25	31.25	25	31.25
4	0.25	24.29	26.66	35.55	26.66	35.55
5	0.3	29.28	28.57	40.81	28.57	40.81
6	0.35	34.25	30.76	47.33	30.76	47.33
7	0.4	39.16	33.33	55.55	33.33	55.55
8	0.45	43.97	36.36	66.11	36.36	66.11
9	0.5	48.08	40	80	40	80
10	0.55	52.01	44.44	98.76	44.44	98.76
11	0.6	55.74	50	125	50	125
12	0.65	67.59	57.14	163.26	57.14	163.26
13	0.7	106.4	66.66	222.22	66.66	222.22
14	0.75	173.5	80	320	80	320
15	0.759	192.3	82.98	344.34	82.98	344.34
16	0.8	293.6	100	500	100	500

Table 4. Voltage Stresses for Various Duty Ratios.

S.no.	Duty ratio(D)	Output Voltage V_0	% Ripple	P_{in}(W)	P_{out}(W)	%Efficiency
1	0.1	8.822	1.088	0.254	0.194	76.3
2	0.15	14.09	0.638	0.576	0.496	86.1
3	0.2	19.24	0.675	1.026	0.925	90.1
4	0.25	24.29	0.658	1.596	1.475	92.4
5	0.3	29.28	0.614	2.29	2.14	93.4
6	0.35	34.25	0.729	3.102	2.932	94.5
7	0.4	39.16	0.68	4.03	3.833	95.1
8	0.45	43.97	0.682	5.056	4.833	95.5
9	0.5	48.08	0.707	6.014	5.779	96.09
10	0.55	52.01	0.692	7.006	6.762	95.2
11	0.6	55.74	0.699	8.026	7.764	96.7
12	0.65	67.59	0.710	11.764	11.421	97.1
13	0.7	106.4	0.751	29.18	28.30	97.0
14	0.75	173.5	0.743	78.5	75.25	95.8
15	0.759	192.3	0.847	96.88	92.44	95.4
16	0.8	293.6	0.80	235.8	215.50	91.3

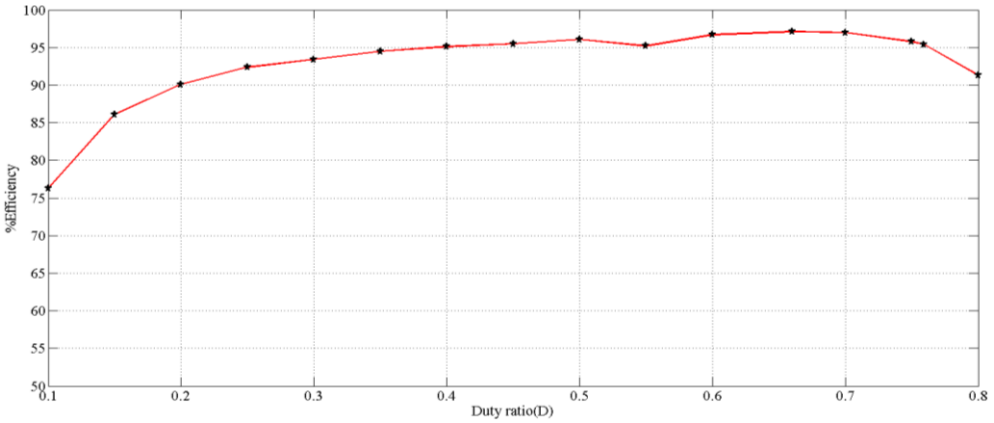

Figure 25. The efficiency graph for various duty ratios.

From Table 3 for various duty ratios ranging from 0.1 to 0.8 the efficiency values which are obtained are plotted in Fig. 25. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the percentage of efficiencies is taken on y-axis with an interval of 5%. There is a gradual increase of efficiency percentage values.

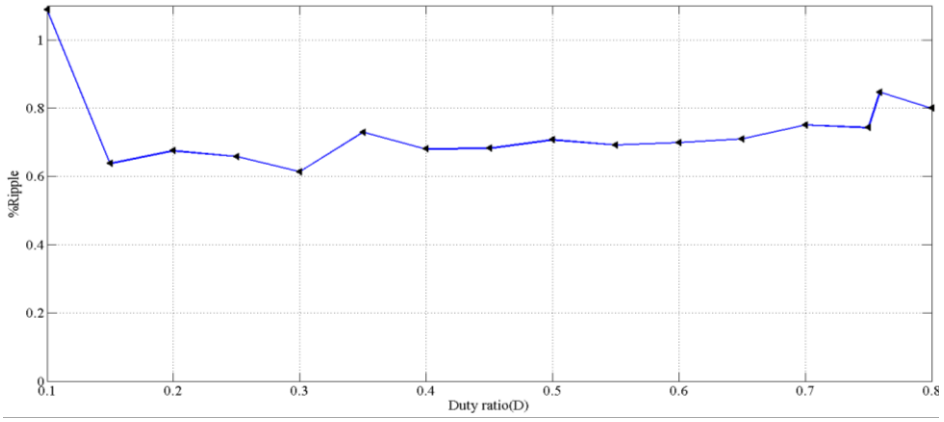

Figure 26. The ripplefactor for various duty ratios.

From Table 3 for various duty ratios ranging from 0.1 to 0.8 the ripple factor values which are obtained are plotted in Fig. 26. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the ripple factor is taken on y-axis with an interval of 0.1. The ripple factor values are low and does not exceed beyond the value of 1.

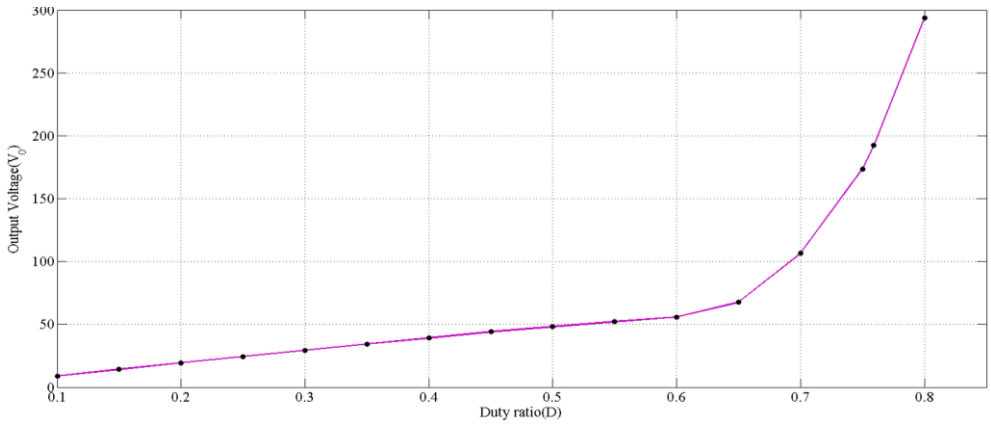

Figure 27. The graph shows the output voltages for various duty ratios.

From Table 3 for various duty ratios ranging from 0.1 to 0.8 the output voltage values which are obtained are plotted in Fig. 27. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the

output voltage is taken on y-axis with an interval of 0.1. The output voltage values are gradually increasing and has reached the most expected value which gives the best performance trait for the converter.

From Table 4 for various duty ratios ranging from 0.1 to 0.8 the diode voltage stress values which are obtained are plotted in Fig. 28 and Fig. 29. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the output voltage is taken on y-axis with an interval of 50 V. The diode voltage stress values are gradually increasing and has reached the most expected value which gives the best performance trait for converter. The various changing values for the first and the second diode are calculated and are represented from the Table 4 where the values are obtained from the scope values of the simulated waveforms.

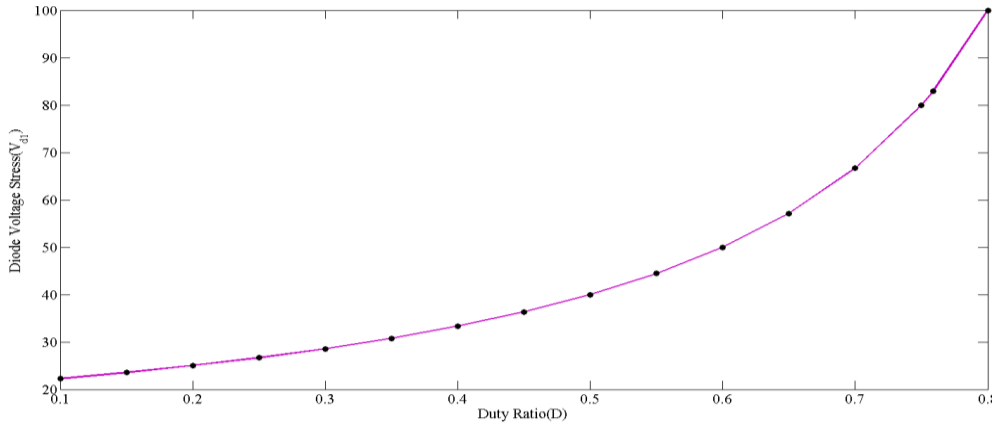

Figure 28. The graph shows the first diode voltage stress values for various duty ratios

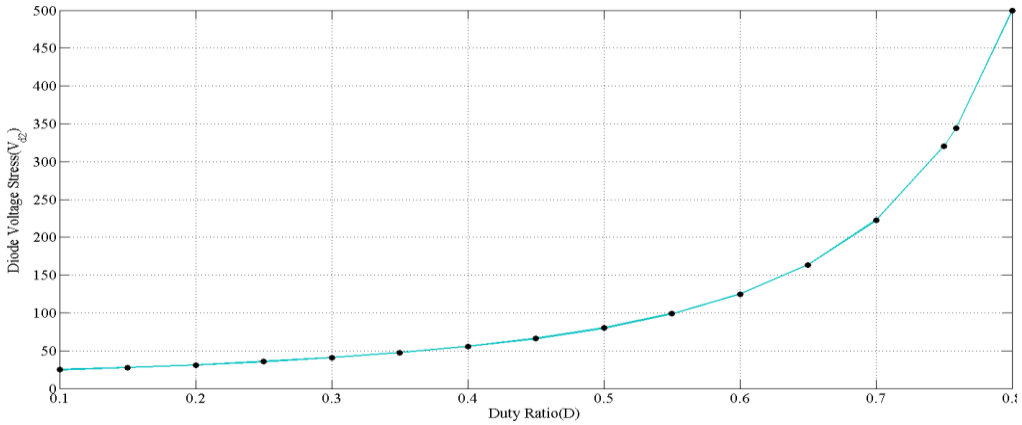

Figure 29. The graph shows the second diode voltage stress values for various duty ratios.

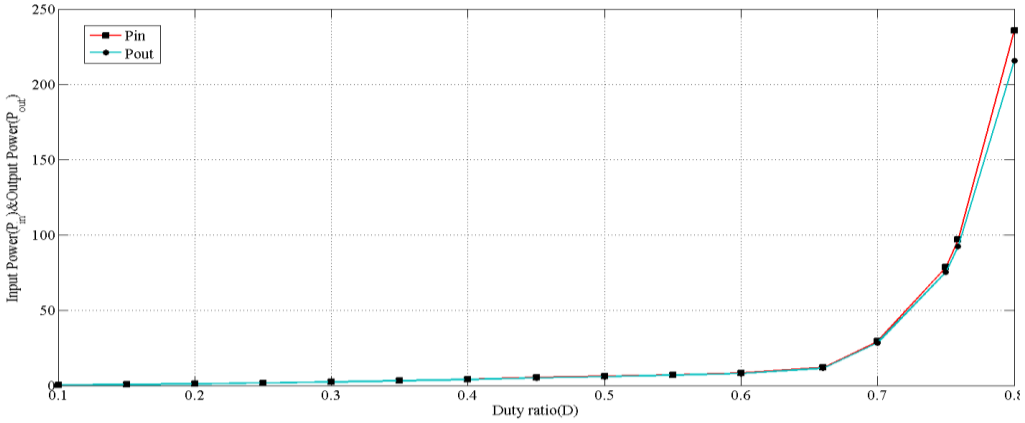

Figure 30. The graph shows input and output power values for various duty ratios.

From Table 3 for various duty ratios ranging from 0.1 to 0.8 the input and output power values which are obtained are plotted in Fig. 30. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the output voltage is taken on y-axis with an interval of 50Watts.The input and output values of the proposed buck-boost converter are calculated and are placed in Table 3 and both the power values are compared and plotted which gives the accurate values resulting in the efficient outcome results of the converter.

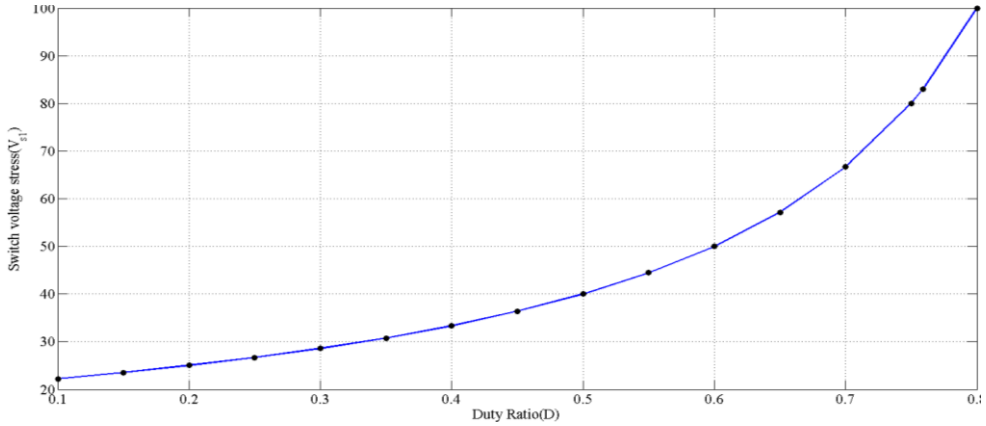

Figure 31. The graph shows the first power switch voltage stress values for various duty ratios.

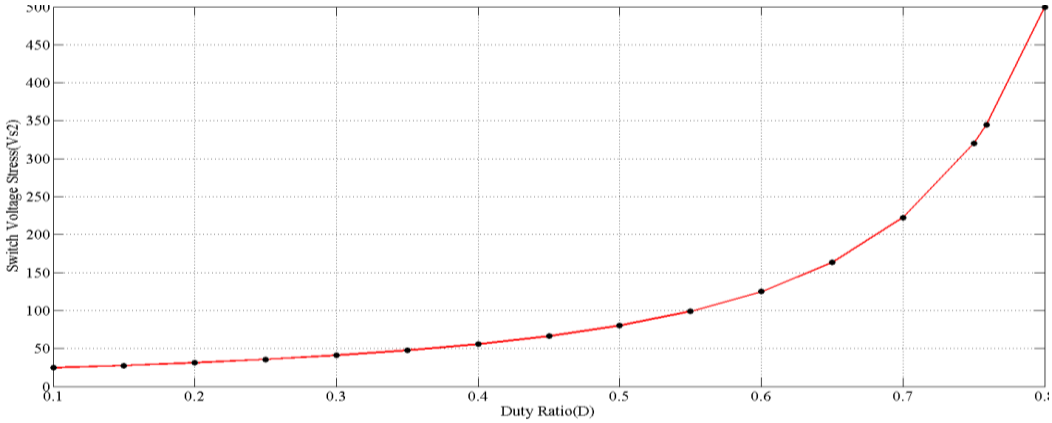

Figure 32. The graph shows the second power switch voltage stress values for various duty ratios.

From Table 4 for various duty ratios ranging from 0.1 to 0.8 the diode voltage stress values which are obtained are plotted in Fig. 31 and Fig. 32. The duty ratio values are taken on the x-axis from 0.1 to 0.8 and the output voltage is taken on y-axis with an interval of 50 V.The voltage stress values of both switches are gradually increasing and has reached the most expected value which gives the best performance trait for the newly proposed buck-boost configuration.The various changing values for the first and the second diode are calculated and are represented from the Table 4 where the values are obtained from the scope values of the simulated waveforms.

11. CONCLUSION

A new non-isolated buck-boost topology which displays the optimization of its construction topology and voltage gain to operate over the limits of the classic buck-boost converter is studied in this thesis. The circuit layouts, working principles, and comparisons with other converters are described. By applying the empirical parametric values, MATLAB simulations and performance analysis of the novel non-isolated buck-boost converter were carried out. The novel non-isolated buck boost converter features, advantages such as a simple design and control method, positive output voltage, and a large

step-up voltage gain. Hence, it is appropriate for all types of switching mode power supply applications which require high step-up voltage gain.

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