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Design a clamp based active filter for the single stage voltage boost small power grid-connected system

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Abstract: Generally, two-stage voltage conversion is preferred for low-voltage DC sources such as PV (photovoltaic) modules, fuel cells, batteries, and super-capacitors however it is not suitable for the small power grid-connected system due to the cost and size. This work considers a single-stage, voltage level enhancement technique with a modified existing system. However, due to the clipped waveform, its output contains low-order harmonics. We design and implement an active filter, based on a clamper circuit to eliminate this clipped waveform. This filter has two tasks. First, detect the lower order harmonics then generate and add friendly harmonics. In our terminology, friendly harmonics are opposite in polarity with the low-frequency harmonics and the same polarity with the fundamental frequency. To prove the novelty, a comparative analysis with the existing strategy is also explained here. We also attempt to depict at least a 0.8% addition reduction in total harmonic distortion by comparing it with another methodology.

Keywords: *Filter, Inverter, Multi level inverter, Neutral point clamp, Over-modulation, Total harmonic distortion*

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Nomenclature	
V_{RN}, V_{YN}, V_{BN}	Line to Neutral Voltages
V_{Ro}, V_{Yo}, V_{Bo}	Pole Voltages
V_{RY}, V_{YB}, V_{BR}	Line to Line Voltages
$V_{\propto}, V_{\beta}$	Orthogonal Voltages
m	Modulation Index
V_{mpt}	Maximum Power Point Voltage
w	Angular Frequency
MPP	Maximum Power Point
T_1, T_2, T_3, T_4	Switches in one phase inverter legs
R_1, R_2, R_3, R_4	Switches in R phase inverter legs
V_{DC}	Inverter input Voltage
UCW	Upper Carrier Wave
LCW	Lower Carrier Wave
V_{P-P}	Voltage Peak to Peak
V_{Sat}	Saturated Voltage
ODE	Ordinary Differential Equation
V_P	Peak value of Modulating Wave
a_0, a_n, b_n	Fourier Series coefficients
$f(x)$	Non Sinusoidal Periodic Function
T	Time
$SVPWM$	Space Vector Pulse Width Modulation
BSS	Battery Storage System
P,Q	Active and reactive power

1. INTRODUCTION

For the low-voltage DC source, two-stage power converters are generally preferred [1]. In the first stage, the input DC voltage increases beyond the peak voltage of the grid DC-DC converter then it is converted into AC in the later stage. This strategy not only reduces efficiency but also increases cost and size. According to literature, a boost inverter provides a higher voltage than a DC input voltage. The differentials of three-phase boost inverters provide for stepping up/down operation using a double boost dc-dc chopper [2, 3]. However, the output current of this inverter contains harmonics. There is another way to step up and down the voltage using the impedance network and shoot-through method in Z-source inverters [4, 5]. Nevertheless, they require not only a large number of passive components but also have leakage current problems. The split-source inverters are also used for buck-boost operation [6, 7]. However, the simultaneous switching of all switches under high voltage stresses affects the reliability and efficiency (due to high switching frequency). The switching losses can be reduced in the dual-buck structured buck-boost inverters in this regard [8-10]. This inverter is also useful for eliminating dead time in switching signals, high efficiency, and high reliability but an experimental setup is not given.

As another type, the buck-boost inverter in Ref. [11] integrates a boost dc-dc chopper and a Hybrid-bridge inverter with a limiting leakage current facility. Even so, it uses a complicated control technique that influences the noise and efficiency by combining continuous conduction mode and discontinuous conduction mode in later conduction mode and sliding mode of operation [12]. Recently, a diamond-shaped multilevel inverter and A Single-phase Hybrid Switched-capacitor inverter were used to reduce voltage ripple in low-power appliances. However, the cost is lower but has fewer lifetimes [13, 14]. Additionally, the passive filter with a higher value of L and C is also required [15, 16]. Therefore, we cannot say it is a single-stage boost inverter. In the literature, a dynamic neutral point clamped (NPC) inverter constructed with cross switched and silicon gallium-trioxide device and one dimension SVPWM techniques are examined [17, 18]. The outcome of later topology lowered the fault current to 52 A while maintaining a more than 99% efficiency [18]. Similarly, two T-type inverters in [19] and adding zero sequences in PWM [20] are used to boost the voltage level. Two different capacitors with self-voltage regulating capabilities are incorporated to achieve a maximum voltage-boosting gain of up to 1.5 in an application presented in Ref. [20].

To produce a voltage-boosting yield of 1.5, a pair of capacitors having self-voltage adjusting abilities is incorporated. Furthermore, the proposed system can generate seven voltage levels [19, 20]. Circuit analysis and prototype experimental findings are used to confirm its operation. This methodology provides one of the best voltage boosting solutions due to the use of two capacitors therefore if we count capacitors as separate states then this methodology is also considered a two stages topology [20]. Additionally, online harmonic extraction and synchronization algorithm-based control are also present in [21] to eliminate the need for a phase-locked loop and traditional filters, allowing the device to recover the fundamental frequency components more precisely. The latest current injection method is used for lower order harmonics elimination and reactive power (Q) support of a three-level NPC-based shunt active harmonic filter. This algorithm is known as the fundamental power frequency signal extraction algorithm [22].

The biggest research gap is most of the technique is used during the initial designing of the system. However, with the existing system voltage boosting is very complicated and costly. The main objective of this work is to find out single-stage boosting without compromising the power quality. Herewith without disturbing the existing system, we have to finish our task.

2. OPERATING PRINCIPLE

A single stage voltage-boosting inverter has to work in over-modulation region. Over-modulation means the peak of these sinusoidal wave voltages is higher than the peak of the carrier. Among the various reasons, one of the most important reasons is to increase the output voltage as in Refs. [23]. With sine triangle PWM, the maximum fundamental voltage whatever we could get 50% of the input voltage. After adding a third harmonics, we can get $0.577V_{DC}$ (15% more). In over-modulation, one can get a maximum of 6-step voltage or $0.644V_{DC}$ of fundamental voltage. However, it introduces low-frequency distortion in the output. In this paper, the over-modulation limit extends further compared to the previous researches. Over-modulation can define in terms of modulation index m.

$$m = \frac{V_{RN}}{V_{mpt}} \tag{1}$$

The modulation index is equivalent to the transformer turn ratio (secondary to primary). If its value is more than unity then the inverter works as a voltage-boosting mode. Therefore, we consider a higher value modulation index.

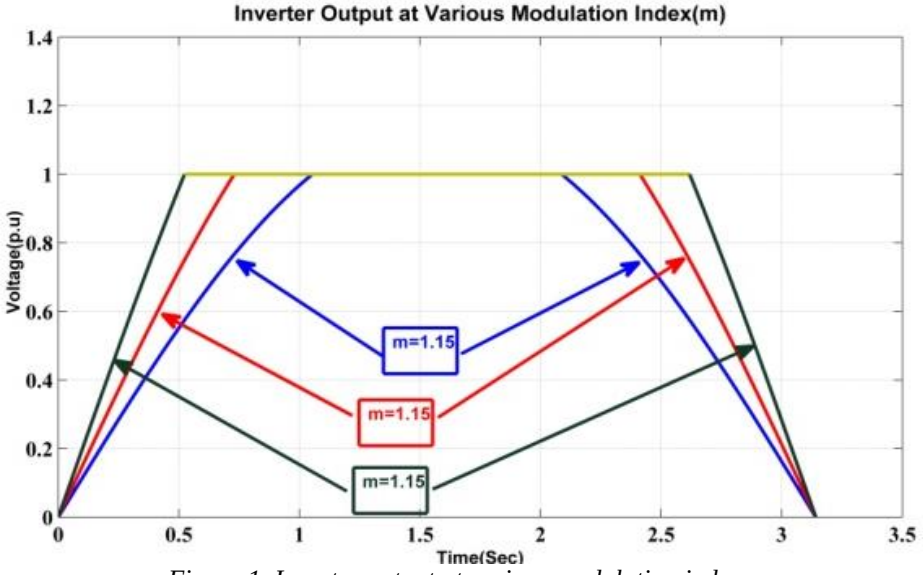


Figure 1. Inverter output at various modulation indexes.

In Fig. 1, if the modulation index is increased, then the waveform is clipped and the tendency of pulse dropping also increases. Therefore, the switching tendency of each switch reduces drastically (as shown in Fig. 2).According to Fig. 2, the double arrow is the region where the *R* phase is not switching (i.e., pulse dropping). The top gate device will be continuously on. Similarly, on the next pulse dropping, it is continuously off here. Therefore, there are no pulses at the on and off region; it is called pulse dropping.

By comparing Figs. 2 and 3, we can quickly examine the pulse dropping nature of the same device in under and over-modulation. If we proceed for a higher value of *m*, then the minimum switching loss occurs in the inverter however, a high low harmonic ripple generates. Detail design and basic concept of the filter is presented in the next section.

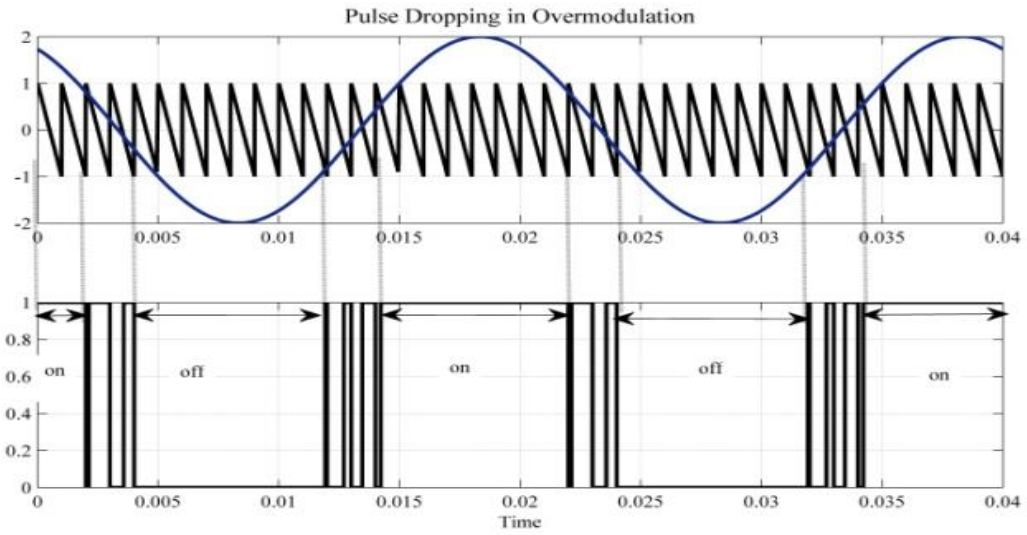


Figure 2. Pulse dropping in over-modulation.

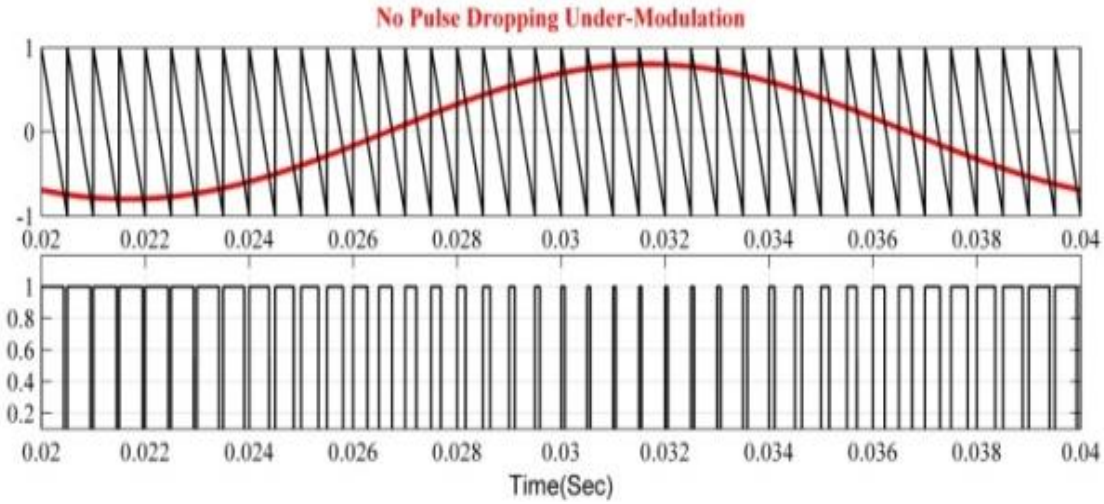


Figure 3. No-pulse dropping in under modulation.

2.1. Clipper Clamper Concept

The output waveforms of STPWM at various indexes are shown in Fig. 1. The clipped waveform due to pulse dropping is also obvious. To obtain ideal sinusoidal waveform, a complementary waveform is needed rather than a deteriorated one. It can be made by a battery introducing a simple clamper circuit so-called "biased clamper circuit". The output waveform of this bias clamper circuit resembles to the remaining part of the inverter. Since the clipper point of an inverter is $0.5V_{DC}$ (1 p.u.). If the same DC voltage source is used for the biasing of the clamper circuit, then the overall waveform can improve; consequently, overall THD can reduce.

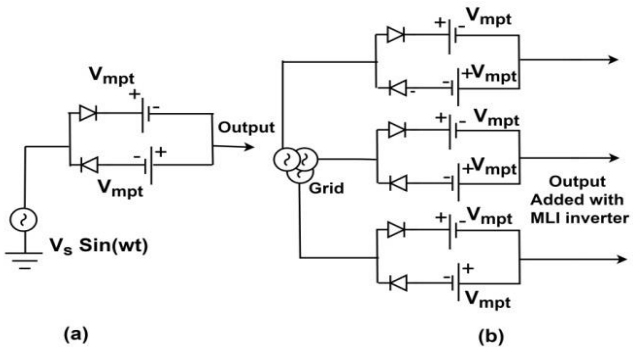


Figure 4. (a) Single, (b) three phase clamper circuits.

The single-phase clamper circuit is presented in Fig. 4(a). In this circuit, anti-parallel diodes with batteries (sometime it may be PV array output) are connected to the AC supply. The extension of this circuit, i.e., the three-phase clamper circuit, is shown in Fig. 4(b). The output of this circuit connects to the MLI inverter.

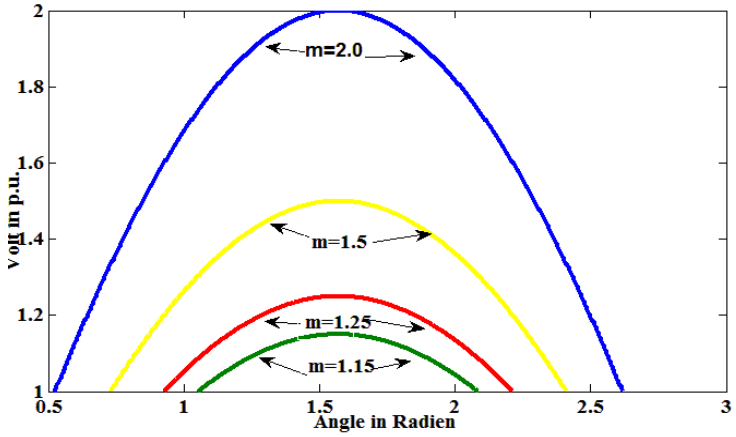
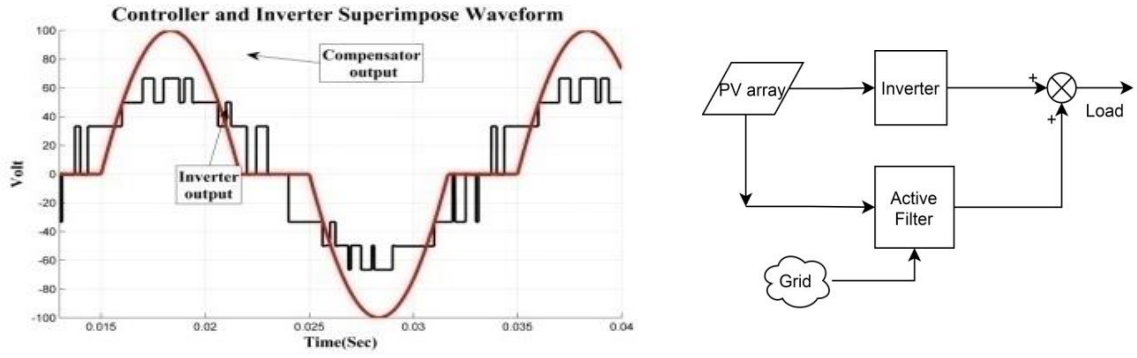


Figure 5. Filter output at various modulation indexes in half cycle.

The corresponding output waveform of a single-phase clamper circuit with the same modulating indexes (as shown in Fig. 1) has shown in Fig. 5. The modulation index depends on the peak value of the carrier wave and the DC voltage (PV array voltage) [23].

Suppose due to an increase in temperature, the standalone PV array output voltage reduces, so modulating index increase from 1.15 to 2, then the output of the clamper circuit is also increased from green to blue color waveform (as shown in Fig. 5) and superimpose Simulink output (Fig. 6(a)) with block diagram (as shown in Fig. 6(b)).



(a) *(b)*

Figure 6. (a) Super impose filter and inverter output voltages, (b) the block diagram.

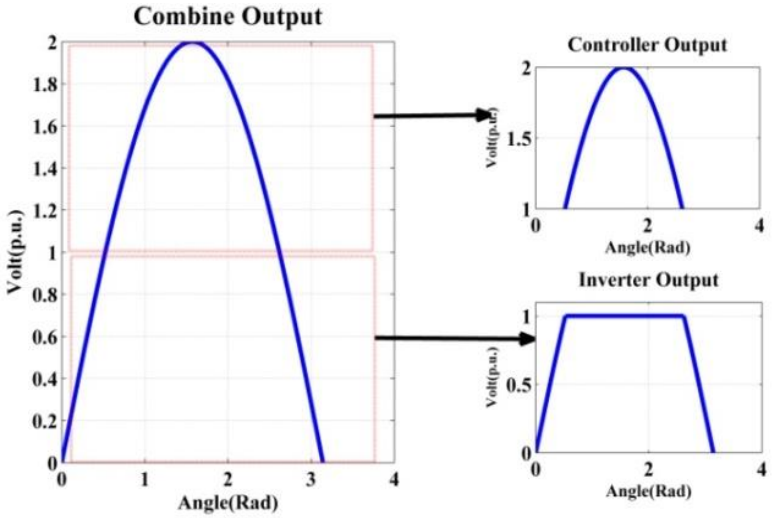


Figure 7. Filter and inverter output waveform.

2.2. Mathematical Modelling of Filter and Inverter Outputs

The output equations of the filter (controller) and inverter are based on the clipper and clamper concept (as shown in Fig. 7). The mathematical representation of this inverter waveform (per phase) is given by Eq. 2. Similarly, the filter circuit waveform at the same modulation indexes has shown in Eq. 3 (Considering m >1) i.e. inverter output waveform,

$$f(x) = \begin{cases} m\sin wt & , wt \le \sin^{-1}\dfrac{1}{m} \\ 1 & , \ \sin^{-1}\dfrac{1}{m} \le wt \le \pi - \sin^{-1}\dfrac{1}{m} \\ m\sin wt & , \pi - \sin^{-1}\dfrac{1}{m} \le wt \le \pi \end{cases} \qquad (2)$$

and filter output waveform is,

$$f(x) = \begin{cases} 0 & , \ wt \le \sin^{-1}\dfrac{1}{m} \\ m\sin wt - 1 & , \ \sin^{-1}\dfrac{1}{m} \le wt \le \pi - \sin^{-1}\dfrac{1}{m} \\ 0 & , \pi - \sin^{-1}\dfrac{1}{m} \le wt \le \pi \end{cases} \qquad (3)$$

For harmonic analysis these equations (Eqs. 2 and 3) are transformed into the frequency domain by using Fourier analysis. So, we have to find out the Fourier series coefficient, [24] shown in Eq. 4

$$= \frac{2}{\pi}\left(\int_0^{\sin^{-1}\frac{1}{m}} \mathrm{m}\sin(\mathrm{x}) * \sin\frac{\mathrm{n}\pi\mathrm{x}}{\pi} * \mathrm{dx} + \int_{\sin^{-1}\frac{1}{m}}^{\pi-\sin^{-1}\frac{1}{m}} 1 * \sin\frac{\mathrm{n}\pi\mathrm{x}}{\pi} * \mathrm{dx} + \int_{\pi-\sin^{-1}\frac{1}{m}}^{\pi} \mathrm{msin}(\mathrm{x}) * \sin\frac{\mathrm{n}\pi\mathrm{x}}{\pi} * \mathrm{dx}\right. \qquad (4)$$

2.3. Inverter Output

By using Eq. 4 harmonics spectra of each part of inverter has been shown by Eqs. 5 to 7.

$$\frac{2}{\pi}\int_0^{\sin^{-1}(1/\mathrm{m})} (\mathrm{m}\sin(\mathrm{x}) * \sin(\mathrm{n}.\mathrm{x}))\,\mathrm{dx} = \frac{2\mathrm{m}\sin\left(\mathrm{n}\sin^{-1}\left(\frac{1}{\mathrm{m}}\right)\right)\sqrt{\frac{\mathrm{m}^2-1}{\mathrm{m}^2}} - \mathrm{n}\cos\left(\mathrm{n}\sin^{-1}\left(\frac{1}{\mathrm{m}}\right)\right)}{\pi(\mathrm{n}^2-1)} \qquad (5)$$

$$= \frac{2}{\pi}\int_{\sin^{-1}(1/m)}^{\pi-\sin^{-1}(1/m)} 1 * \sin(n.x)\,dx \;= \frac{\pi\cos\left(n\sin^{-1}\left(\frac{1}{m}\right)\right) - \cos\left(n\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)}{2n} \tag{6}$$

$$\frac{2}{\pi}\int_{\pi-\sin^{-1}(1/m)}^{\pi}(m\sin(x) * \sin(n.x))dx$$

$$\begin{aligned}
&= \frac{2}{\pi(n^2-1)}\left(m\left(\frac{1}{2}\sin\left((n-1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n\right.\right.\\
&+\frac{1}{2}\sin\left((n-1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)\frac{1}{2}\sin\left((nb+1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n\\
&+\frac{1}{2}\sin\left((n+1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)+\frac{1}{2}\sin(n(n-1)\pi)\\
&\left.\left.+\frac{1}{2}\sin(n-1)\pi-\frac{1}{2}\sin(n(n+1)\pi)+\frac{1}{2}\sin(n-1)\,\pi\right)\right)
\end{aligned} \tag{7}$$

Similarly, for the filter,

$$b_n^{'} = \frac{2}{\pi}\int_0^{\pi} f'(x)\ \sin\frac{n\pi x}{\pi}\ dx$$

$$= \frac{2}{\pi}\left(\int_0^{\sin^{-1}\frac{1}{m}} 0\ \sin\frac{n\pi x}{\pi}dx + \int_{\sin^{-1}\frac{1}{m}}^{\pi-\sin^{-1}\frac{1}{m}}(m\sin(x)-1)\ \sin\frac{n\pi x}{\pi}\ dx + \int_{\pi-\sin^{-1}\frac{1}{m}}^{\pi} 0\ \sin\frac{n\pi x}{\pi}\ dx\right) \tag{8}$$

$$= \frac{2}{\pi}\left(0 + \int_{\sin^{-1}\frac{1}{m}}^{\pi-\sin^{-1}\frac{1}{m}}(m\ \sin(x)-1)\ \sin(nx)\ dx + 0\right)$$

2.3.1 Filter output:

By using Eq. 8 Fourier transform of an active harmonics filter output (as shown by Eq. 9).

$$\frac{2}{\pi}\int_{\sin^{-1}(1/m)}^{\pi-\sin^{-1}(1/m)}(m\sin(x)-1)\ \sin(n\,x)\,dx$$

$$\begin{aligned}
&= \frac{2}{n(n^2-1)\pi}\left(1\left(\frac{-1}{2}m\sin\left((n-1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n^2\right.\right.\\
&+\frac{1}{2}m\sin\left((n+1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n^2\\
&+\cos\left(n\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n^2-\frac{1}{2}m\sin\left((n-1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n\\
&-n.m\sin\left(n.\sin^{-1}\left(\frac{1}{m}\right)\right)\sqrt{\frac{m^2-1}{m^2}}\\
&-\frac{1}{2}m\sin\left((n+1)\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)n\\
&\left.\left.-\cos\left(n\left(-\pi+\sin^{-1}\left(\frac{1}{m}\right)\right)\right)+\cos\left(n\sin^{-1}\left(\frac{1}{m}\right)\right)\right)\right)
\end{aligned} \tag{9}$$

All electrical quantities are in per unit.

2.4. MLI NPC Test System

By considering NPC inverter as a test system and it is based on single pole triple throw switch so that can apply $\pm 0.5V_{dc}$ and zero voltage at the load terminal (represent in Fig. 8)

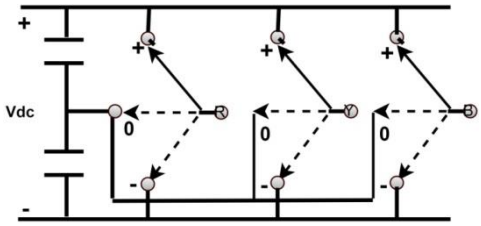


Figure 8. Multi-level inverter with single pole triple throw

As shown in Fig. 8, we have the option of either connecting it to the positive bus or DC midpoint or negative bus. Earlier, the DC midpoint in a two-level inverter is not available for making an electrical connection. Sometimes load current may flow in or out of this particular point, and we have a single pole triple throw switch, so it is called a three-level inverter.

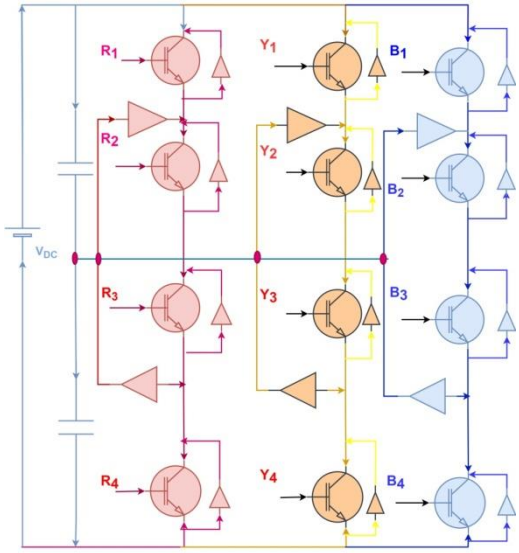


Figure9. Multi-level neutral point clamped inverter

Various combinations of pole voltages are (using eqs. (10-12))

$$V_{RO} = 0, \pm\frac{V_{dc}}{2} \tag{10}$$

$$V_{YO} = 0, \pm\frac{V_{dc}}{2} \tag{11}$$

$$V_{BO} = 0, \pm\frac{V_{dc}}{2} \tag{12}$$

Similarly, the line-to-line voltage we can calculate by Eq. (13)

$$V_{RY} = V_{RO} - V_{YO} \tag{13}$$

$$V_{RY} = 0, \pm\frac{V_{dc}}{2}, \pm V_{dc} \tag{14}$$

The number of levels counts on the bases of the line-to-line pole voltage so it can also call a 5-level inverter as we have shown by Eq. (14). Here, in this paper, the number of levels is equivalent to the number of pole voltages. The top two devices (R_1 and R_2) are on the bottom two (R_3 and R_4) off. In this case, phase R is connected to $\frac{V_{dc}}{2}$. Hence, this is the pole connected to the top throw. We can connect the pole to the bottom throw, by keeping R_1 and R_2 off, and R_3 and R_4 (as shown in Fig. 9) on. Therefore, we will have this pole connected to the bottom throw. Apparently, pole voltages can be zero, when the pole R is connected to O, by the middle two switches being on. The same way pole voltages of Y and B are zero if the middle two switches are on as shown in Table 1.

Table1. Switching sequence with pole voltages

R_1	R_2	R_3	R_4	Pole Voltage
1	1	0	0	$0.5V_{DC}$
0	1	1	0	0
0	0	1	1	$-0.5V_{DC}$

It is also possible to connect R to O; by turning off R_1 and R_4 & on R_2 and R_3. Therefore, R could establish a connection with O. Two different paths would depend on the load current. All switches have the bi-directional current flowing capability. Per phase load voltages is presenting by Eq. 15

$$V_{RN} = \frac{1}{3}(V_{RY} - V_{BR}) \tag{15}$$

Various combination of phase to neutral voltages as shown by Eq. 16

$$V_{RN} = 0, \pm\frac{V_{dc}}{3}, \pm\frac{V_{dc}}{2}, \pm\frac{V_{dc}}{6} \pm \frac{2V_{dc}}{3} \tag{16}$$

Hence, this converter can apply nine levels of voltages at the pole regardless of the direction of the current and line to neutral voltages (as shown by Eq. 16). There are also two complementary switches pairs available R_1 and R_3 & R_2 and R_4 i.e.in two-level inverter; there is one pair of complementary switches; now here two pairs of complementary switches.

Earlier, in STPWM for the two-level inverter, we could compare a one sine wave with one carrier wave [14]. Now in NPC for single sine wave with two carrier waves, because we have to produce two signals, it can also be with two sine waves with one carrier, but in our case, we consider one sine and two carrier waves.

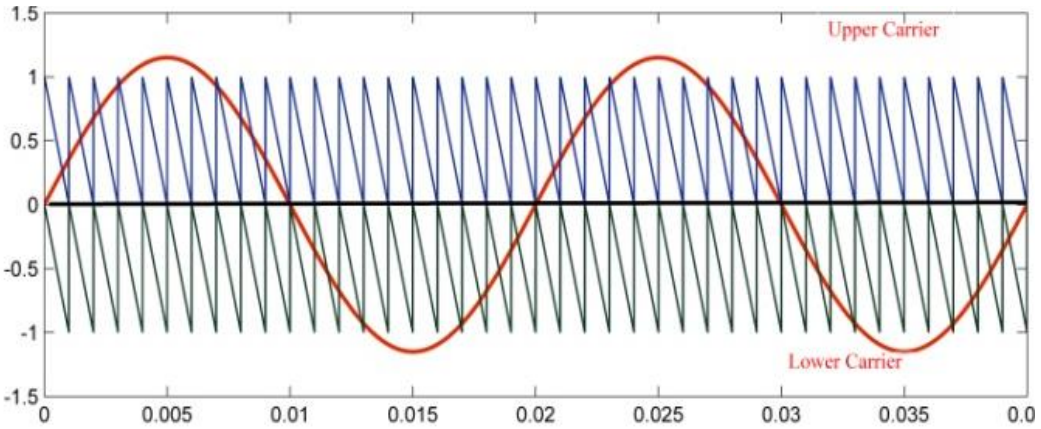


Figure 10. Carrier wave for NPC

There are two different carriers, one way of doing with the same R, Y, and B, but now there are two level-shifted carriers (as shown in Fig. 10). In this figure, only the R phase is drawn; it is higher than

both the carrier signals, then the R phase both the top switches on. If it is lower than the upper carrier wave but higher than the lower carrier wave, then the middle two switches on. Similarly, it is lower than both the carrier waves the bottom two switches on.

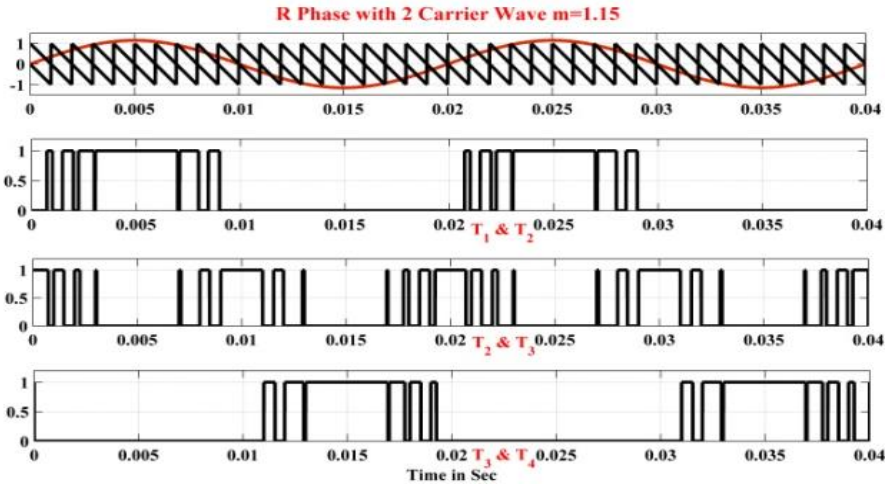


Figure 11. R phase with combined switching pairs ($T_1\ T_2$, $T_2\ T_3$, and $T_3\ T_4$) at m=1.15.

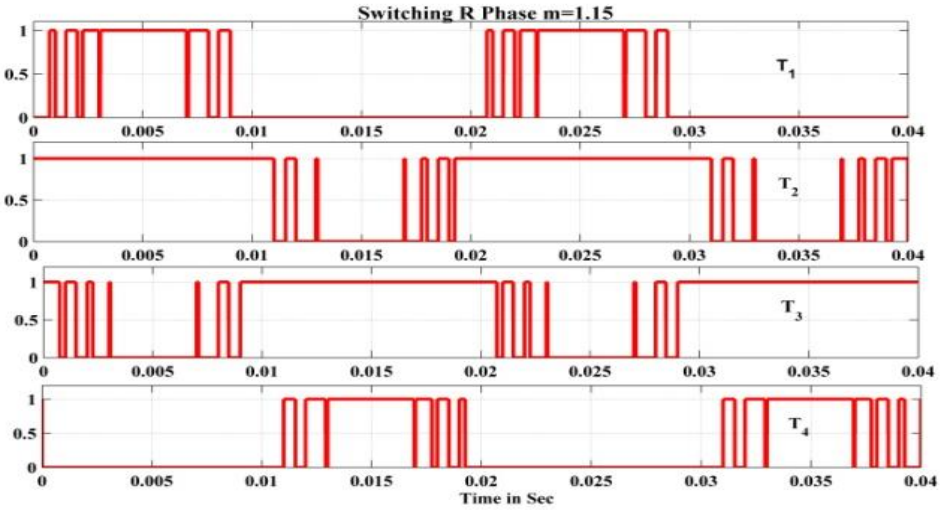


Figure12.R Phase has individual Switching Pairs (T_1, T_2, T_3, T_4) at m=1.15.

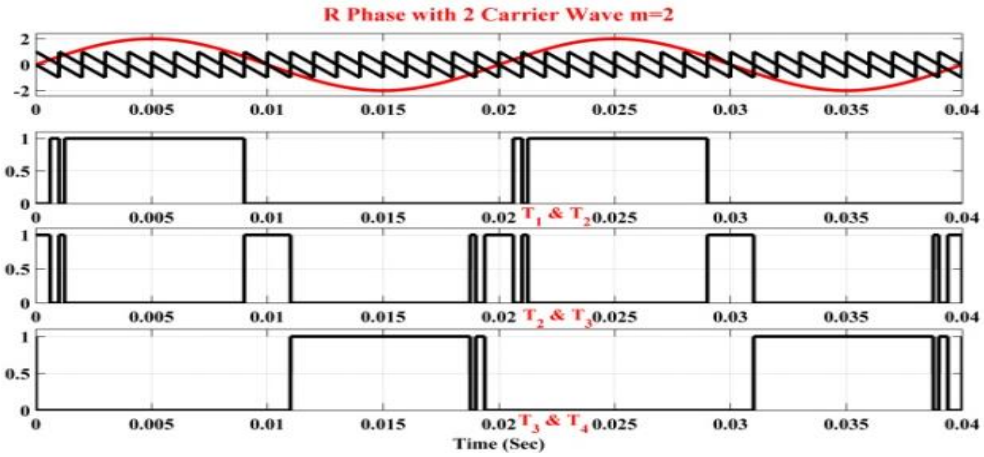


Figure 13. R phase with the combined switching pairs ($T_1\,T_2, T_2\,T_3$, and T_3, T_4) at m=2.0.

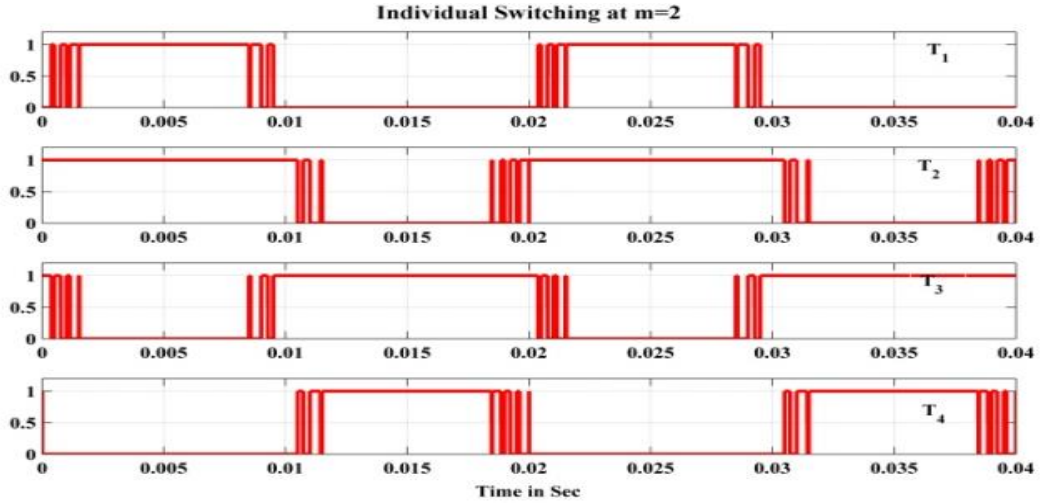


Figure 14. Switching pulses for R phase switches at m=2.0.

In over-modulation, (zone I) combine and individual switching of R phase have been shown in Figs. 11 and 12 respectively. If we enter in deeper modulation indexes (zone II), then the combine switching operation (as shown in Fig. 13) and individual switching approximately equal to 6-step operation (as shown in Fig. 14). It has been also valid for MLI. In this case, the switching frequency is less; however, the THD is very high in stand-alone PV system. In this case, low harmonic frequency voltage and current are very high, and to compensate for these ripples, we have to design the controller.

3. SYSTEM IMPLEMENTATION WITH FILTER AND MLI

3.1. Hardware Implementation

Hardware implementation of complete setup is in three steps

3.1.1 Carrier wave generator

We show an electronic circuit using OP-AMP in Fig. (15) for the design of a carrier wave generator. The following circuit parameters are V_{P-P} =7 V, V_{Sat}=14 V, C=0.05 μF, R_2=6KΩ, f_0=10 kHz and by using the following relations,

$$R_3 = \frac{2R_2}{V_{P-P}} V_{Sat} \quad (17)$$

$$C_1 = \frac{R_3}{4R_2 R_1 f_o C} \quad (18)$$

We can calculate the values of R_3 and C_1 of carrier wave generator by using Eqs. (17-18) as shown in Fig. 15.

3.1.2 UCW and LCW:

We also implement two level-shifted carrier waves electronic circuit by using OP-AMP in Figs. 16 and 17.

3.1.3 Designing of pulse generator

Pulse generation has been explained in an earlier section the same mechanism is used for designing pulse generators. As we know, pulse generator consists carrier wave (as shown in Fig. 15) and two level shifted carrier wave (as shown in Fig. 16 with experimental setup in Fig. 17). Neutral point clamp inverter consists three lags (i.e. three phases) and all legs are identical (except 120° phasor shifting) therefore 1 phase circuit diagram is shown in Fig. 18.

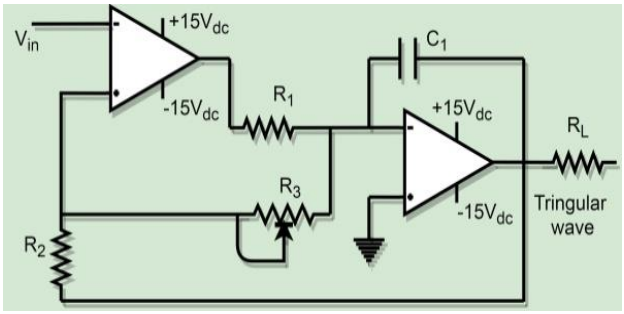


Figure 15. Circuit diagram for carrier wave generator

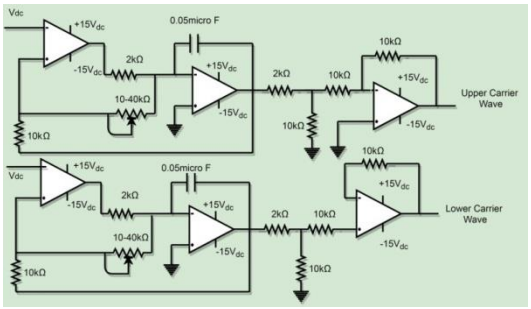


Figure16. Circuit diagram for two level shifted carrier wave for NPC

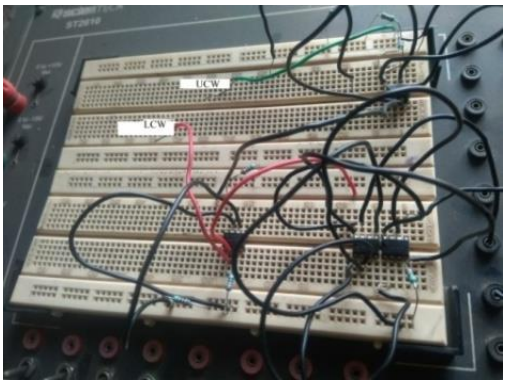


Figure 17. Experimental Setup for two carrier waves

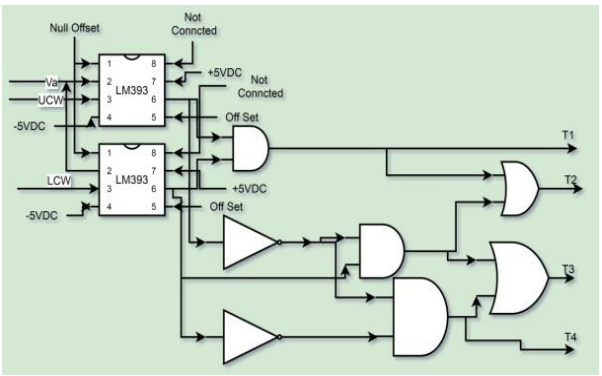


Figure 18. Circuit Diagram for pulse Generator (R-Phase)

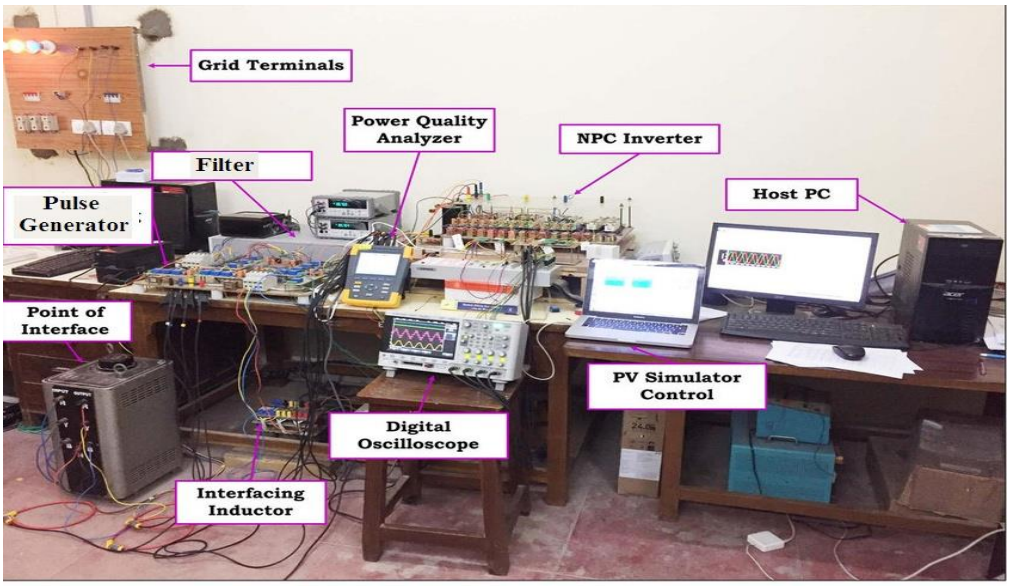


Figure 19. Experimental setup

The performance of the proposed voltage boosting strategy is illustrated through simulation, mathematical modeling and experimental results. The experimental setup for a small power grid-connected 3L-NPC solar photovoltaic inverter is shown in Fig. 19. An 11.5 kW solar PV array is emulated by using CHROMA 62050H-600S solar array simulator. A 3Level -NPC inverter is developed by using Siemens BSM75GB120DN2 IGBT modules and is driven through a pulse generator with a gate drive opto-coupler. The voltage feedback signals measured by using LEM LV-25 sensors are fed to the control algorithm via the CP1104 I/O connector. The load is connected to the grid through a filter and inverter. The performance of the filter is assessed in terms of total harmonic distortion (percentageTHD) and output higher voltage amplitude concerning to low PV simulator generated voltage.

3.2 Simulink Model with Software Implementation

The simulation model (as shown in Fig. 20) has the following power GUI setting as shown in Tables 2 with designing parameters as shown in Table 3.

Table 2. POWERGUI Setting

1	Solver	ODE23tb(Stiff/TR/BDF2)
2	Discrete step time	50*10-6 Sec
3	Simulation Time	0.04 Sec

Table 3. Designing Parameters

S. No.	Parameter	Value
1	Supply Frequency	50 Hz
2	Carrier Frequency	2000 Hz
3	D.C. Link Capacitor	106μF
4	Inverter Voltage	> 110V

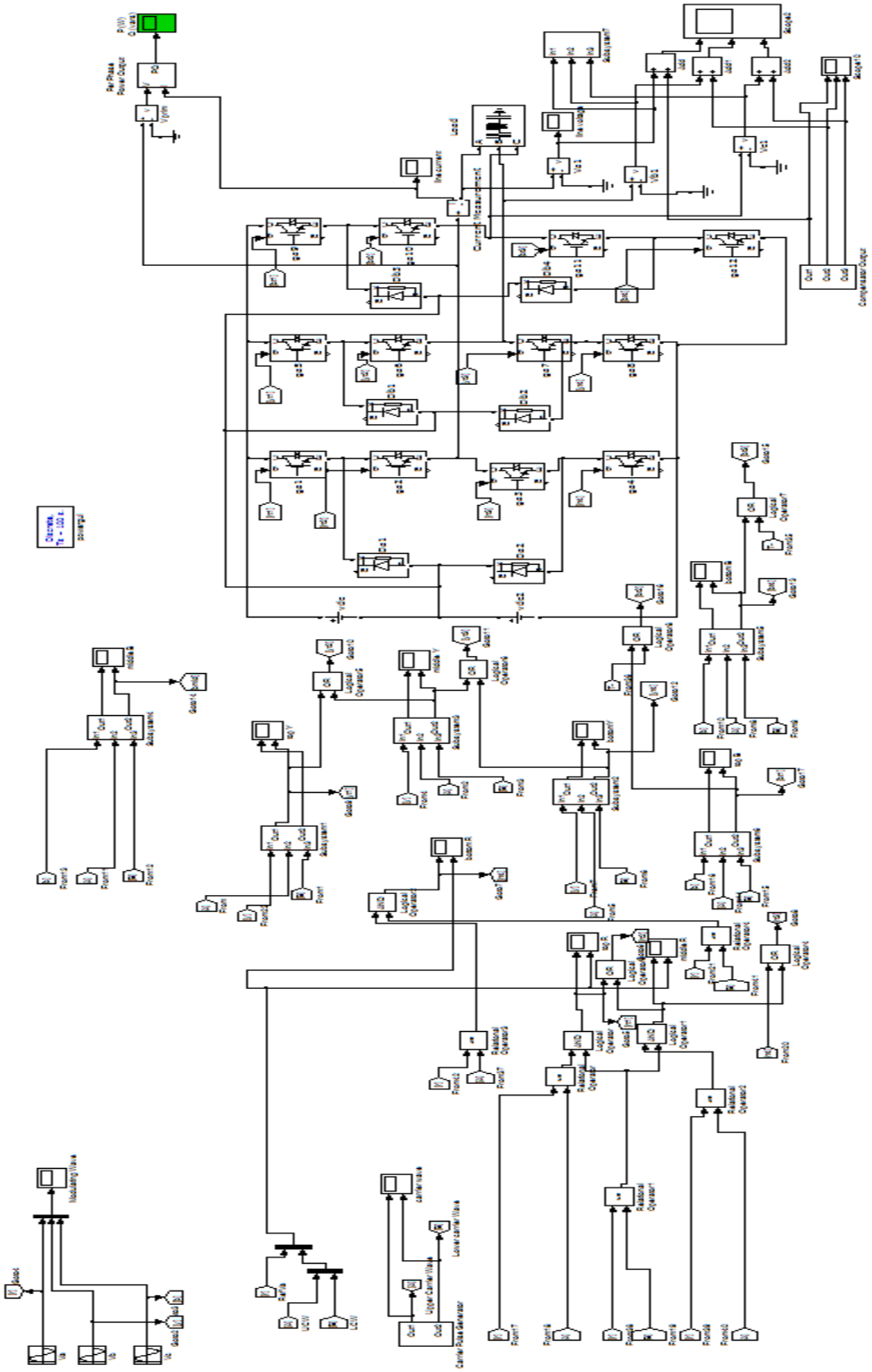


Figure 20. Simulink model complete setup in a compressed form.

4. RESULTS AND DISCUSSION

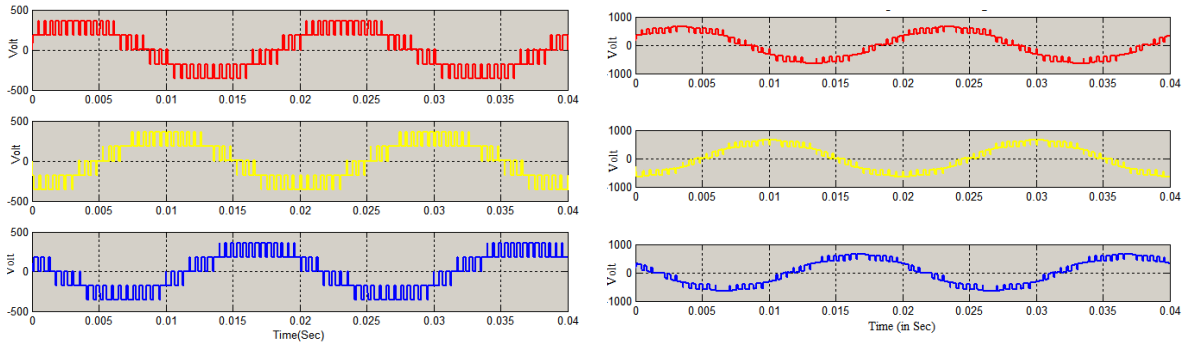
For the validation of these filter outcomes three different ways have been used. In the first segment simulation results in real time mode has been shown with appropriate assumption. In order to provide

strong evidence results based on mathematical modeling and experimental set up are also presented. In order to proof the novelty we have compare our results with and without filter in another segment.

4.1. Simulation Results

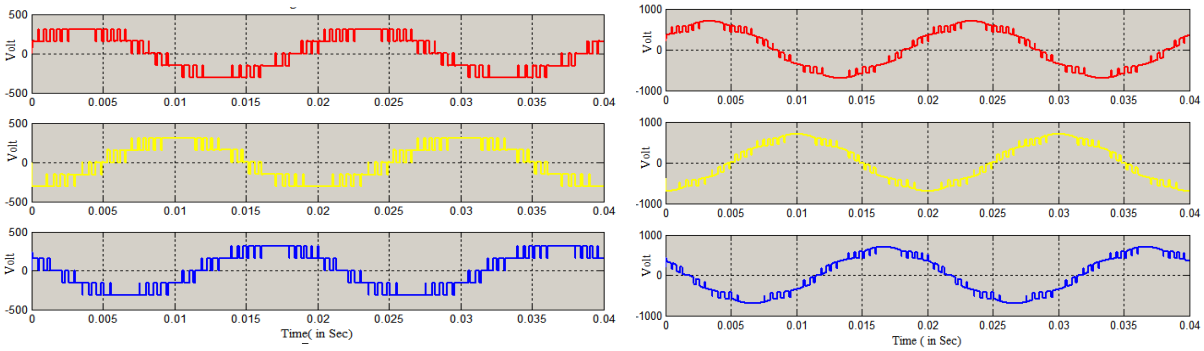
Following assumptions have been considered during this simulation:

Diode cut-in voltage is neglecting. It is a fair assumption because of our DC voltage of hundred volts and the diode cut in voltage (0.7 volts). DC ripple current is neglecting due to a single-stage without dc chopper. The switching delay has been neglected (very high switching frequency).



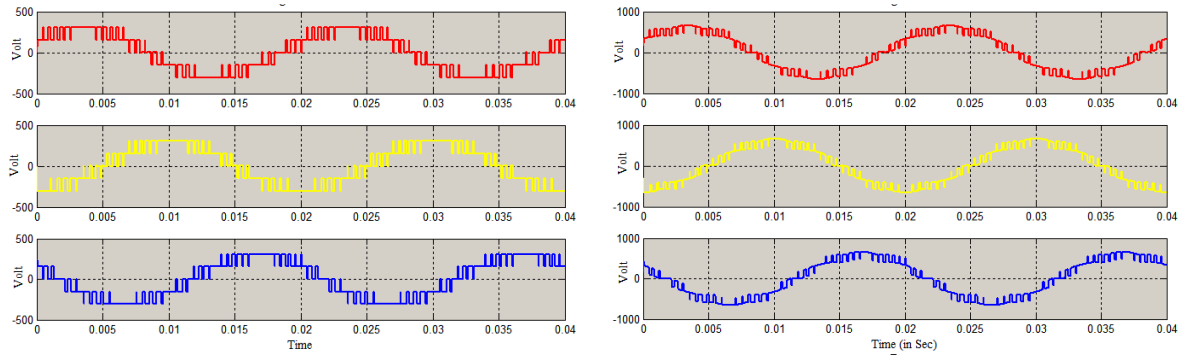
(a) *(b)*

Figure 21. Final output at m=1.15: (a) without filter, (b) with filter.



(a) *(b)*

Figure 22. Final output at m=1.5: (a) without filter, (b) with filter.



(a) *(b)*

Figure 23. Final output at m=2.0: (a) without filter, (b) with filter.

Figs. 21(a), 22(a) and 23(a) show the final output (inverter without filter) at various modulation indexes. The filter can provide the filler voltage in the pulse-dropping region. In this region, the filter generates a clamp signal and adds up with a clipped inverter output. Therefore, that overall THD reduces. Now the output voltage at various modulation indexes is shown in Figs. 21(b), 22(b) and 23(b) the final output (combine the output of inverter and filter). This filter can provide the filler voltage in the pulse-dropping region. In this region, the filter generates a clamp signal and adds up with a clipped inverter signal. Therefore, that overall THD reduces.

4.2. Results Based on Mathematical Modeling

By using Eqs. (5-7, 9) we can obtain a similar nature of output in terms of the harmonic spectrum.

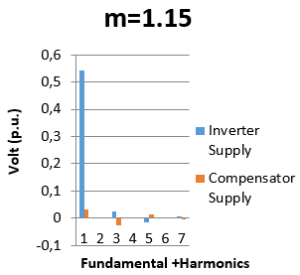


Figure 24. Fundamental and harmonics supply by inverter and filter (1st, 3rd, 5th, and 7th) at m =1.15.

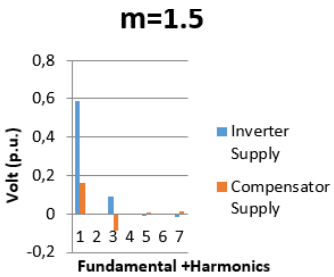


Figure 25. Fundamental and harmonics supply by inverter and filter (1st, 3rd, 5th, and 7th) at m=1.5.

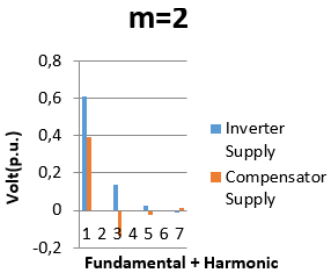


Figure 26. Fundamental and harmonics supply by inverter and filter (1st, 3rd, 5th, and 7th) at m=2.0.

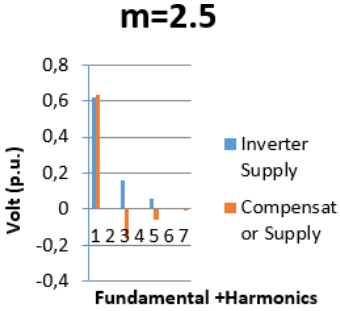


Figure 27. Fundamental and harmonics supply by inverter and filter (1st, 3rd, 5th, and 7th) at m=2.5.

The harmonic spectrums at various modulating indexes (*m*) of the inverter and filter have shown in Figs. 24, 25, 26 and 27 at *m*=1.15, 1.5, 2 and 2.5 respectively. The filter generates the opposite polarity of harmonics with the same amplitude as the inverter. They cancel each other due to the opposite polarity. These figures also indicate that harmonic components increase with a higher modulation index. It has been shown that the increment in the modulation index increases the lower order harmonics. The filter provides reverse polarity harmonics (*w.r.t.* to the inverter) and after adding this, we can reduce the overall THD.

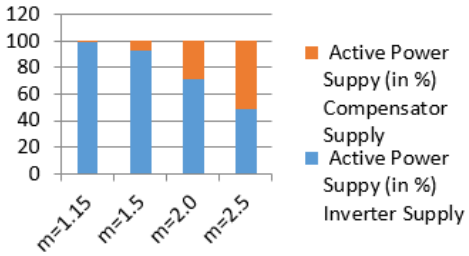


Figure 28. Inverter and filter contribution at various modulation indexes.

The increment in m than the filter contribution is more on fundamental voltage (Fig. 28). The filter provides more voltage than the inverter if the modulation index is more than 2.5. If we connect this filter, the fundamental of AC, supply reduces so that the corresponding active power contribution also decreases. However, harmonic has been generated. Still, the inverter has the reverse polarity of harmonics, and both cancel each other (also explained earlier in mathematical modeling). Under modulation region *m*<1 mathematical model is not valid so, the filter does not work. The whole system works as a conventional NPC inverter. For a very high modulation index, the inverter contribution is less as shown in Fig. 28.

4.3. Experimental Results

In this section, the experimental results has been shown in Fig. 29. There is blank space (in Figs. 29(a,c)), which is filled up by filter as shown in Figs. 29(b,d). Figs. 29(b,d) waveforms approximately match with Fig. 22(b) and Fig. 23(b) *R* phase line to line voltages respectively.

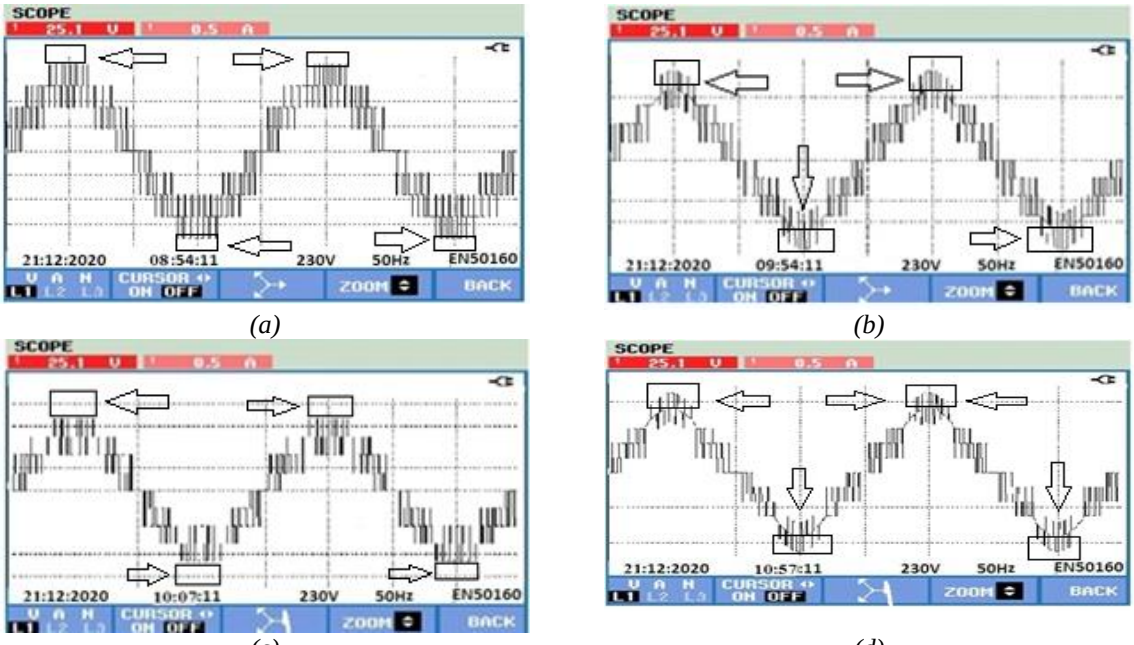


Figure 29. (a) Overall output at m=1.5 without stabilizer, (b) experimental validation of Fig. 22 with stabilizer, (c) overall output at m=2 without stabilizer, and (d) experimental validation of Fig. 23 with stabilizer.

5. CONCLUSION

In the present paper, we have designed an active filter along with a single-stage power booster to improve overall efficiency. Due to the single-stage conversion, the number of components reduces. It has been shown that the increment in the modulation index (from 1.15 to 2.0) increases the lower-order harmonics. The filter provides reverse polarity harmonics (*w.r.t.* to the inverter) and after adding this, we can nullify the overall THD. By comparing with the existing topology, we try to reduce at least 2.5% more THD. Therefore, the filter can eliminate the low voltage ripple in a single stage by adding some friendly harmonics. The salient feature of this filter is easy to construct without modification to the existing system and simple plug-and-play in voltage boosting mode. This filter can automatically disconnect and shift into the step-down mode if it is required. For the validation of this work, experimental, theoretical, and results based on a mathematical model also presented. The experimental power scope waveform is matching with the Simulink scope waveform. It is due to harmonics elimination and verification by modulating figures. Further, this filter will very useful to stabilize the voltage level for renewable energy sources like PV arrays. It will also helpful to nullify the impact the shadow of building with unequal height with uncertain weather conditions.

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