Research Article GU J Sci 36(1): 208-218 (2023) DOI: 10.35378/gujs.998008

Gazi University

Journal of Science

http://dergipark.gov.tr/gujs

Design of a Low Cost X-Band LNA with Sub-1-dB NF for SATCOM Applications

Galip Orkun ARICAN[1,*], Nursel AKCAM[2]

[1]*ASELSAN Inc., Communication and Information Technologies Division, 06200, Ankara, Turkey*
[2]*Gazi University, Faculty of Engineering, Department of Electrical and Electronics Engineering, 06570, Ankara, Turkey*

Highlights

- Design of a low-cost low noise amplifier with sub-1-dB noise figure for SATCOM applications.
- Common source and source degeneration topologies were used to enhance the electrical performance.
- A low noise figure with high gain and moderate linearity performance were obtained.

Article Info

Received: 21 Sep 2021
Accepted: 09 Feb 2022

Keywords

X-Band
LNA
FET
Noise figure
SATCOM

Abstract

In this article, we demonstrate a low-cost 7.25-7.75 GHz two-stage low noise amplifier with sub-1-dB noise figure for satellite communication applications. The microstrip technology on Rogers RT5880 substrate with the dielectric constant of 2.2 and thickness of 0.508 mm were utilized to develop a low noise amplifier. The printed-circuit-board technology offers a variety of profits such as being low-cost, lighter-weight and re-configurability after the manufacturing process make this technology charming for satellite communication systems for both commercial and military applications. Since the monolithic microwave integrate circuit technology provide much smaller sized circuits and high electrical performance especially at the millimeter-wave frequencies, the printed microstrip technology can be a significant rival to integrated-circuit technology with its proven reliability, easier, cheaper and faster manufacturing process, compactible electrical performance in X-band applications. Moreover, the proposed amplifier was developed with utilizing California Eastern Laboratories' CE3512K2 transistor on Rogers-RT5880 and surface mount devices were utilized in the matching networks to reduce the size. In addition, the source-generation and interstage matching topologies were implemented to simplify the matching complexity to enhance the noise and gain. The prototype was manufactured with utilizing LPKF prototyping machine. The developed LNA exhibits a measured gain of 23.5±0.5 dB with the noise figure of less than 0.9 dB and input/output return loss better than 11.5 dB in the operating frequency bandwidth. Furthermore, the developed amplifier has a measured carrier to interference of -59 dBc and P1dB of 13 dBm at the center frequency while consuming a total DC power of 50 mW.

1. INTRODUCTION

In the recent years, the satellite communication systems have received significant attention in many application areas such as internet, fax, telephony, data transfer, financial transactions, military and much more [1]. With these facilities, the satellite communication (SATCOM) applications have become an indispensable necessity for both commercial and military consumers in the modern life and tactical field. A high sensitive and reliable SATCOM systems plays a significant role in the absence of the terrestrial communication on side. In addition, geostationary (GEO) satellites contribute a wide range network coverage and long distance secure communication [2, 3]. Due to the expeditiously growing interest on the SATCOM, an appreciable interest has occurred in the development of the low-cost, lighter-weight and reliable modern microwave receiver systems [4]. In order to respond the needs of the next generation SATCOM systems, a high sensitive and wider dynamic range receivers needs to be developed [5]. Cryogenic microwave low noise amplifiers are the crucial subsystems in a receiver system. The low noise amplifier (LNA) has a key role in a SATCOM receiver requiring high dynamic range, excellent gain flatness

*Corresponding author, e-mail: goarican@aselsan.com.tr

to determine the figure of merit of the system [6]. The monolithic microwave integrated circuits (MMIC) and printed microstrip technology are widely utilized in the LNA design. The MMICs have the advantage of having very compact size, being ultra-low weight and having lower intrinsic NF than the microstrip technology. Moreover, the microstrip technology on printed circuit board (PCB) has a proven reliability in high frequency microwave applications. On the other hand, the manufacturing process of the MMIC technology is very complex, expensive and needs to be qualified. These characteristics make the MMIC technology charming in the millimeter-wave frequency applications. However, unlike integrated circuits, the microstrip technology is much cheaper and provides flexibility to the designers in a possible mismatch.

In this paper, a low-cost LNA with sub-1-dB noise figure (NF) was developed for X-band SATCOM applications. In the design, common source (CS) topology with source degeneration (SD), independent bias circuits and interstage matching topologies were utilized to achieve the tradeoff between the NF, small signal gain and linearity. Common source topology with source degeneration retains the NF as minimum as possible and approaches the input impedance to 50 Ω to simplify the input matching network. In addition, the independent biasing lines give opportunity to control each transistor separately and interstage matching topology keeps the maximum power transfer between the stages. The proposed LNA was manufactured on a low-loss Rogers RT5880 substrate using the microstrip technology with California California Eastern Labratories' (CEL) packaged CE3512K2 FET. The developed LNA has achieved a NF of 0.9 dB and a small signal gain of 23.5±0.5 dB over 7.25-7.75 GHz. Moreover, the output power at 1-dB compression point has achieved +13 dBm and the carrier to interference was measured as -59 dBc at 7.5 GHz. The developed LNA is low-cost, easy to manufacture, can be utilized in X-band SATCOM applications and can be fit to other frequencies and applications.

2. MATERIAL METHOD

2.1. Circuit Design

In the communication systems, LNA plays a crucial role to amplify the received weak signal with adding minimum noise to the system. The high gain and low NF performance of the LNA determines the dynamic range of the system. In addition, LNA needs to work as linear as feasible so as not to cause to the intermodulation distortion. So as to achieve the electrical requirements, a variety of design topologies were examined in different approaches and a two-stage LNA design with common source topology were utilized in the design. In advance, common source topology has the minimum noise figure (NF_{min}), high small signal gain and low power dissipation with respect to the other topologies such as common gate and cascaded topologies. On the other hand, the common source topology has moderate linearity, narrow bandwidth and poor stability performance. Moreover, a commercially available CEL super low noise and high gain radio frequency (RF) FET CE3512K2 was utilized in the design. In addition, S-parameters and NF data file of the transistor, which was provided by the manufacturer, was utilized in the design. Furthermore, the 1st was designed to minimize the NF and maximize the small signal gain and 2nd stage was designed to achieve better intermodulation distortion while keeping the noise figure as minimum as feasible. The input and output terminations of the two-stage LNA were matched to 50 Ω.

The total NF of the N^{th} stages system can be calculated by Harold Friis' total noise factor (F_{total}) (Equation (1)). In this equation, F_i denotes the noise factor of the i^{th} stage, G_j denotes the gain of the j^{th} stage. According to the Friis' equation, it is obvious that the noise performance of the 1st stage predominantly affects the total noise performance of the system. So as to keep the noise of the system minimum, the gain of the 1st stage needs to be as high as possible while the noise is minimum to limit the effects of the noise of the next stages.

$$F_{total} = F_1 + \sum_{i=2}^{N} \frac{F_i - 1}{\prod_{j=i}^{N} G_{j-1}}. \quad (1)$$

In the design, the single CE3512K2 FET was analyzed in the Advanced Design System (ADS) schematic software. The S-parameters and noise figure simulations was performed with using the transistor measurement results that was given in the datasheet. In the simulations, it was seen that single transistor was unstable in the operating frequency bandwidth and so as not to confront with the unwanted oscillations,

the single transistor needs to be stabilized. On the other hand, the input impedance of the single transistor needs to be matched to the complex conjugate of the optimum input impedance (Γ_{opt}=0.18+j52) to accomplish the minimum noise figure performance. In the design, the SD technique was implemented with adding an inductive shunt transmission line to the source termination of the single transistor to approach the input impedance to the 50 Ω in the Smith chart. This technique was utilized to be able to construct the input matching network with less components. In other words, SD technique simplifies the input matching network and using less components prevent adding up extra noise to the system. However, an optimum source inductor need to be added to the transistor; because greater inductance enhances the stability and increases the noise figure.

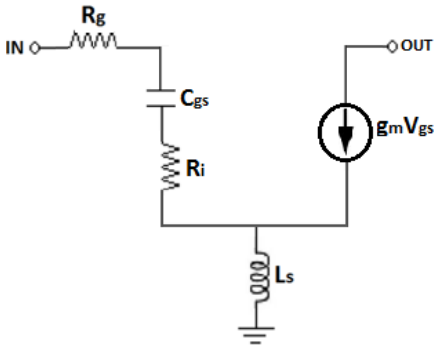

Figure 1. *The simplified equivalent circuit the common source topology*

The simplified schematic of the common source topology with source degeneration is shown in Figure 1. According to this equivalent circuit model, the input impedance of FET with an inductive source generation (Ls) is expressed as in Equation (2)

$$Z_{in} = R_g + R_i + \frac{g_m L_s}{C_{gs}} + \frac{1}{sC_{gs}}. \tag{2}$$

where R_g is the gate resistance, R_i is the intrinsic channel resistance, C_{gs} is the gate-to-source capacitance and g_m is the transconductance factor of the CE3512K2 FET. In the Equation (2), the value of the R_g gate resistance bounds up with the number and shape of gate finger and the value of the R_i, the intrinsic channel resistance bounds up with the channel geometry and contact metallization [7]. The F_{min} utilizing the Fukui equation for gallium arsenide (GaAs) FET can be calculated with using the Equation (3) [8]

$$F_{min} = 1 + \frac{2FL}{F_t}\sqrt{\frac{I_{opt}(R_g+R_s)}{E_c L}} \tag{3}$$

where I_{opt} is the optimum current (mA) for F_{min}, E_c is the peak velocity field (kV/cm); L is the gate length (μm), F and F_t are the operating and cutoff frequencies (GHz), respectively. According to the Equation (3), the F_{min} of the FET can be achieved with the packaged transistor just by the changing the biasing conditions to obtain the optimum current. In order to obtain the F_{min} condition, the 1st stage's drain current was set to 10 mA with a DC power dissipation of 20 mW.

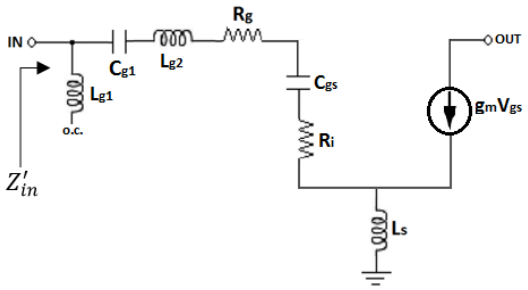

Figure 2. *The schematic of the 1st stage's input matching circuit*

Figure 2 shows the schematic of the 1st stage's input matching circuit. In the schematic design, the effects of the input matching network and inductive source degeneration were analyzed and it was observed that the 1st stage's input matching is compressing the input return loss (S_{11}) and NF with an agreement between them [7]. The simplified input impedance (Z'_{in}) of the LNA can be expressed as in the Equation (4)

$$Z'_{in} = R_g + R_i + \frac{g_m L_s}{C_{gs}} + \frac{1}{sC_{gs}} + \frac{1}{sC_1} + \frac{1}{sL_{g1}} + sL_{g2} \quad (4)$$

where L_{g1}, L_{g2} and C_{g1} are input matching components. The impedance of the input matching network was set to the complex conjugate of the optimum noise source reflection coefficient to achieve NF_{min}. In the Equation (4), the sum of the first three terms is the real part and it was seen that the L_s precisely have authority on the real part thereby abstained from utilizing any resistor so as not to increase the NF [7].

In the design, one of the significant specification is the stability. So as to enhance the stability of LNA, the gate biases of both stages were supplied on a series resistor (R_g) of 500 Ω and the parallel RC circuit was utilized at the input of the drain termination of the transistor. In the stability circuit, R_{st} (35 Ω) has a duty to decrease small signal gain in the lower frequencies and works as a second load in the higher frequencies. On the other hand, C_{st} (0.6 pF) plays a role as low reactance in lower frequencies and high reactance in the higher frequencies. Figure 3 shows the stability and bias circuit of the amplifier.

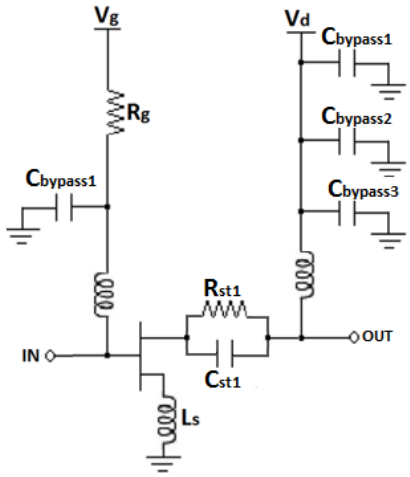

Figure 3. *The schematic of the stability and bias circuits*

The gate biases were supplied on RF choke inductor to choking the high frequency alternating current flowing to direct current (DC) power supply and bypass capacitor ($C_{bypass1}$) of 5.6 pF were connected near choke inductor to restrain the unwanted signal, which can be caused to the unwanted oscillations, from entering to the system. Moreover, a series R_g (500 Ω) was used at the gate bias to enhance stability. Besides, the drain biases were supplied for both stages on the RF choke inductor and parallel connected bypass capacitors $C_{bypass1}$, $C_{bypass2}$ and $C_{bypass3}$ whose values were 120 pF, 27 pF and 5.6 pF, respectively. Furthermore, serially connected DC block capacitors C_{g1}, C_{d1} and C_{d2}, whose values were 1.8 pF, to prevent the direct current flow through to the RF input and output ports [9]. Furthermore, the interstage matching topology was utilized between the 1st and 2nd stages for achieving the maximum power transfer to enhance gain and noise performance [10]. The interstage matching was constructed with the open stub and serially connected tapered transmission line and DC block capacitors. The 2nd stage's drain current was set to 15 mA with 2 V to enhance the linearity and the total power consumption of LNA was 50 mW. Figure 4 shows the schematic of the two-stage LNA.

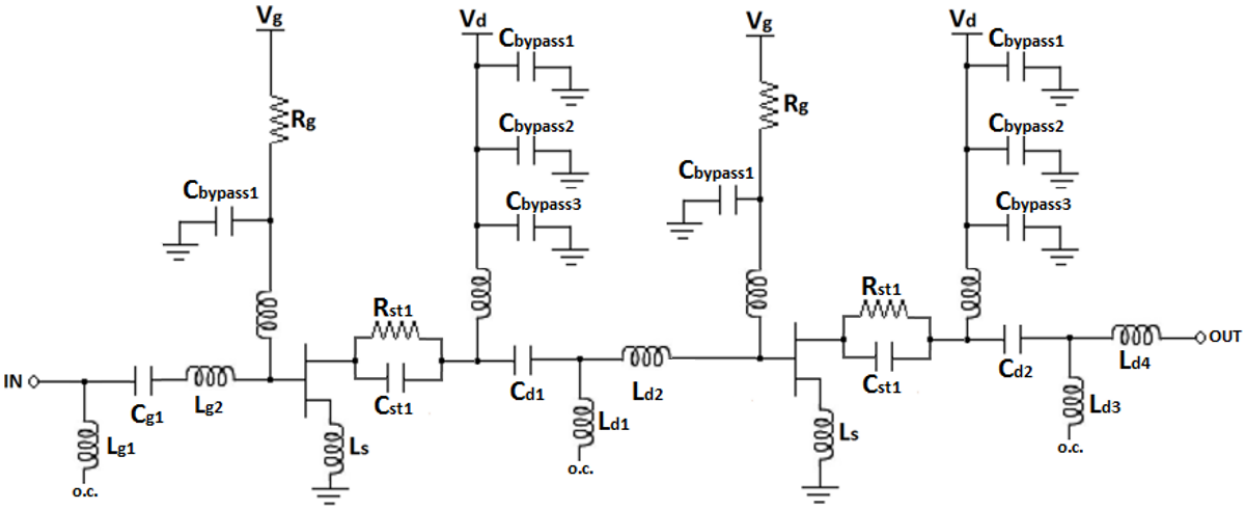

Figure 4. *The schematic of the two-stage LNA*

2.2. Electromagnetic Simulation Results

The electromagnetic (EM) analysis of the proposed LNA was achieved with utilizing the method of moment (MoM) in the ADS Momentum software. In EM simulations, both individual stages and two-stage LNA were stabilized and stability performance was checked with utilizing both k-factor and μ-factor tests. In the stability simulation results, it was observed that the design was unconditionally stable up to 20 GHz. Figure 5 shows the simulated stability results of the LNA.

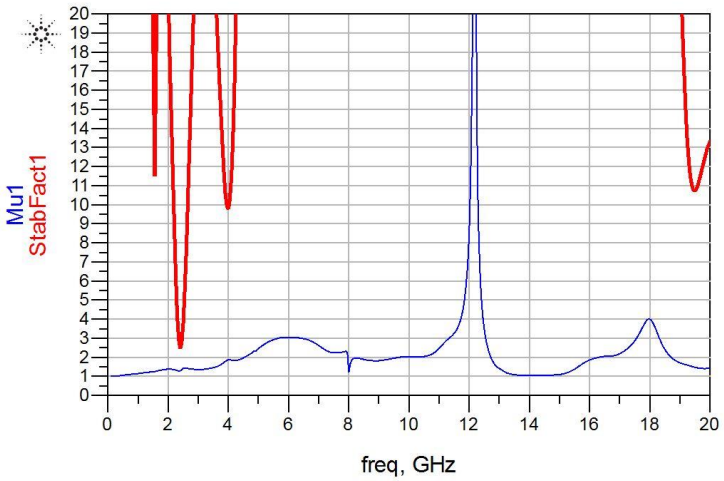

Figure 5. *Simulated stability results of the LNA*

Figure 6 shows the S-parameters simulation of the two-stage LNA design. In S-parameter simulation results, it was observed that the I/O return losses were lower than -15 dB and the small signal gain was higher than 23.2 dB over 7.25-7.75 GHz.

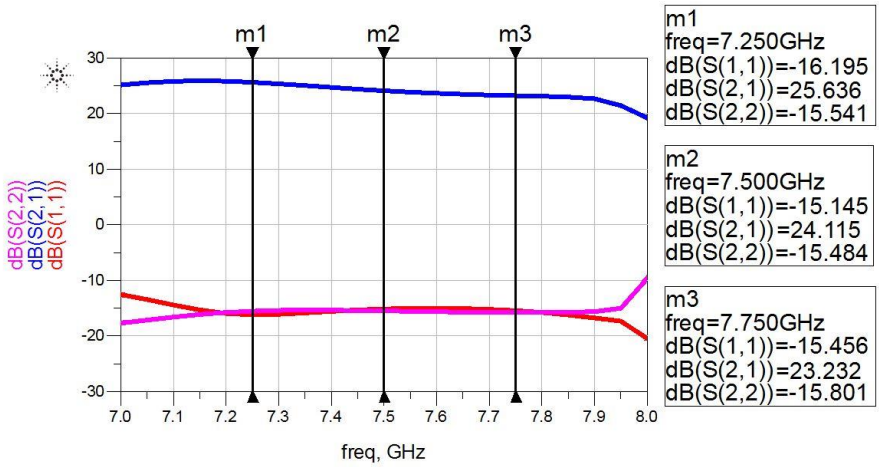

Figure 6. *Simulated S-parameters results of the LNA*

Figure 7 shows the simulated NF of the two-stage LNA design. In the noise figure simulation results, it was observed that the noise figure was lower than 0.7 dB over 7.25-7.75 GHz. Since the single transistor has ~0.3 dB NF performance, the inductive source, matching networks and the NF of 2nd stage of the LNA increases the NF up to 0.7 dB.

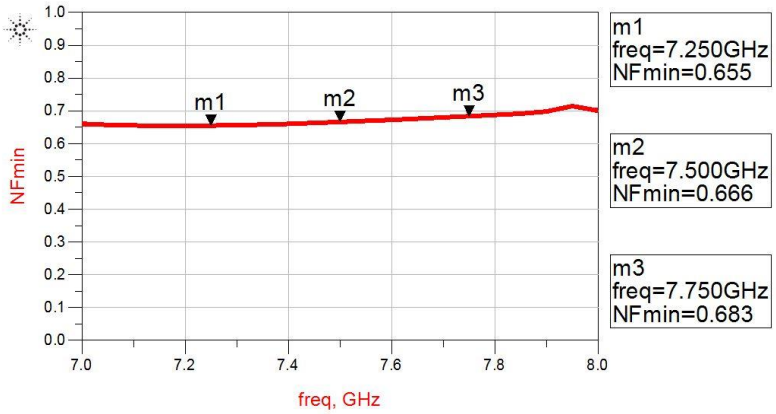

Figure 7. *Simulated noise figure result of the LNA*

Figure 8 shows the layout and photograph of the two-stage LNA. The proposed design was manufactured on a Rogers RT5880 substrate. The Rogers RT5880 substrate's thickness is 0.508 mm, the dielectric constant (ε_r) is 2.2 and the copper thickness is 35 μm. In addition Southwest end launch female SMA connectors were utilized on the measurements.

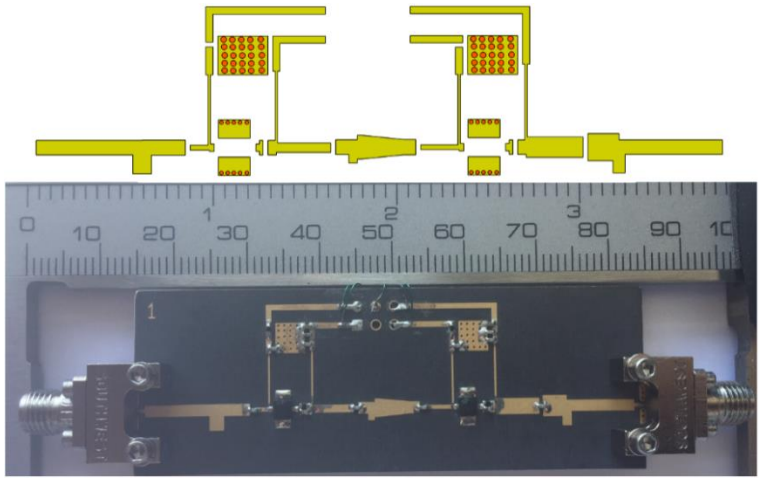

Figure 8. *Layout and Photograph of the LNA*

3. THE RESEARCH FINDINGS AND DISCUSSION

The S-parameters of the LNA were measured with utilizing Keysight N5244B PNA-X. In the S-parameters measurements, the LNA were biased with $2V_{ds}$ with a total drain current of 25 mA and the developed LNA is achieved 23.5±0.5 dB small signal gain in the frequency range of 7.25-7.75 GHz. In addition, the I/O return losses were lower than -13 dB and -11.5dB, respectively. The measurement results of S-parameters were given in the Figure 9.

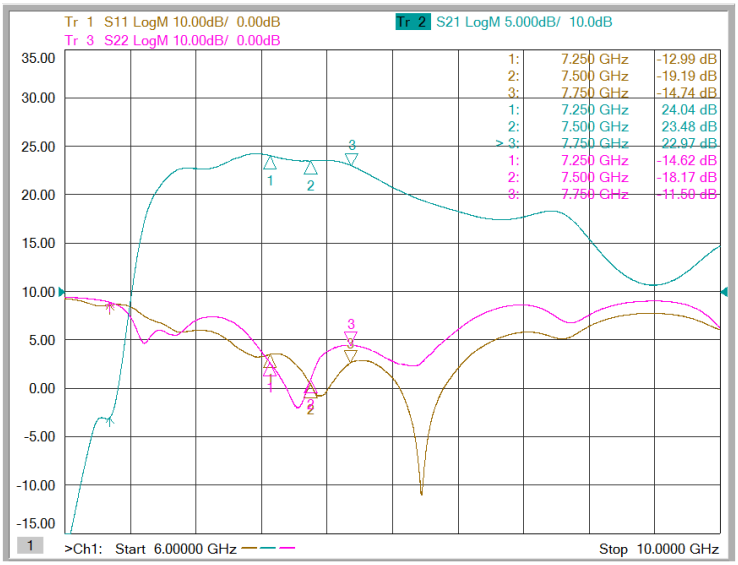

Figure 9. *Measured S-parameters of the LNA*

The NF of the LNA was measured with utilizing Keysight N5244B PNA-X with option 029 at ambient temperature. In NF measurements, the cold source method was utilized to measure the ultra-low noise amplifier with a lower uncertainty. The average NF was approximately 0.8 dB and NF was lower than 0.9 dB over 7.25-7.75 GHz. The variation in the simulated and measured NF is approximately 0.2 dB in the operating frequency bandwidth. Moreover, this variation can be caused by the manufacturing sensitivity and measurement uncertainties. The measured NF of the LNA is given in the Figure 10.

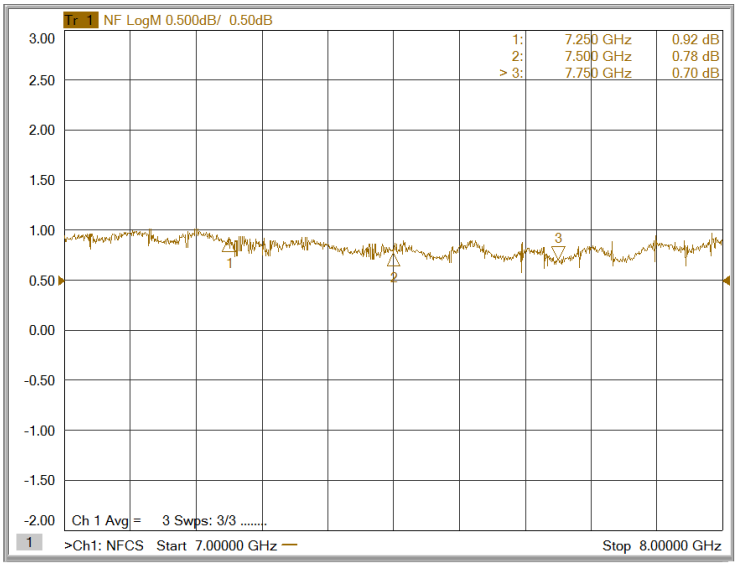

Figure 10. *Measured NF of the LNA*

In the P_{1dB} measurement, the input port of the LNA was connected to the Keysight N5182B Vector Signal Generator and input power was increased from -55 dBm to -5 dBm. In addition, the output of the LNA was

measured with utilizing the Rohde Schwarz FSW Signal & Spectrum Analyzer. In the measurements, the output power at 1-dB compression power was measured as +13 dBm and the gain was measured as 23 dB at the center frequency. The measured P_{1dB} of the LNA is given in the Figure 11.

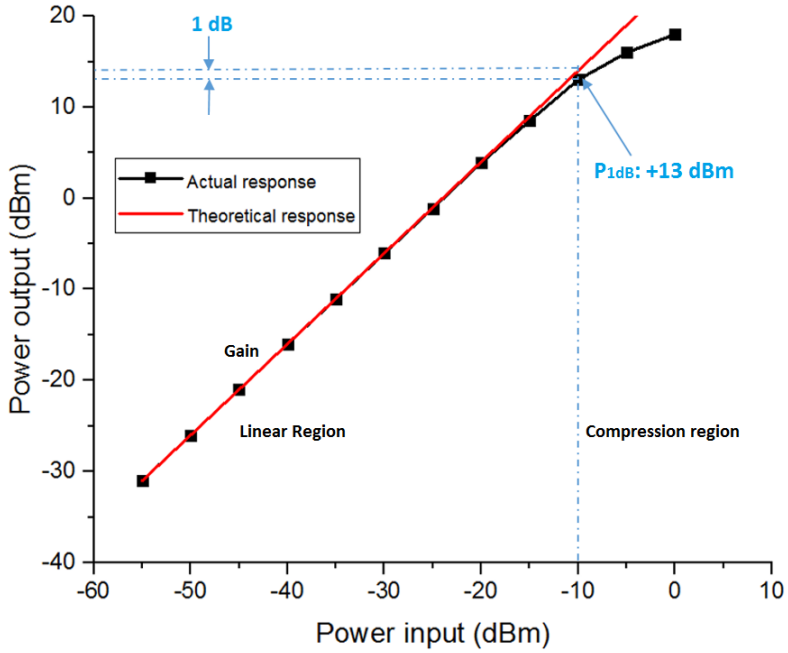

Figure 11. *Measured P_{1dB} of the LNA*

The intermodulation distortion measurement was done with utilizing Keysight N9030B Signal Analyser and two Keysight MXG Analog Signal Generators. In the measurement, two tone signals with equal amplitude but in different phases were applied to the input port of the LNA at the maximum input power of -35 dBm. The generated two tone signals with 1 MHz spacing were combined with an RF combiner. The measured C/I of the LNA was achieved -59 dBc at 7.5 GHz. Figure 12 shows the measured C/I of the LNA.

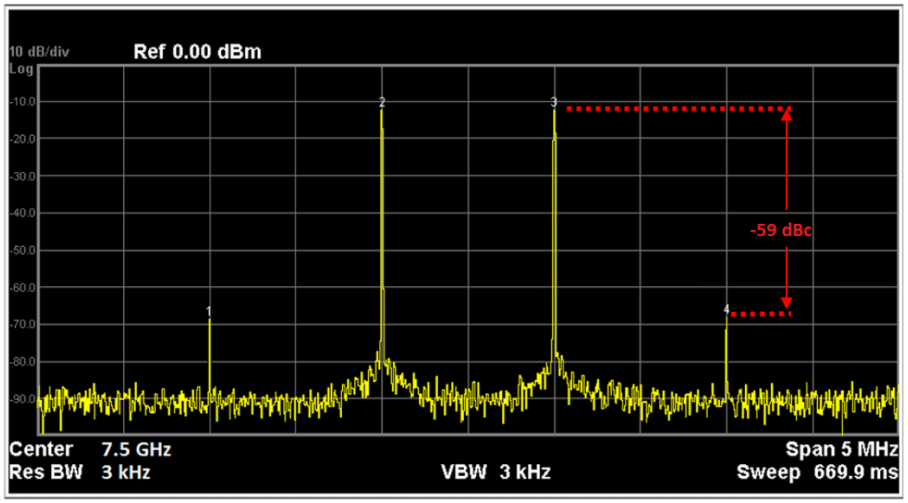

Figure 12. *Measured C/I of the LNA*

Figure 13 shows the measured and simulated S-parameters and NF of the LNA. It was observed that the simulated S-parameters for the operating frequency bandwidth was good agreement with the measurement results. However, it was observed that there were slight difference between the measurement and simulation results in the small signal gain and NF of the LNA. The measured small signal gain was ~1.5 dB less than the simulation results and the measured NF was ~0.2 dB higher than the simulated NF. These slight differences in the simulation and measurement results can be caused by the measurement uncertainties or the connectors that were utilized in the measurements.

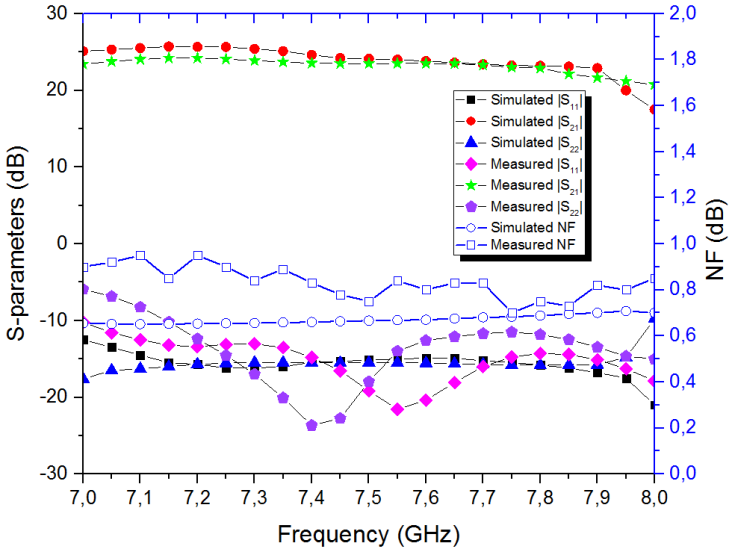

Figure 13. *Measured and Simulated S-parameters and NF of the LNA*

Table 1 shows the summary of the measured electrical specifications of manufactured X-band LNA at the room temperature.

Table 1. *Summary of measured electrical performances*

Specifications	Unit	Values
Operating Frequency	MHz	7250 – 7750
Minimum RF Power	dBm	-55
Small Signal Gain $\|S_{21}\|$	dB(min)	23.5 ± 0.5
Input Return Loss $\|S_{11}\|$	dB(min)	-13
Output Return Loss $\|S_{22}\|$	dB(min)	-11
Noise Figure	dB	0.8 ± 0.1
Gain Flatness	dBp-p	1.07
C/I	dBc	-59
P1dB	dBm	+13

Table 2 shows the comparison between the developed X-band LNA and recently presented LNAs in the literature. The noise figure and small signal gain performance of the developed LNA was better in NF and was compatible in small signal gain performance with low DC power consumption in the literature.

Table 2. *The comparison of X-band LNAs*

Ref.	Technology	# of stages	Bandwidth (GHz)	Gain (dB)	NF (dB)	PDC (mW)
[11]	0.1 µm GaAs pHEMT	2	3.8 – 19.8	>18.5	<2.0	40
[12]	0.15 µm GaAs pHEMT	3	3.2 – 14.7	>33.6	<1.3	45
[13]	0.15 µm GaN HEMT	-	9.0 – 11.0	>13.5	<2.2	1280
[14]	0.25 µm GaN HEMT	3	7.5 – 10.5	>25.0	<2.5	-
[15]	0.25 µm GaN HEMT	3	8.0 – 10.0	>24.0	<1.3	900
[16]	0.25 µm AlGaN/GaN HEMT	3	7.4 – 11.4	>23.0	<1.6	1200
[17]	0.2 µm GaAs pHEMT	3	1.5 – 11.7	>11.6	<4.8	10
[18]	0.15 µm GaAs pHEMT	4	3.0 – 15.0	>28.0	<2.5	200
[19]	0.15 µm GaAs pHEMT	2	3.1 – 8.0	>4.0	<5.0	-
[20]	0.25 µm InGaAs pHEMT	2	0.1 – 10.0	>19.0	<2.0	450
[21]	0.18 µm GaAs pHEMT	4	3.0 – 12.0	>15.2	<3.5	127
This work	GaAs FET	2	7.25 – 7.75	>23.0	<0.9	50

4. RESULTS

This article presents the results of the developed low cost X-Band LNA with sub-1-dB noise figure for SATCOM applications. The proposed LNA was utilized the common source topology with source degeneration topology to achieve the NF_{min} as well as high gain. In addition, an interstage matching were utilized to accomplish the maximum power transfer to enhance the small signal gain. Moreover, separate biasing lines and parallel RC stability circuit on the output was utilized for the circuit stabilization. The developed LNA was manufactured on Rogers RT5880 substrate and commercially available CE3512K2 FET, 0402 packaged SMD resistor and capacitors were utilized in the LNA. In the measurement, the developed LNA has a gain of 22.5 ± 0.5 dB in the frequency bandwidth while the input and output (I/O) return losses were lower than -13 dB and -11 dB, respectively. The measured NF was better than 0.9 dB over 7.25-7.75 GHz and the carrier to interference was -59 dB at 7.5 GHz. The developed LNA is suitable for SATCOM applications because of its proven technology, low-cost and high electrical performance.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

REFERENCES

[1] Dai, L.L., Choi, J., Chan, V.W., "Communication satellites–technologies and systems", Encyclopedia of Life Support Systems (EOLSS), United Nations Educational, Scientific and Cultural Organization, 1-43, (2007).

[2] Knopp, A., Schwarz, R.T., Lankl, B., "MIMO system implementation with displaced ground antennas for broadband military SATCOM", MILCOM 2011 Military Communications Conference, Baltimore, 2069-2075, (2011).

[3] Florian, C., Resca, D., Biondi, A., Scappaviva, F., "An X-to-Ka band MMIC up-converter in GaAs pHEMT technology for Ka-band broadband satellite communications", Microwave and Optical Technology Letters, 56(11): 2649-2656, (2014).

[4] Kwon, K., Kim, S., Son, K.Y., "A hybrid transformer-based CMOS duplexer with a single-ended notch-filtered LNA for highly integrated tunable RF front-ends", IEEE Microwave and Wireless Components Letters, 28(11): 1032-1034, (2018).

[5] Montazeri, S., Wong, W.T., Coskun, A.H., Bardin, J.C., "Ultra-low-power cryogenic SiGe low-noise amplifiers: Theory and demonstration", IEEE Transactions on Microwave Theory and Techniques, 64(1): 178-187, (2015).

[6] Arican, G.O., Akcam, N., Yazgan, E., "Ku-band GaAs mHEMT MMIC and RF front-end module for space applications", Microwave Optical Technology Letter, 63(2): 417-425, (2021).

[7] Jarndal, A.H., Bassal, A.M., "A broadband hybrid GaN cascode low noise amplifier for WiMax applications", International Journal of RF and Microwave Computer-Aided Engineering, 29: e21456, (2019).

[8] Oxley, C.H., "Calculation of minimum noise figure using the simple Fukui equation for gallium nitride (GaN) HEMTs", Solid State Electronics, 45(1): 677-682, (2001).

[9] Venkatesh Murthy, B.T., Srinivasa Rao, I., "High-gain sub-decibel noise figure low noise amplifier for atmospheric radar", Microwave Optical Technology Letter, 58(7): 1618-1622, (2016).

[10] Arican, G.O., Akcam, N., Yazgan, E., "Ku-band MMIC LNA design for space applications", International Conference on Electrical and Electronics Engineering (ICEEE), Istanbul, Turkey, 274-278, (2019).

[11] Chen, Y.C., Wang, Y., Chiong, C.C., Wang, H., "An ultra-broadband low noise amplifier in GaAs 0.1-μm pHEMT process for radio astronomy application", In 2017 IEEE International Symposium on Radio-Frequency Integration Technology, Seoul, Korea, 80-82, (2017).

[12] Wang, Y., Chiong, C.C., Nai, J.K., Wang, H., "A high gain broadband LNA in GaAs 0.15-μm pHEMT process using inductive feedback gain compensation for radio astronomy applications", Proceedings of the IEEE International Symposium on Radio-Frequency Integration Technology, Sendai, Japan, 79-81, (2015).

[13] Kobayashi, K.W., Campbell, C., Lee, C., Gallagher, J., Shust, J., Botelho, A., "A reconfigurable s-/x-band GaN cascode LNA MMIC", Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium, Miami, USA, (2017).

[14] Kim, B., Gao, W., "X-band robust current-shared GaN low noise amplifier for receiver applications", Proceedings of the 2016 Compound Semiconductor Integrated Circuit Symposium, Austin, USA, (2016).

[15] Vittori, M., Colangeli, S., Ciccognani, W., Salvucci, A., Polli, G., Limiti, E., "High performance X-band LNAs using a 0.25 μm GaN technology", Proceedings of the 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Giardini Naxos, Italy, 157-160, (2017).

[16] D'Angelo, S., Biondi, A., Scappaviva, F., Resca, D., Monaco, V.A., "A GaN MMIC chipset suitable for integration in future X-band spaceborne radar T/R module Frontends", Proceedings of the 21st International Conference on Microwave, Radar and Wireless Communications (MIKON), Krakow, Poland, (2016).

[17] Yousef, K., Jia, H., Pokharel, R., Allam, A., Ragab, M., Yoshida, K., "A 2–16 GHz CMOS current reuse cascaded ultra-wideband low noise amplifier", Proceedings of the 2011 Saudi International Electronics, Communications and Photonics Conference (SIECPC), Riyadh, Saudi Arabia, (2011).

[18] Zhang, H., Qian, G., Zhong, W., Liu, C., "A 3–15 GHz ultra-wideband 0.15-μm pHEMT low noise amplifier design", Proceedings of International Conference on Communication Systems (ICCS), Shenzhen, China, (2016).

[19] Wu, C.S., Chang, C.H., Lin, T.Y., Wu, H.M., "A ultrawideband 3–10 GHz low-noise amplifier MMIC using inductive-series peaking technique", Proceedings of the 2011 International Conference on Electric Information and Control Engineering, Wuhan, China, 5667-5670, (2011).

[20] Memioglu, O., Gundel, A., "A High Linearity Broadband Gain Block/LNA MMIC with Diode Predistortion in GaAs pHEMT Technology", Proceedings of the 18th Mediterranean Microwave Symposium (MMS), Istanbul, Turkey, 120-123, (2018).

[21] El Bakkali, M., Touhami, N.A., Elhamadi, T.E., Elftouh, H., Lamsalli, M., "High gain 0.18 μm-GaAs MMIC cascode-distributed low-noise amplifier for UWB application", Microelectronics Journal, 108: 104970, (2021).