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# The Short Channel and Quantum Confinement Effects on Transfer Characteristics of Si NWMOSFET Depending on the Gate Length and Temperature

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**ABSTRACT:** With advancements in nanomaterial synthesis, semiconductor device technology entered a new era with nanotechnology. In fact, quantum effects such as confinement and tunneling have played a significant role in device characteristics. In this work, we have investigated quantum ballistic transport properties of Si nanowire MOSFET (Si NWMOSFET) with 4 nm gate length. Since gate length is shorter than the electron wavelength in our Si NWMOSFET, ballistic transport in one dimension (1D) is expected to be the dominant mechanism for carrier transport. Therefore, the parameters which are crucial for efficient MOSFET operation such as gate length, temperature, gate voltage have been simulated using the density gradient method to present quantum confinement effect on device transfer characteristics. We have found that Si NWMOSFET has an $I_{on}/I_{off}$ ratio > $10^8$, which is close to ideal value for similar nano MOSFETs. Moreover, due to short channel, intersubband scattering can deteriorate 1D ballistic transport properties of Si NWMOSFET, especially in low temperatures.

**Keywords:** Si NWMOSFET, ballistic transport, 1D transport, short channel effect, quantum confinement

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## INTRODUCTION

Field-effect transistors (FETs) consisting of three terminals, source, drain and gate electrodes, are crucial components of CMOS (Complementary Metal Oxide Semiconductor) devices to achieve energy efficient high speed switching. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with long channel has transport characteristics based on a drift-diffusion model in which charge carriers (electrons and holes) are scattered by phonons, impurities or carriers themselves. These scattering events eventually deteriorate transport characteristics resulting in a decrease of drain current. Recent progress in top-down material synthesis and adaptation in current electronic devices have enabled the realization of nanowire structures in device applications such as FETs, memories(Lim et al., 2017), sensors(Li et al., 2004), light-emitting diodes(Q. Peng et al., 2004), and photovoltaic cells(Peng et al., 2005).

Notably, Si nanowire FETs (Si NWFET) are attracting much interest due to being the most compatible candidate for mainstream CMOS devices since today's conventional Si CMOS integrated circuit technology can readily be a production line to fabricate Si NWFET with the advantage of low cost. Particularly, Si NWFETs can push forward performance of scaled down CMOS. Recent experimental studies have demonstrated that Si NWFETs with ~10 nm or smaller nanowires using gate-all-around and(Singh et al., 2008) multigate or stacked architecture (Nair & Alam, 2007; Ng et al., 2009) have higher on-current than planar MOSFETs. Moreover, Si NWFETs have naturally quasi one-dimensional conduction because of restricted degree of freedom of carriers in nanowire apart from bulk Si. Owing to this restriction, mobile electrons in the conduction (or valence) bands of the Si NWFET form Bloch waves that must fit in the channel. This restricts momentum and propagation of the Bloch waves, enforced by periodic boundary conditions, in NW. Thus, all carriers are uniformly driven by the gate voltage leading to the suppression of current leakage (Bangsaruntip et al., 2009; Chhowalla et al., 2016).

However, up to now quantum confinement effects were mostly observed experimentally at ultralow temperatures within relatively large channel diameters (Trivedi et al., 2011). To be able to apply quantum characteristics to real device applications, the size of the channel must be sub-10 nm so that the quantum size effect can cope with thermal broadening. Also, Si NWFETs with diameters as small as 3 nm have been fabricated lithographically (top-down approach) on silicon-on-insulator (SOI) substrates (Singh et al., 2008; Trivedi et al., 2011) and their performance was enhanced at 300°K for sub-5 nm top-down patterned p-Si [110] NW FETs (Yi et al., 2011).

However, shorter channel lengths cause higher off-state currents, which are not desired, since some charge carriers between the source and drain electrodes cause current at such short channel lengths even under gate voltage that tends to suppress the current flow. Also, higher off-state currents cause higher static power, and consequently heat dissipation and temperature of the device increases(Colinge, 2004; Ferain et al., 2011). Electronic band structure (Neophytou, Paul, & Klimeck, 2008; Neophytou, Paul, Lundstrom, et al., 2008) and mobility (Buin et al., 2008; Jin et al., 2007) of Si nanowires are known to be highly sensitive to quantum confinement of carriers in sub-10 nm Si nanowires, even at room temperature. Due to this quantum confinement, mobility of carriers is high (Kim & Lundstrom, 2008) and multiple electronic sub-bands can contribute to the electronic conduction giving rise to exceptional conduction. However, quantum confinement induced effects can vanish at high temperature or drain bias (Jin et al., 2007) since carriers experience inter sub-band scattering under high drain bias. For practical reasons Si NWFETs should have $I_{on}/I_{off}$ ratio at least $10^6$ and $I_{off}$ should be lower than the measurement limit (~$10^{-15}$A) at room temperature with millivolt range drain bias. Very recently, p-MOSFET made of Si nanowire have shown to exhibit p-type transfer characteristics with $I_{on}/I_{off}$ ratio greater than $10^6$,

subtreshold slope (SS) less than 100 mV/decade, $I_{off}$ lower than the measurement limit (~$10^{-15}$A), and threshold voltage ($V_T$) of less than 2V (Trivedi et al., 2011; Zhang et al., 2018). Additional factors such as nanowire diameter, cross-sectional shape, crystal orientation, mechanical stress, and surface properties (Jung & Shin, 2013) of Si nanowires also significant to establish required $I_{drain}$-$V_{drain\text{-}source}$ ($I_d - V_d$) characteristics of Si NWFETs. In turn, these factors also change the electronic band structure of Si nanowires affecting the essential device transfer characteristics (Nehari et al., 2005).

Moreover, Si nanowire MOSFET with cylindirical gate all around architecture with gate lenght of 7 nm has shown to have higher $I_{On}/I_{Off}$ (~$4 \times 10^8$). Also gate all around nanowire Si MOSFET with gate lenght 16 nm has a slightly better short channel control compared to similar geometric size circular nanowires (Cho et al., 2008).

Very Recently, Si NWFETs has shown to exhibit gate dependence g-factor due to hole spins and can be operated as few-hole quantum dot. This can enable manipulation of hole spin resonance with microwave modulation on gate, offering fast electrically driven qubit systems (Voisin et al., 2016).

Consequently, considering Si NWFETs in integrated circuits, parameters such as Si NW channel length/width, on-off bias-gate voltage range, and temperature are utterly relevant for circuit designers to address the challenges of nano electronics. But these parameters all depend on electronic structure of Si NW. Still, device characteristics of Si NWMOSFETs having different geometrical properties and crystal symmetries are technologically and scientifically crucial to guide high-end experimental studies. Therefore, here we have studied quantum ballistic transport properties of sub-10 nm Si nanowire MOSFET (Si NWMOSFET) with [2-4 nm] gate length using state of art density gradient method. Since this method takes into consideration electronic structure effects implied in effective masses, we have compherensively unveiled quantum transport characteristics of Si NWMOSFET with different gate lengths. We have calculated quantum ballistic transport properties depending on channel characteristics and temperature upon applied different gate and bias voltage to shed light on optimized device parameters governed strictly by electronic structure as such that short channel effects can be controlled electrostatically via gate.

## MATERIALS AND METHODS

### Structural Properties of Simulated Si NWMOSFET

The channel of the simulated Si NWMOSFET is formed by an intrinsic Si nanowire with a 3.2 nm square cross section, surrounded by an oxide layer of thickness 0.6 nm as shown in Figure 1. $SiO_2$ oxide layer determines the characteristic length of FET, thus it has been modeled explicitly. The oxide layer behaves as a quantum barrier (~3.15 eV) for the conduction band of Si [100] NW, which has 6 degenerate conduction bands splitting into two non-equivalent valleys with different effective masses. The initial length of the channel is 4 nm. The simulated Si NWMOSFET is confined in both [001] (top) and $[11\bar{0}]$ (sides) directions. This structure is well compatible with experimentally synthesized Si nanowires (Bollani et al., 2019).

Thus, the carriers (holes and electrons) are free to move through the channel only in the [110] direction in 1D regime. This restriction in moving direction leads to quantized energy level of electronic subbands. Since electronic structure of the channel strongly depends on the boundary conditions of quantum confinement, hence closely related to the geometric parameters of Si NWMOSFET, internal geometric parameters of NW affect the final transfer outputs of Si NWMOSFET. The simulated Si NWMOSFET has 3.2 nm width, which is very close to the wavelength of an electron (~10 nm), therefore Si NWMOSFET is expected to show ballistic conductance along the channel. Source and drain are made

of n-type doped Si with doping concentration of $10^{20}$ $cm^{-3}$. As the transfer performance of Si NWMOSFET is determined by the aspect ratio of the channel length (L) and channel width (W), we have investigated the MOSFET characteristics for varying L, under different drain bias and gate voltages.

From technological point of view, one of the most important challenges in minimizing MOSFET devices is to maintain the electrostatic dominance of the gate over the channel while suppressing short channel effects. In this study, the effect of the gate length, temperature, and gate voltage will be examined using density gradient method to model Si NWMOSFET characteristics by including quantum confinement effect. In addition, source and drain contacts are modeled as semi-infinite and in internal equilibrium. The Fermi levels for source and drain differ by the applied voltage $V_d$. Our approach also can be presented as a capacitive model as shown in Figure 1(a). In this model, capacitors are formed between each of three electrodes of the MOSFET and the channel competes to get electrostatic dominance over the channel. At atomic scale, dispersive character of the conduction band of Si NW changes depending on the applied gate voltage, leading to distinctive behavior of carriers and in turn device transfer outputs.

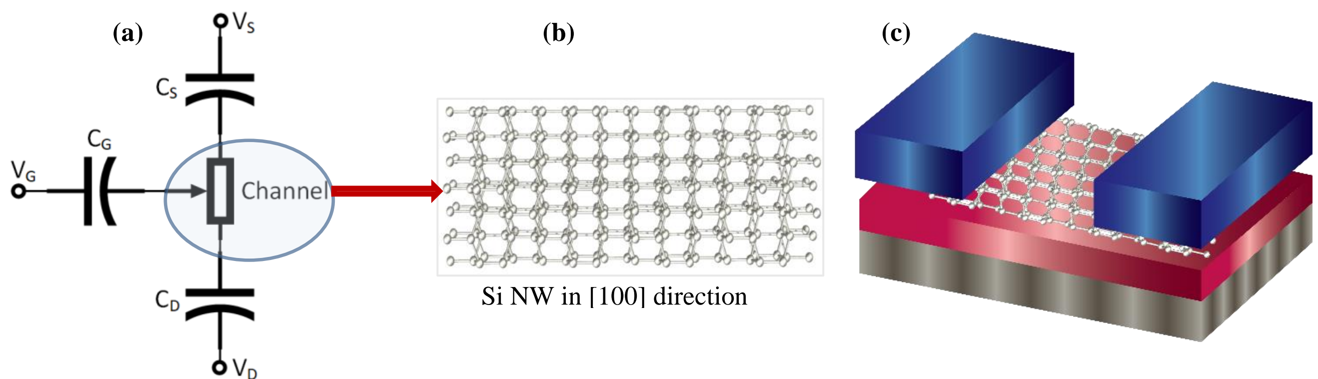


**Figure 1** Si NWMOSFET circuit model. Cd, Cg, Cs are capacitances and Vd, Vg, Vs are voltages of drain, gate and source, respectively. (b) Atomic scale model of Si NW. It constitutes the channel of MOSFET (c) Si NWMOSFET with source and drain at top (gate is not shown for clarity)

**Table 1**. Parameters used in Si NWMOSFET device simulation using density gradient method. $m_0$ is rest electron mass ($9.10938356 \times 10^{-31}$kg)

| **Parameters used in Si NWMOSFET simulation** | | | | | | |
|---|---|---|---|---|---|---|
| **Channel Length (nm)** | **Doping concetration (source/drain) ($cm^3$)** | **Effective mass (in x direction)** | **Effective mass (in z direction)** | **Gate-metal work function(V)** | **Temperature (°K)** | **Oxide layer thickness (nm)** |
| 4.0 | $10^{20}$ | $0.8 \cdot m_0$ | $0.5 \cdot m_0$ | 4.5 | 300 | 0.6 |
| 2.2 | $10^{20}$ | $0.8 \cdot m_0$ | $0.5 \cdot m_0$ | 4.5 | 77 | 0.6 |

## Density Gradient Method

Density gradient (DG) method is particularly drift diffusion method with quantum confinement effects and well suited enough to engineer semiconductor devices in nanoscale (Ancona, 2011). Therefore, we have employed the DG method with quantum confinement effect to understand short channel effects and transfer characteristics of Si NWMOSFET. In this regard, Poisson's equation is solved iteratively and equation of state of electron (or hole) depends not only on density but also the gradient. That makes Density Gradient method suitable to calculate quantum effects in low dimensional

systems. Since applied drain and gate voltages ($V_d$ and $V_g$) control the occupation of the allowed electronic states that can contribute to the current, the density of mobile carriers should be determined to understand and to tune output characteristics of NWMOSFETs. In addition, the density of mobile carriers in the channel dictates the channel potential as given in Eqn. (1). This channel potential changes depending on the carrier concentration in the channel. So, in order to determine the channel potential; Poisson's equation describing the relationship between charge concentration and channel potential must be solved self-consistently.

$$\nabla \cdot (\epsilon_s \nabla V) = -\rho \quad (1)$$

Here, $\rho$ is charge density (C/m$^3$), $\epsilon_s$ permittivity (F/m) and $V$ is the electric potential. The charge density has contributions from hole, electron, and ionized donor and acceptor concentrations as given in Eqn. (2).

$$\rho += q(p - n + N_d^+ - N_a^-) \quad (2)$$

$$\mathbf{J}_n = q\, n \left( \mu_n \nabla E_{fn} + \left( \frac{(E_c - E_{fn})\mu_n + Q_{th,n}}{T} \right) \nabla T \right) \quad (3)$$

$$\mathbf{J}_p = q\, p \left( \mu_p \nabla E_{fp} + \left( \frac{(E_v - E_{fp})\mu_p + Q_{th,p}}{T} \right) \nabla T \right) \quad (4)$$

Electron and hole current densities are calculated using Eqn. (3-4). $E_c$ and $E_v$ are the conduction band and valance band edges, $Q_{th,n}$ and $Q_{th,p}$ are non-equilibrium thermal diffusion coefficients (m$^2$/s), and $T$ is the temperature.

$$E_c = -(V + \chi_0) \quad , \quad E_v = -(V + \chi_0 + E_g) \quad (5)$$

The conduction band edge and valance band edges depend on the electric potential of the device ($V$) as given in Eqn. (5). Here, $\chi_0$ is the electron affinity of Si and $E_g$ is the bandgap of Si NW. In DG theory, carrier concentrations are written in terms of quantum potentials as given in Eqn (6-7) using gradients of quantum potentials. These potentials are quantum corrections to incorporate quantum confinement in the channel along the circumference of wire and along the radial direction of Si NW.

$$\nabla \cdot \left( \mathbf{b}_n^{DG} \cdot \nabla \sqrt{n} \right) = \frac{\sqrt{n}}{2} \left( +E_c - E_{fn} + \phi_n - \frac{k_B\, T}{q} \ln(Nc[m]^3) \right) \quad (6)$$

$$\nabla \cdot \left( \mathbf{b}_p^{DG} \cdot \nabla \sqrt{p} \right) = \frac{\sqrt{p}}{2} \left( +E_c - E_{fp} + \phi_p - \frac{k_B\, T}{q} \ln(Nv[m]^3) \right) \quad (7)$$

In Eqn. (6-7), $E_{fn}$ and $E_{fp}$ are quasi Fermi levels and $\mathbf{b}_n^{DG}$, $\mathbf{b}_p^{DG}$ effective mass tensors for transport directions and should be gathered from Schrödinger type calculations to include quantum confinement effects in short channels properly. Because in the ballistic (quasi-ballistic) transport regime, the mean free path of carriers (λ) is longer than (similar to) L; charge carriers are only scattered by boundaries of the NW, giving rise to only contact resistance during electronic transport. Also, $\phi_n$ and $\phi_p$ are related to n and p, respectively as given in Eqn. (8).

$$n = e^{\frac{q\phi_n}{k_B\, T}} \quad , \quad p = e^{\frac{q\phi_p}{k_B\, T}} \quad (8)$$

The transverse and longitudinal effective masses of Si NW have been gathered from (Stanojević et al., 2010) for similar Si NW. Parameteres used in the simulation have been given in Table 1.

## RESULTS AND DISCUSSION

### Quantum Confinement Induced Transfer Characteristics of Si NWMOSFET

It is known that Si NW with a diameter of ~3 nm is a direct semiconductor with a direct bandgap of 1.619 eV and its electronic band structure strongly depends on the nanowire width. The energy separation of discrete subbands (ΔE) in electronic band structure changes with the Si NW diameter (Luisier et al., 2006). For Si NW with a diameter of 3.2 nm, the energy difference between two band minima can be taken as 100 meV, which is calculated using tight-binding model (Stanojević et al., 2010). Moreover, confinement-induced 1D transport behavior is observable provided that the source−drain bias $(qV_d)$ is smaller than $\Delta E$ subband separation energy.

Although short channel length can give rise to ballistic 1D transport in Si NWMOSFET channel, this ballistic transport can be deteriorated via intersubband scattering especially in low temperatures. Due to short channel length, quantum well is formed in the channel and this quantum confinement potential localizes carriers in the channel. With this confinement potential, energy quantization occurs and creates an infinite barrier against the movement of electrons normal to the x-y plane. Nevertheless, applying gate voltage changes this confinement potential, allowing more carriers to be injected into channel with applied gate voltage. Also, temperature can significantly alter the height of this quantum confinement potential. Figure 2 and Figure 3(a) show that lowering temperature to liquid nitrogen (77 K) increases the height of the quantum confinement potential. However, applying gate voltage has a drastic effect on the height of confinement potential even at room temperature as such that gate voltage lowers the confinement potential as depicted in Figure 2(a) and Figure 3(c). Lowering the confinement potential enables more carriers to be injected into channel upon application of gate voltage. At zero gate voltage, no conductive path from source to the drain is avaliable so that no tunneling current can survive as opposite to Si NWMOSFET with 15 nm gate length in which the channel can not be fully depleted by the gate (Lim et al., 2017).

In addition, temperature also enables carriers to be mostly localized towards the gate (z- direction) as shown in Figure 3 (b). This suggests that the possible thermionic emission of carriers into gate can increase as temperature increases, allowing trapping/detrapping in the barrier material. Because, at high temperatures, electron concentration along z-direction penetrates more into the gate oxide region. Gate length also determines the electron concentration in the transport direction (x-direction) throughout the channel.

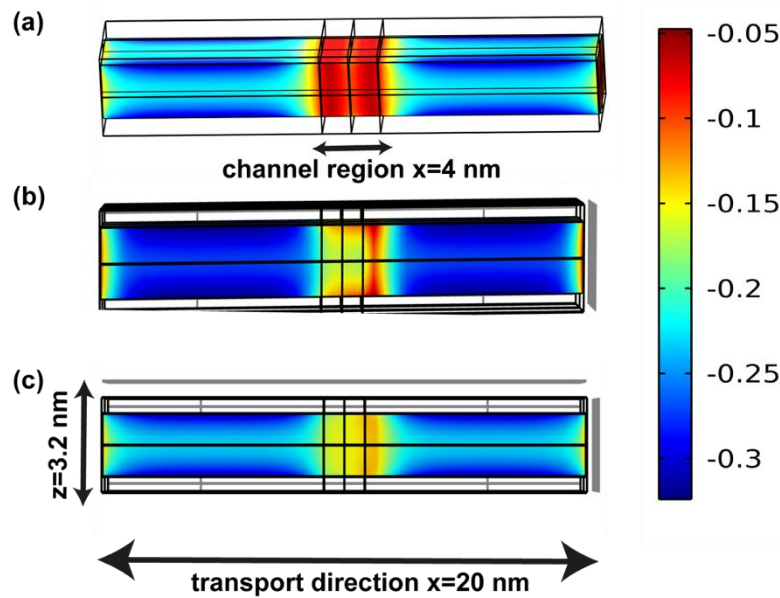


**Figure 2** The change of quantum potential in Si NWMOSFET along the channel for (a) $V_g = 0\ V, V_d = 0\ V$, width=3.2 nm, $L_x = 4$ nm, and temperature T=300°K, (b) $V_g = 0.4\ V, V_d = 0.6\ V$ and T= 77°K, (c) $V_g = 0.4\ V, V_d = 0.6\ V$ and T=300°K

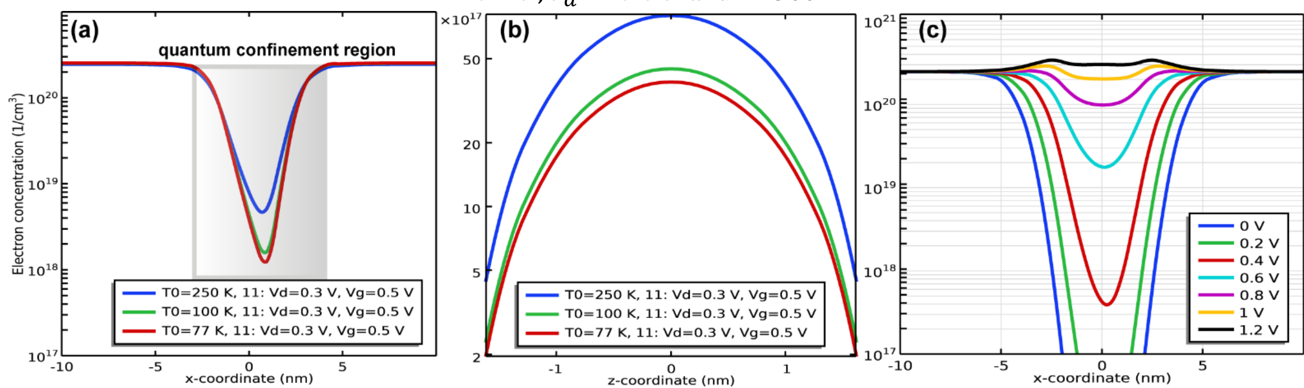


**Figure 3** Electron concentration (1/cm$^3$); (a) along the transport direction (x coordinate) (b) towards the oxide barrier direction (z coordinate) for varying temperature, $V_d$ and $V_g$'s. (c) Electron concentration in transport direction depending on the applied gate voltage

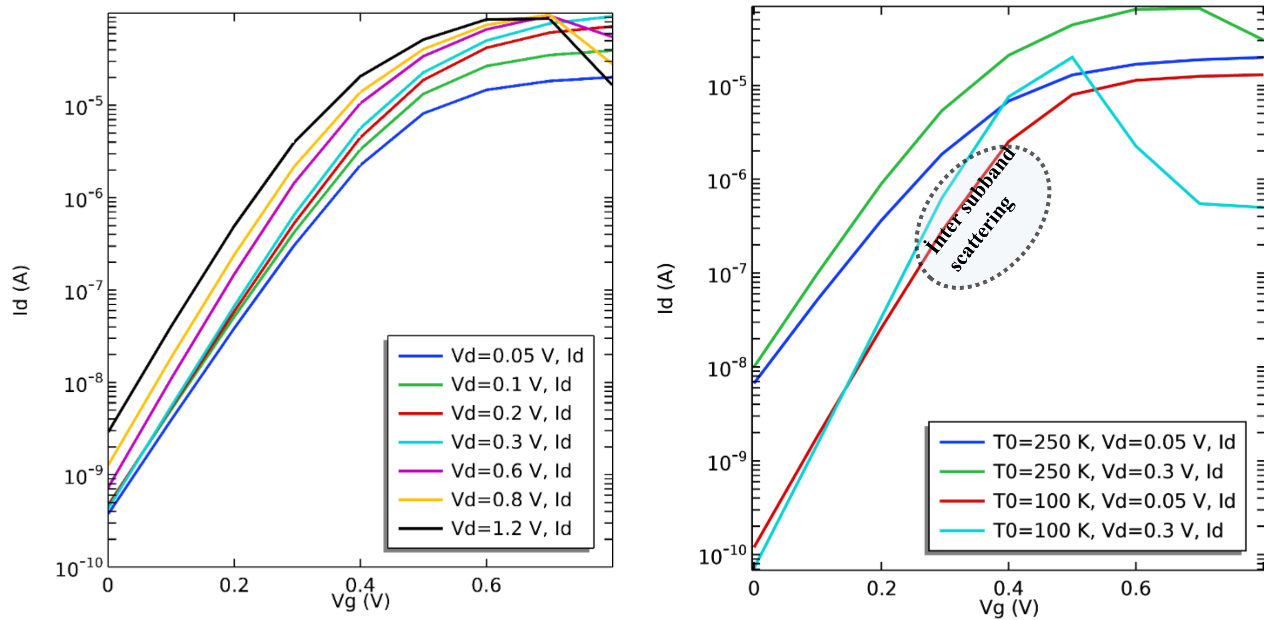


**Figure 4** Change of $I_d$ as a function of $V_g$ in log scale for different values of $V_d$ under varying gate voltages and at (a) room temperature (b) 100°K and 250°K for Si NWMOSFET with a channel length of 4 nm

We have also explored transfer characteristics to present the performance of Si NWMOSFET. Figure 4(a) demonstrates that the room-temperature $I_d - V_g$ characteristics are similar to those of an ordinary MOSFET except for the kinks in higher drain voltages. These kinks can be attributed to ballistic behavior of the Si NWMOSFET as confirmed with experimental (Cho et al., 2008) and theoretical (Kim & Lundstrom, 2008) studies for NWFETs. At a fixed drain voltage, varying the gate voltage changes the number of electron energy levels that can contribute to the current, because the band edge states are capacitively coupled to the gate electrode (Tsuchiya et al., 2006). Thus, conduction band edges come closer to the Fermi level as the drain voltage increases, so the number of current carrying modes in the electronic structure increases, consequently, $I_d$ increases. Moreover, off state current is on the order of $10^{-9}$ A for lower drain voltages but off state current slightly increases with increasing drain voltages. It should be noted that our Si NWMOSFET has an $I_{on}/I_{off}$ ratio on the order of $10^8$. This value is very close to ideal novel MOSFET device (Chhowalla et al., 2016). But this ratio changes with the swing of gate potential, which is still an eminent problem for current MOSFETs.

The subthreshold swing (SS) can be extracted from $I_d$–$V_g$ curves in the log scale. The SS values are for our Si NWMOSFET as high as 85 mV/dec, which is quite high as compared to GaN NWMOSFETs with similar geometry (Thingujam et al., 2020).

On the other hand, $I_d - V_g$ characteristics of Si NWMOSFET change with temperature as shown in Figure 4(b). At low temperatures, the current remains lower than that at higher temperatures, as can be seen from the log scale. We would expect that mobility increases at low temperatures because of reduced phonon scattering, thus, the current increase would be expected. However, the magnitude of the current increases as temperature goes up to 250°K due to reduction of intersubband scattering. Thus, the impact of the intersubband scattering becomes less significant as the temperature increases. In particular, drain voltage of 0.05 V is very close to ΔE for 4nm Si NWMOSFETs, suggesting possible intersubband scattering in low voltages.

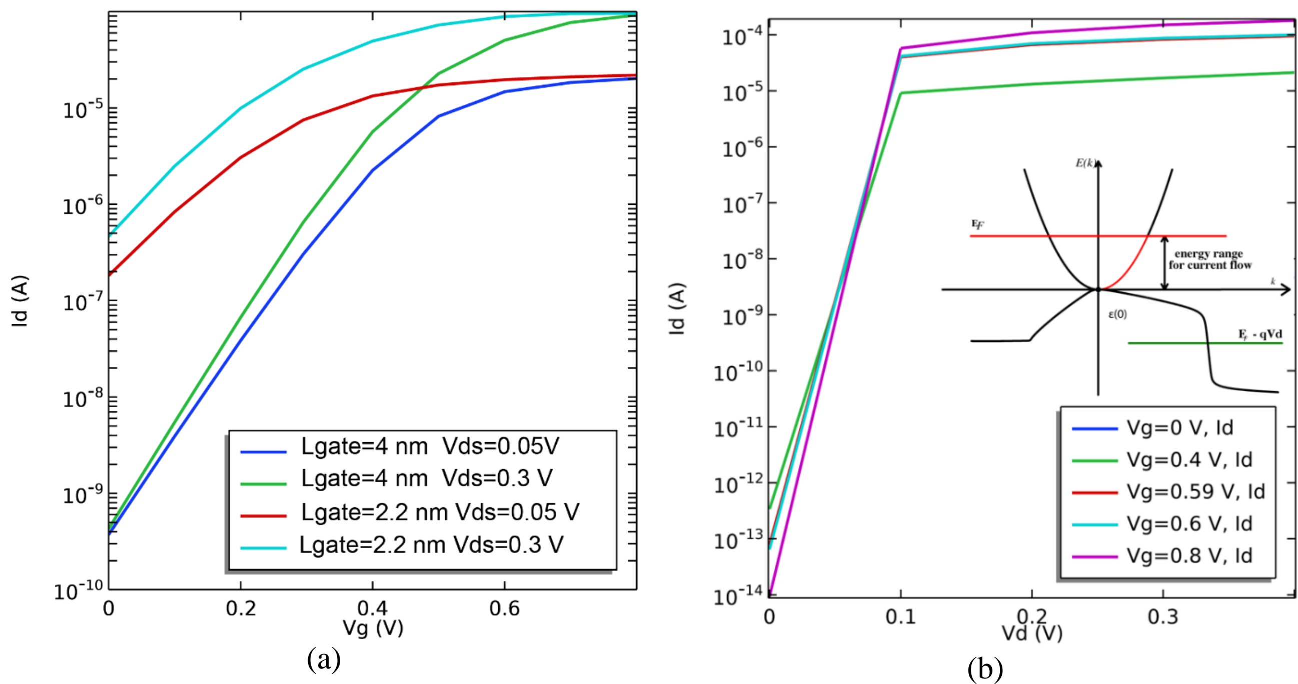


**Figure 5** $I_d - V_d$ characteristics for (a) different gate lengths, $L$ (b) for $L = 4nm$ and for different $V_g$ values at room temperature (300°K)

Performance of Si NWMOSFET has also been simulated for different gate lengths of 4 and 2.2 nm. We have found that gate length of 4 nm is better in terms of off-current and $I_{on}/I_{off}$ ratio as clearly given in Figure 5 (a). In 2.2 nm Si NWMOSFET, tunneling leakage current ruins the device performance. 2.2 nm is found to be limiting gate length for our Si NWMOSFET in terms of device operation. Although the 4 nm Si NWMOSFETs are expected to show significant short channel effect, its high effective mass makes it inherently has lower direct tunneling compared to similar MOSFET made of GaN (Luisier & Klimeck, 2010; Zhu, 2017).

Figure 5 (b) also shows the gate voltage effect on saturation current. Here, gate voltage lowers the conduction band states towards Fermi energy $(E_f)$ as depicted in inset of Figure 5 (b) so that as $V_d$ increases more subband carriers can contribute to current, and $I_d$ rises. Saturation currents are higher at higher drain voltages compared to lower drain voltages. They have slightly different channel resistances because channel resistance is given as $R_{ch} = V_d/I_d$. When $V_d$ is sufficiently small, $I_d$ is nearly independent of $V_g$, and the channel conductance is constant as a characteristic behavior for 1D MOSFETs. Also, saturation drain voltage $(V_{d_{sat}})$ is independent of $V_g$ as shown in Figure 5 (b).

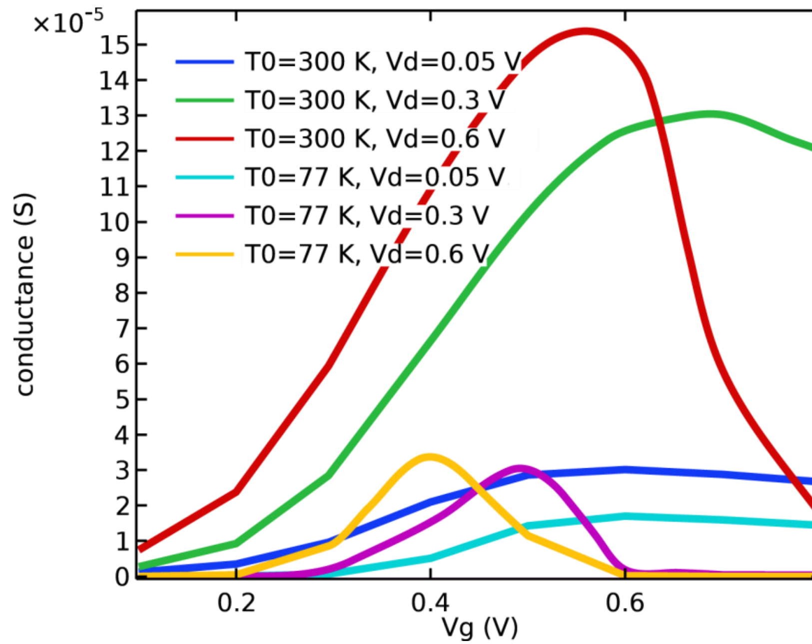


**Figure 6** Transconductance vs $V_g$ at room temperature and at liquid nitrogen temperature for varying $V_d$'s. The length of Si NWMOSFET is 4 nm and width is 3.2 nm

Conductance peaks indicate quantum confinement effect and are experimentally observed only at ultralow temperature and drain bias (Singh et al., 2006). However, observation of such oscillations in transconductance behavior can be possible to at room temperature only if the nanowire cross sectional area is sufficiently small compared to its length. The conductance peaks observed in our Si NWMOSFET smear out at lower temperatures due to intersubband scattering of carriers. Especially, at 77°K, with $V_d = 0.05$ V, the carrier scattering predominates the 1D transport features, thus, the conductance peak spreads. As temperature increases, intersubband scattering is mostly eliminated and 1D conductance peaks become more clear compared to lower temperatures, confirming ballistic 1D character of Si NWMOSFET. These conductance values are low compared to n-type InAs nanowire mosfet and Si NWMOSFET with gate lenght of 2 µm and due to subband scattering (Jönsson et al., 2021; Zhu, 2017).

## CONCLUSION

We have simulated Si NWMOSFET in terms of device parameters and temperature. We have found that quantum confinement induced effects are clearly seen in device transfer characteristics even at room temperature. This study would help to understand Si NWMOSFETs with a width of 3.2 nm and gate length of 4 nm in terms of strong confinement effects. Owing to quantum confinement of carriers in the channel, 1D ballistic transport features manifest themselves in device performance.

We have found that 2.2 nm gate length is a limiting case for this simulated device and intersubband scattering can dominate over phonon scattering, thus, the $I_d$ decreases for lower temperatures as low as liquid nitrogen temperature. Since quantum confinement is a key impact to tune and extend performance and scalability of next-generation MOSFETs, theoretical studies would pave the way for that purpose.

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### Conflict of Interest

The article authors declare that there is no conflict of interest between them.

## Author's Contributions

The authors declare that they have contributed equally to the article.

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