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DESIGN, MODELLING AND SIMULATION OF A FUEL CELL POWER CONDITIONING SYSTEM

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ABSTRACT

In this paper we present work carried out in order to stabilize the output voltage (V_O) of a 1 kW Horizon fuel cell (FC). The work involves the design, modeling and simulation of a power conditioning system (PCS). In the process to stabilize the voltage, it is required to also reduce the input current ripple and to improve the system response to load changes. We present here preliminary results that show that the system works, with the voltage smoothed, the input current ripple reduced and the response time increased.

This work also covers a comparative evaluation of the dynamic behavior of three converter topologies employed in power conditioning: boost converter, sepic converter and interleaved boost converter. The simulation results for the three topologies show that the output voltage of the fuel cell (FC) was stabilized. Furthermore, the results indicate that the interleaved boost converter is a better topology compared to the boost and sepic topologies in terms of our work.

INTRODUCTION

In order to stabilize the output of a FC, a controller is required. These controllers are usually custom designed according to the FC specifications. We present our design which is based on the 1 kW Horizon FC.

Various renewable sources have attracted interest as alternative energy sources to grid electricity. Among these FC technology is considered one of the better options due to its low carbon emissions, its modularity, its high efficiency and its non-intermittence [1]. In spite of the above advantages, fuel cells have disadvantages which include high cost and low round-trip efficiency [2]. As a power generator fuel cells have a problem in that they generate a low unstable output voltage which is of no use in many practical applications [3]. In addition to that, the output voltage is associated with a high current ripple that reduces the FC lifetime. Furthermore, fuel cells have a slow response to load changes.

In working towards the mentioned problems, MATLAB/Simulink (2013a student version) simulation software was used to study the dynamic response of the FC. Based on these simulations, three dc-dc converter topologies were studied to identify the most appropriate topology which would extend the life-time of the FC.

A FC is an electro-chemical device that converts reactants into electricity, heat and water by means of a chemical process [4]. Though each type of a FC is distinguished by its inherent properties, basically a FC consists of three components namely: a cathode, an anode and an electrolyte [5].

Figure 1 is the structure of a FC showing the direction of flow of the electrons and ions. The basic operation of a FC is described as follows: At the anode, hydrogen-rich fuel is fed into the FC chamber where the hydrogen molecules "disintegrate" into hydrogen ions and electrons through a chemical reaction that takes place at the anode surface.

The hydrogen ions flow to the cathode side of the FC via the electrolyte where they react with Oxygen ions to form water molecules. The electrons flow from the anode to the cathode through the load and conductor thereby complete the circuit and generate an electrical current.

In general, fuel cells are distinguished according to the chemical composition of the electrolyte, the fuel used and the characteristic of their operating temperature [7]. From the literature reviewed, there are presently six types of fuel cells. These are the Proton Exchange Membrane Fuel Cell (PEMFC), the Alkaline Fuel Cell (AFC), the Phosphoric Acid Fuel Cell

(PAFC), the Molten Carbonate Fuel Cell (MCFC), the Direct Methanol Fuel Cell (DMFC) and the Solid Oxide Fuel Cell (SOFC).

Since the output voltage of an individual FC is very low, a FC stack is formed by establishing a string of FCs connected in series or parallel to yield a considerably substantial amount of power. This however does not eliminate the variation of the FC stack output voltage associated with high current input ripple and slow response to load changes. To mitigate these problems, an appropriate Power Conditioner (PC) for the selected FC stack must be designed.

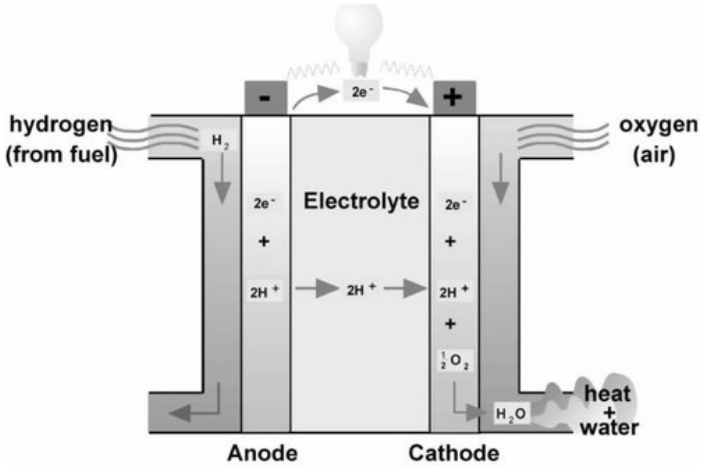

FIGURE 1: PEM FC STRUCTURE [6]

POWER CONDITIONING SYSTEM

Normally a FC Power Conditioning System consists of a FC stack and its auxiliaries which mostly include: a Fuel Processor, Water management, Air System, Thermal Management and a Power Conditioner (PC). In this paper, the focus will be on the design and simulation of the three different types of dc-dc converters with the aim of determining the most efficient topology for regulation of the FC stack output voltage.

In the design of a dc-dc converter, it is required that the FC stack is operated within its linear region. This region is bound by two non-linear regions on either ends of the linear curve as shown in Figure 2.

The polarization curve in Fig.2 gives a relation between the stack voltage and stack current density as a function of the load current [9], [10]. It indicates that the stack voltage decreases as the current density increases. A PC is therefore used to perform the necessary voltage regulation in order to eliminate the stack's low unstable output voltage, high input ripple and slow dynamic response [11] , [12].

Practically, a PC is realized with the dc-dc-ac concept. The dc-dc-ac concept is realised either as a single-stage topology or multi-stage topology [13]. The single stage topology only consists of the dc-ac inverter; in contrast, the multi-stage topology is made up of the dc-dc converter cascaded with the dc-ac inverter. The dc-dc converter produces a high stable dc voltage from the low unstable dc voltage of a FC stack. The dc-ac inverter produces an ac output voltage from the output voltage of the dc-dc converter.

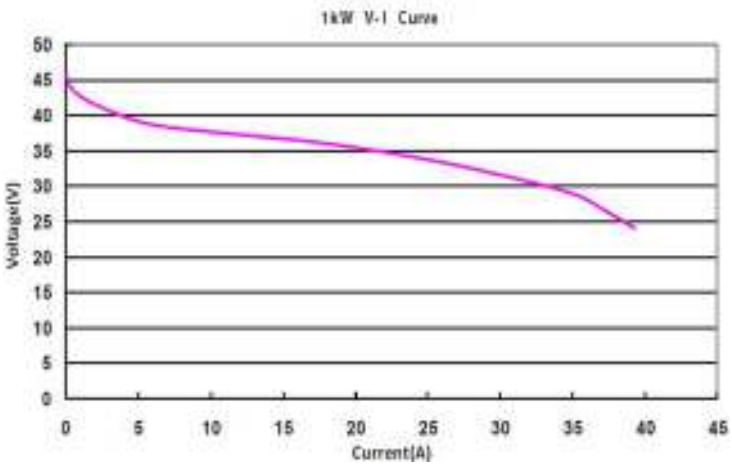

FIGURE 2: POLARISATION CURVE [8]

DESIGN, MODELLING AND SIMULATION OF CONVERTERS

There are several topologies of dc-dc converters to choose from in the design of a power conditioner [14]. In this work the topologies considered included boost converter, sepic converter and interleaved boost converter. An equivalent mathematical model of each converter was generated and simulated in MATLAB/Simulink. The converter designs were based on the 1 kW Horizon FC stack specifications. Simulation of the designs was carried out and the results were analysed and compared to determine the most appropriate converter topology. Table 1 gives information on the fuel cell specifications utilised for the design of the three converter topologies.

TABLE 1: PEM FC STACK TECHNICAL SPECIFICATION

Description	Parameter	unit
Number of cells	48	_
Rated power	1	kW
No load Voltage	45.6	V
Reactants	H_2 and O_2	_
H_2 gas purity	≥ 99.995	%
Max. Stack temp.	65	^oC
H_2 Pressure	0.45-0.55	bar
Flow rate @ max	13	L/min
Start-up time	≤ 30	s (@ ambient temp)
Stack efficiency	40	% (28.8 V@ 35 A)

MODELLING

The modelling carried out in this work is based on the work of [15], [16] and [17] . The following converter topologies are modelled:

1. BOOST CONVERTER

A boost converter operating in continuous conduction mode (CCM) with a switching period T and duty cycle D was considered under ideal conditions [18].

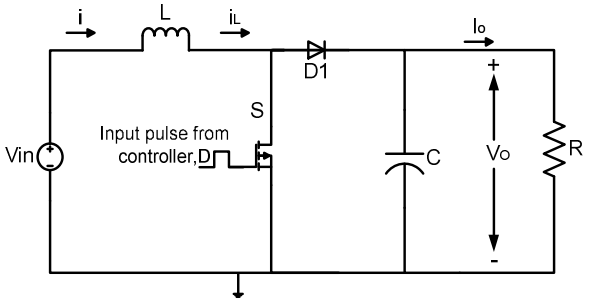

FIGURE 3: BOOST CONVERTER

An ideal boost converter circuit is shown in Fig.3 above. The converter consists of an inductor L, input voltage V_{in}, switch S, diode D1, capacitor C, load resistor R, input current i(t), inductor current iL(t), output current $i_O(t)$ and the duty cycle D. The minimum and maximum duty cycle, D_{min} and D_{max} for a lossless boost converter is given by the following equations:

$$D_{max} = 1 - \frac{V_{in\_min}}{V_o} \times \eta \qquad (1)$$

where, D_{max} is the maximum duty cycle required to keep the converter in CCM and to produce the desired output voltage for any given minimum input voltage, $V_{in\_min.}$

$$D_{min} = 1 - \frac{V_{in\_max}}{V_o} \times \eta \qquad (2)$$

where, D_{min} is the minimum duty cycle required to keep the converter in CCM and to produce the desired output voltage for any given maximum input voltage, $V_{in\_min.}$

1.1. The time interval $0 \leq t \leq DT$

During the time interval $0 \leq t \leq DT$ the boost converter circuit in Fig. 3 is represented by Fig.4. The figure shows the equivalent circuit of the converter when the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) switch is in the ON state. Here DT is the time when a switch is ON, so that $(1 - D)T$ is the time when a switch is OFF.

During this interval the inductor is charged and the output capacitor C provides power to the load, where V_o is the output voltage across C. D_1 is reversed biased and the voltage across its terminals is equal to -Vo. The dynamics of the converter for the state $0 \leq t \leq DT$ is given by the following set of differential equations:

$$\begin{cases} \frac{di_L(t)}{dt} = \frac{1}{L}(V_{in}(t)) \\ \frac{dv_o(t)}{dt} = \frac{1}{C}(-\frac{v_o(t)}{R}) \end{cases} \qquad (3)$$

where, $V_{in}(t)$ is the input voltage, $i_L(t)$ is the current through the inductor L and $v_o(t)$ is the voltage across the capacitor C. The input current i(t) is equivalent to $i_L(t)$.

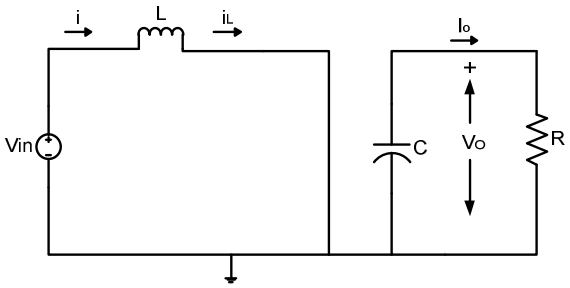

FIGURE 4: CONVERTER CIRCUIT WHEN S IS ON

1.2. The time interval $DT \leq t \leq T$

During the time interval $DT \leq t \leq T$, the boost converter circuit in Figure 3 is represented by Figure 5. The diagram below shows the equivalent circuit of the converter when the MOSFET is in the OFF state.

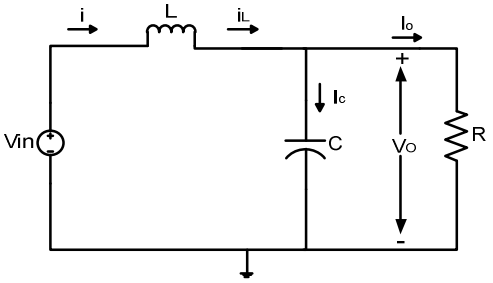

FIGURE 5: CONVERTER CIRCUIT WHEN S IS OFF

During this interval the inductor L discharges current to the output capacitor C. The dynamics of the converter for the state $0 \leq t \leq DT$ is given by the following set of differential equations:

$$\begin{cases} \frac{di_L(t)}{dt} = \frac{1}{L}(V_{in}(t) - V_o(t)) \\ \frac{dv_o(t)}{dt} = \frac{1}{C}(i_L(t) - \frac{v_o(t)}{R}) \end{cases} \qquad (4)$$

where $V_{in}(t)$ is the input voltage, $i_L(t)$ is the current through the inductor L, $i_C(t)$ is the current through the capacitor and $v_o(t)$ is the voltage across the capacitor C.

2. INTERLEAVED-BOOST CONVERTER

An interleaved boost converter operating in continuous conduction mode (CCM) with a switching period T and duty

cycle D was considered under ideal condition. The interleaved converter is shown in Fig.6. The converter consists of two input inductors $L_1 = L_2$, one output capacitor C, two MOSFET switches S_1 and S_2, and two diodes D_1 and D_2. By using the input current ripple cancellation property, the current ripple is nearly reduced to zero for a duty cycle of 0.5. The interleaved boost converter consists of two traditional boost converters interleaved together; as a result its steady state equations are similar to the steady state equations of the traditional boost converter.

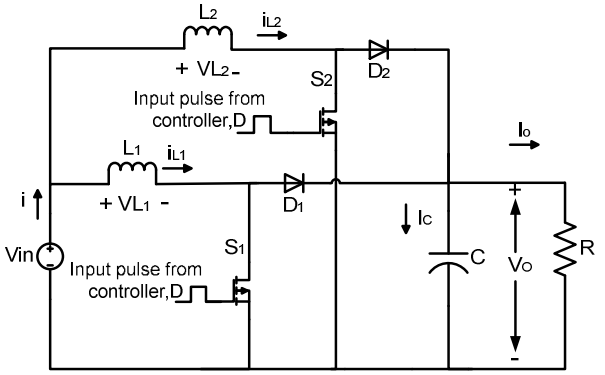

FIGURE 6: INTERLEAVED BOOST CONVERTER

When the converter is analysed under steady state operation in CCM, the voltage across all the inductors and the current through the output capacitor over one switching cycle is equal to zero. The switches are operated at 180 ^{o} out phase such that when L_1 is charging L_2 is simultaneously discharging and vice versa.

The minimum and maximum duty cycle, D_{min} and D_{max} for a lossless interleaved boost is determined by using equation (1) and equation (2).

2.1. The time interval $0 \leq t \leq DT$

During the time interval $0 \leq t \leq DT$, the interleaved boost converter circuit in Fig.7 is represented by Fig.7. The figure shows the equivalent circuit of the converter for the MOSFETs state S_1 is ON and S_2 is OFF. Here DT is the time when a switch is ON, so that $(1 - D)T$ is the time when a switch is OFF.

During this time interval, L_1 is charging and L_2 discharging current to C. The dynamics of the converter for the state $0 \leq t \leq DT$ is given by the following set of differential equations:

$$\begin{cases} \dfrac{di_{L1}(t)}{dt} = \dfrac{V_{in}(t)}{L_1} \\ \dfrac{di_{L2}(t)}{dt} = \dfrac{V_{in}(t) - V_O(t)}{L_2} \\ \dfrac{dV_C(t)}{dt} = \dfrac{-V_O(t)}{CR} \end{cases} \quad (5)$$

where $V_{in}(t)$ is the input source voltage, $iL_1(t)$ and $iL_2(t)$ is the current passing through the inductor L_1 and L_2 respectively, $V_O(t)$ is the output voltage and $V_C(t)$ is the voltage across the capacitor. The input current is a sum of the average current through L_1 and L_2 and is therefore given as:

$$i(t) = i_{L1}(t) + i_{L2}(t) \quad (6)$$

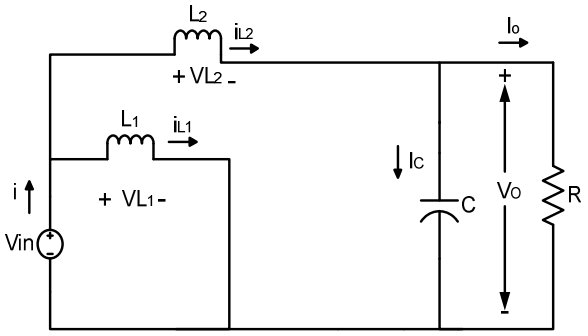

Figure 7: Converter circuit when S1 is ON & S2 is OFF

2.2. The time interval $DT \leq t \leq T$

During the time interval $DT \leq t \leq T$, the interleaved boost converter circuit is by given Figure 8. The diagram in Fig.8 shows the equivalent circuit of the converter for the MOSFETs state S_2 is ON and S_1 is OFF.

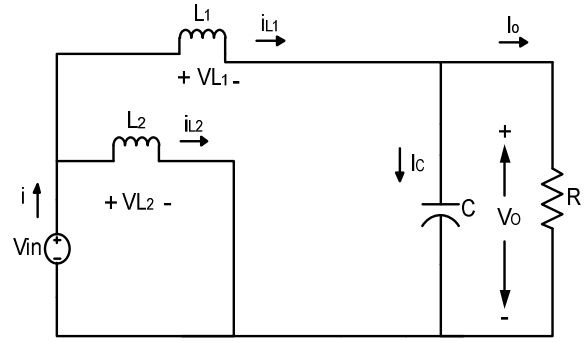

Figure 8: Converter circuit when S2 is ON and S1 is OFF

During this time interval, L_2 is charging and L_1 discharges current to C. The description of the converter dynamics for the state $DT \leq t \leq T$ is given by the following differential equations:

$$\begin{cases} \dfrac{di_{L2}(t)}{dt} = \dfrac{V_{in}(t)}{L_2} \\ \dfrac{di_{L1}(t)}{dt} = \dfrac{V_{in}(t) - V_O(t)}{L_1} \\ \dfrac{dV_C(t)}{dt} = \dfrac{-V_O(t)}{CR} \end{cases} \quad (7)$$

3. Sepic Converter

Lastly, a sepic converter was evaluated for CCM of operation assuming ideal component conditions with a switching period T and duty cycle D [19].

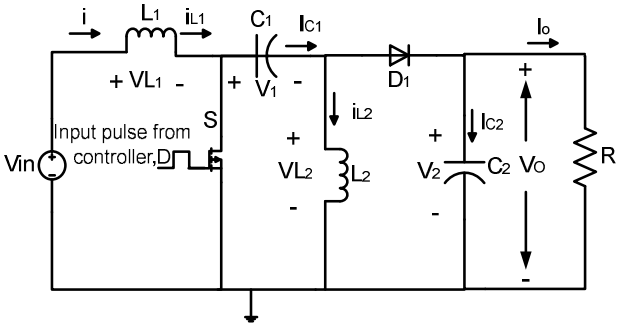

FIGURE 9: SEPIC CONVERTER

The Sepic converter circuit is given by Fig. 9,where V_{in} is input voltage, L_1 and L_2 are inductors, C_1 and C_2 are capacitors, D_1 is a diode, D is the duty cycle, R is the output resistor, i(t) is the input current, iL1(t) and iL2(t) are the inductors currents, I_{C1} and I_{C2} are the capacitors currents, V_1 is voltage across the capacitor C_1 and the voltage across C_2 is equivalent to V_O. The minimum and maximum duty cycle, D_{min} and D_{max} required for the converter to operate in CCM and to produced the desired output voltage is given by the following equations:

$$D_{min} = \frac{V_O}{V_{in\_max} + V_O} \times \eta \tag{8}$$

$$D_{max} = \frac{V_O}{V_{in\_min} + V_O} \times \eta \tag{9}$$

3.1. The time interval $0 \leq t \leq DT$

During the interval $0 \leq t \leq DT$ the sepic converter circuit in Fig.9 is given by Fig.10. The figure shows the equivalent circuit of the converter when S in ON.

During this interval, both L_1 and L_2 are charging, C_1 discharges through L_2 and C_2 provides power to the load. The dynamics of the converter for the state $0 \leq t \leq DT$ is given by the following set of differential equations:

$$\begin{cases} \frac{di_{L1}(t)}{dt} = \frac{1}{L_1}(V_{in}(t)) \\ \frac{dv_1(t)}{dt} = \frac{1}{C_1}(-i_{L2}(t)) \\ \frac{di_{L2}(t)}{dt} = \frac{1}{L_2}(V_1(t)) \\ \frac{dv_2(t)}{dt} = \frac{1}{C_2}(-\frac{v_O(t)}{R}) \end{cases} \tag{10}$$

where $i_{L1}(t)$ is the current through L_1 and $i_{L2}(t)$ is the current through L_2, V_1 is the voltage across C_1 and V_2 is the voltage across C_2.

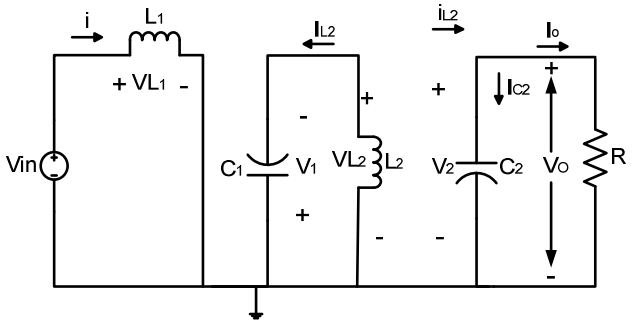

FIGURE 10: SEPIC CONVERTER WHEN SWITCH S IS ON

3.2. The time interval $DT \leq t \leq T$

During this time interval, the sepic converter circuit in Fig.9 is given by Fig.11. The diagram below shows the equivalent circuit of the converter when the MOSFET state is OFF.

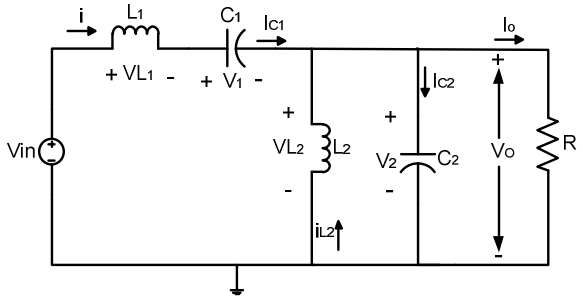

FIGURE 11: CONVERTER WHEN SWITCH S IS OFF

During this time interval the dynamics of the converter is given by the following set of differential equations

$$\begin{cases} \frac{di_{L1}(t)}{dt} = \frac{1}{L_1}(V_{in}(t) - V_1(t) - V_2(t)) \\ \frac{dv_1(t)}{dt} = \frac{1}{C_1}(i(t)) \\ \frac{di_{L2}(t)}{dt} = \frac{1}{L_2}(V_2(t)) \\ \frac{dv_2(t)}{dt} = \frac{1}{C_2}(i_{L1}(t) + i_{L2}(t) - \frac{v_2(t)}{R}) \end{cases} \tag{11}$$

DESIGN AND SIMULATION RESULTS

1.1. Design

A design summary of the converters is given in Table 2, Table 3 and Table 4. The simulation results are shown from Fig.12 to 14 and Table 5.

TABLE 2: DESIGN SUMMARY OF BOOST CONVERTER

Boost converter		
Parameter	Value	Unit
P_{in}	1	kW
Efficiency, η	90	%
$V_{fc\ min}$	28.8	V
$V_{fc\ max}$	45.6	V
V_O	100	V
ΔiL	0.2*i(t)	A
ΔV_o	0.01*V_O	V
Inductor, L	72.2	µH
Capacitor, C	135	µF
Resistor, R_{min}	11.11	Ω
Resistor, R_{max}	222.2	Ω
Duty Cycle, D_{min}	0.6	_
Duty Cycle, D_{max}	0.74	_

TABLE 3: DESIGN SUMMARY OF IBOOST CONVERTER

Interleaved boost converter		
Parameter	Value	Unit
Input power, P_{in}	1	kW
Efficiency, η	90	%
$V_{fc\ min}$	28.8	V
$V_{fc\ max}$	45.6	V
V_O	100	V
ΔiL	0.2*i(t)	A
ΔV_o	0.01*V_O	V
Inductor, L_1=L_2	72.2	µH
Capacitor, C	135	µF
Resistor, R_{min}	11.11	Ω
Resistor, R_{max}	222.2	Ω
Duty Cycle, D_{min}	0.6	_
Duty Cycle, D_{max}	0.74	_

TABLE 4: DESIGN SUMMARY OF SEPIC CONVERTER

Sepic converter		
Parameter	Value	Unit
Input power, P_{in}	1	kW
Efficiency, η	90	%
$V_{fc\ min}$	28.8	V
$V_{fc\ max}$	45.6	V
V_O	100	V
ΔiL	0.2*i(t)	A
ΔV_o	0.01*V_O	V
Inductor, L_1=L_1	71.9	µH
Capacitor, C_1,C_2	280.1,280.1	µF
Resistor, R_{min}	11.11	Ω
Resistor, R_{max}	222.2	Ω
Duty Cycle, D_{min}	0.67	_
Duty Cycle, D_{max}	0.78	_

The MATLAB/Simulink open-loop simulation setup for stabilizing of the fuel cell output voltage as well as the comparative study of the dynamic behaviour of the fuel cell output voltage under different converter topologies is shown in Fig 12, Fig 13 and Fig 14, respectively.

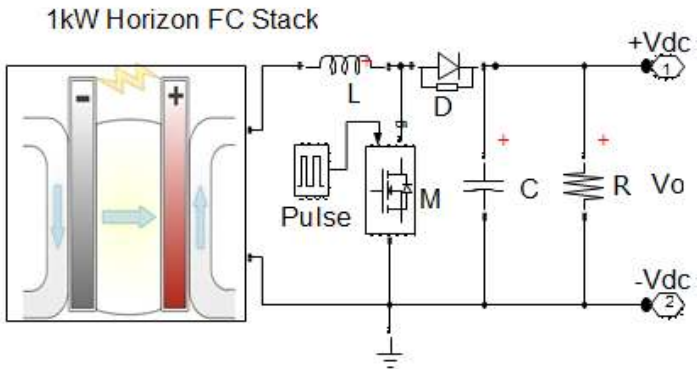

FIGURE 12: BOOST CONVERTER FC PC

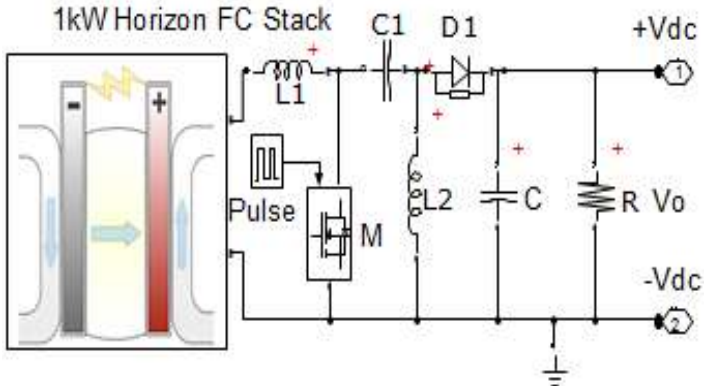

FIGURE 13: SEPIC CONVERTER FC PC

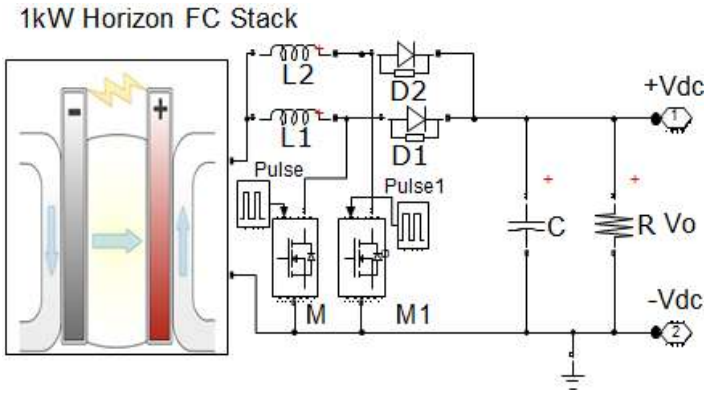

FIGURE 14: INTERLEAVED BOOST CONVERTER FC PC

As shown in figures 12, 13 and 14, a 1 kW Horizon fuel cell is used as a power generator for the dc-dc converter topologies. For each topology, the converter is designed to operate at efficiency of 90 % with an output voltage of 100 V. Later, a battery bank was introduced into the system as an external storage device (ESD) in order to improve the system response to load changes. Given the power rating of the fuel cell as 1 kW, with a requirement that the converters operate at 90 % efficiency

at an output voltage of 100 V, the theoretical output power and the load resistor value of the converters is calculated as follows:

$$Pout = \eta \times Pin = 0.9 \times 1\ kW = 900\ W \qquad (12)$$

where P_{in} is the input power and P_{out} is the output power of the converter. The converter load resistor, R_{min} which is required to achieve maximum power at an efficiency of 90 %, is therefore calculated as:

$$V_O = \frac{Pout}{I_O}, I_O = \frac{900\ W}{100\ V} = 9\ \text{A} \qquad (13)$$

$$\mathrm{R_{min}} = \frac{V_O}{I_O} = \frac{100\ V}{9\ A} = 11.11\ \Omega \qquad (14)$$

A Simulink model for each converter topology is implemented and simulated to validate the design.

1.1.1.Simulation results

Fig.15, Fig.16 and Fig.17 presents simulation results of the open-loop performance of the fuel cell power conditioning system for the three converter topologies without an external ESD. The figure shows a Simulink scope displaying the fuel cell output voltage measured under the simulation of each converter topology. Where the y-axis on each graph represents the magnitude of the measured signal, and the x-axis represents the time in seconds over which the signals were measured.

The time taken for the output voltage of each converter topology to reach a steady state is indicated in the figures. The figures also show the time taken to reach a steady state for the following signals: fuel cell output voltage ripple and fuel cell input current ripple, converters output voltage ripple. A comparison of the results shows that the boost converter topology takes the shortest time to reach a steady state while the sepic converter takes the longest time. In terms of efficiency, neglecting power losses the boost and interleaved boost topologies show a better performance compared to the sepic converter.

In the figures, i_{fc} denotes the fuel cell input current ripple signal and V_{fc} denotes the fuel cell output voltage ripple signal and V_O denotes the output voltage signal of a converter topology. In order to clearly identify the waveforms of each topology, the waveform signal labels in figures 15 to 20 are expressed with an underscore followed by the name of each particular converter topology.

Fig.18, Fig.19 and Fig. 20 presents simulation results of the open-loop performance of the fuel cell power conditioning system for the three converter topologies where a battery bank is used as an external energy storage device (ESD). The measured system signals are displayed by the Simulink scope as shown in the figures. Where the y-axis on each graph represents the magnitude of the measured signal, and the x-axis represents the time in seconds over which the signals are measured.

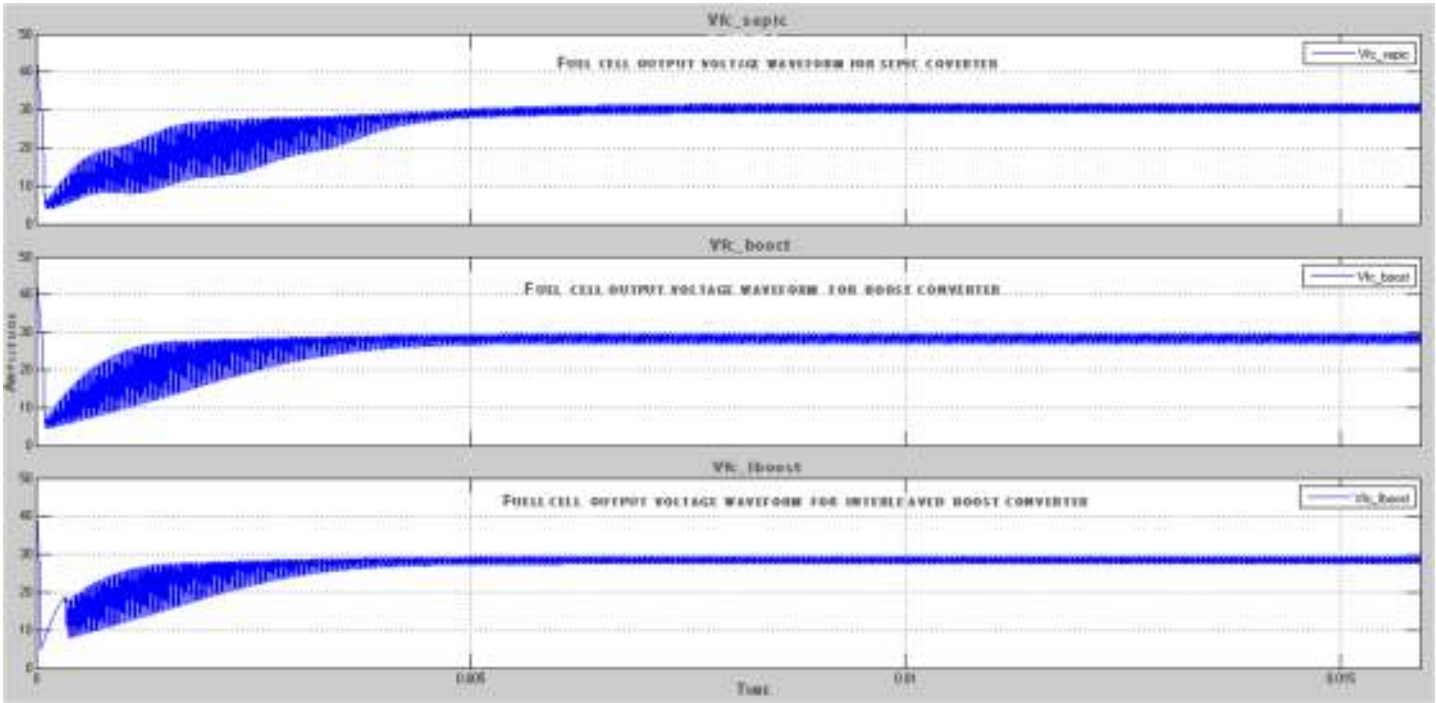

FIGURE 15: FUEL CELL OUTPUT VOLTAGE WITHOUT ESD FOR DIFFERENT CONVERTER TOPOLOGIES

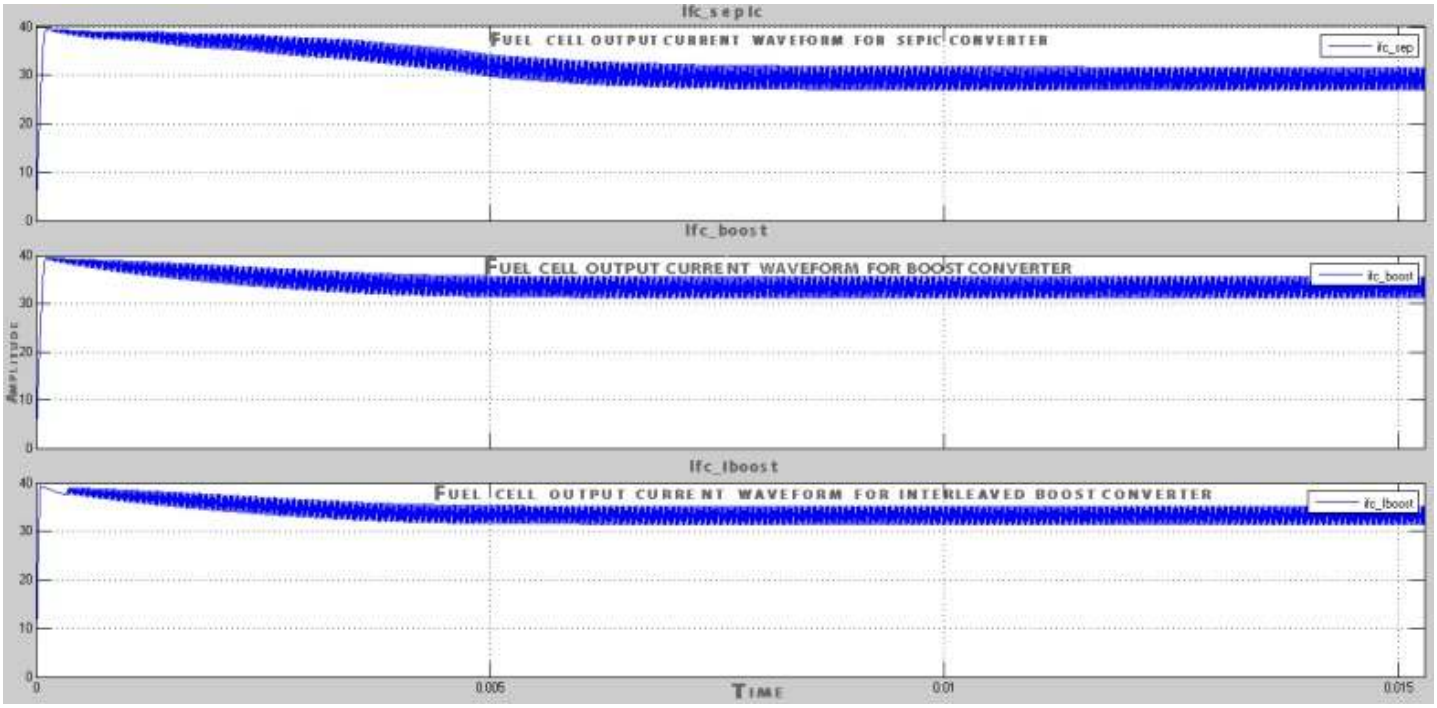

FIGURE 16: FUEL CELL OUTPUT CURRENT WITH ESD FOR DIFFERENT CONVERTER TOPOLOGIES

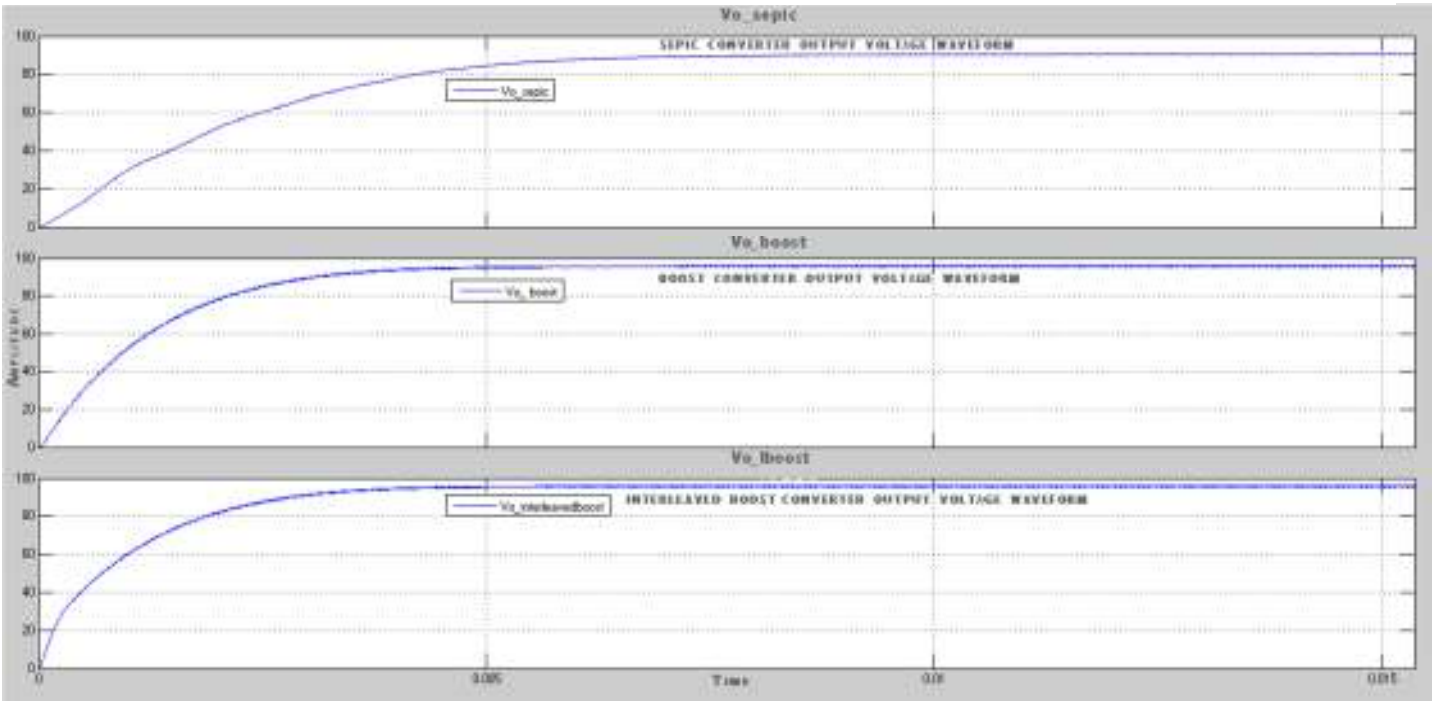

FIGURE 17: CONVERTERS OUTPUT VOLTAGE WITHOUT AN ESD

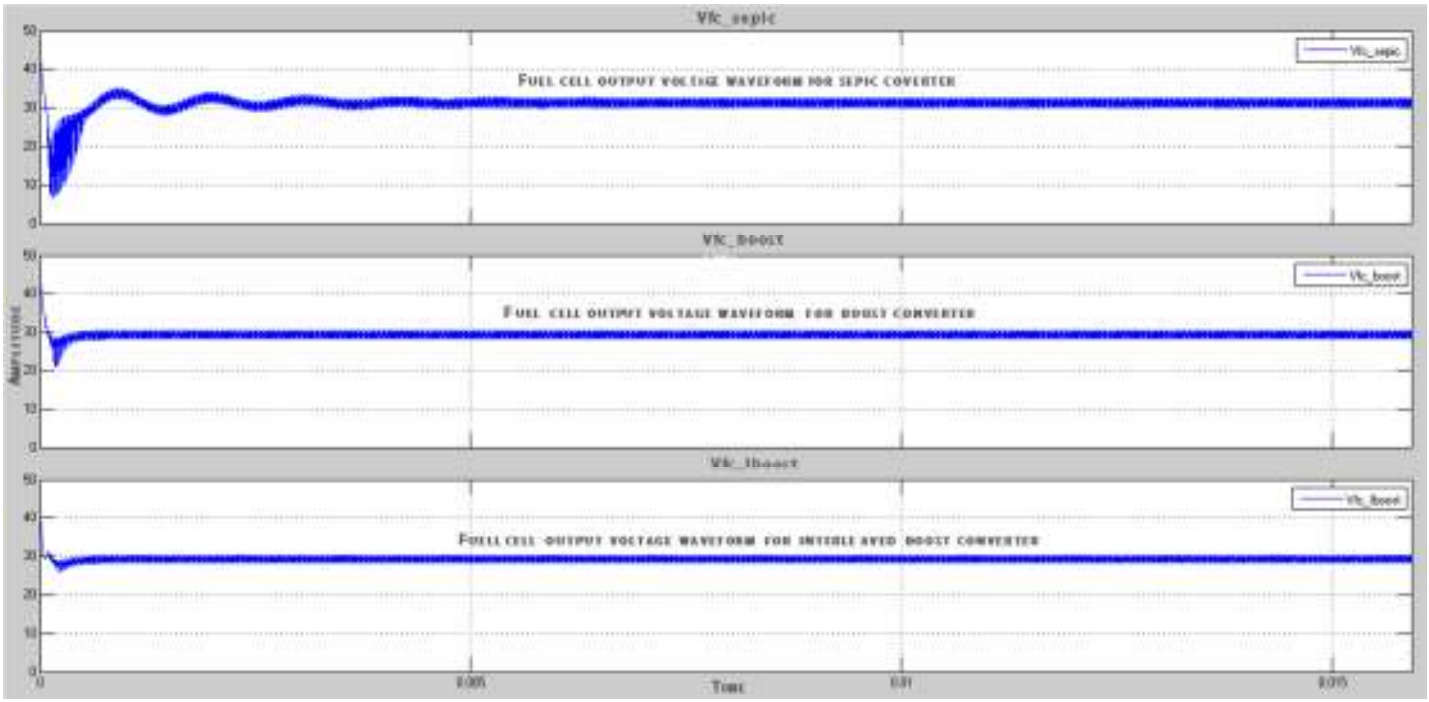

FIGURE 18: FUEL CELL OUTPUT VOLTAGE WITH ESD FOR DIFFERENT CONVERTER TOPOLOGIES

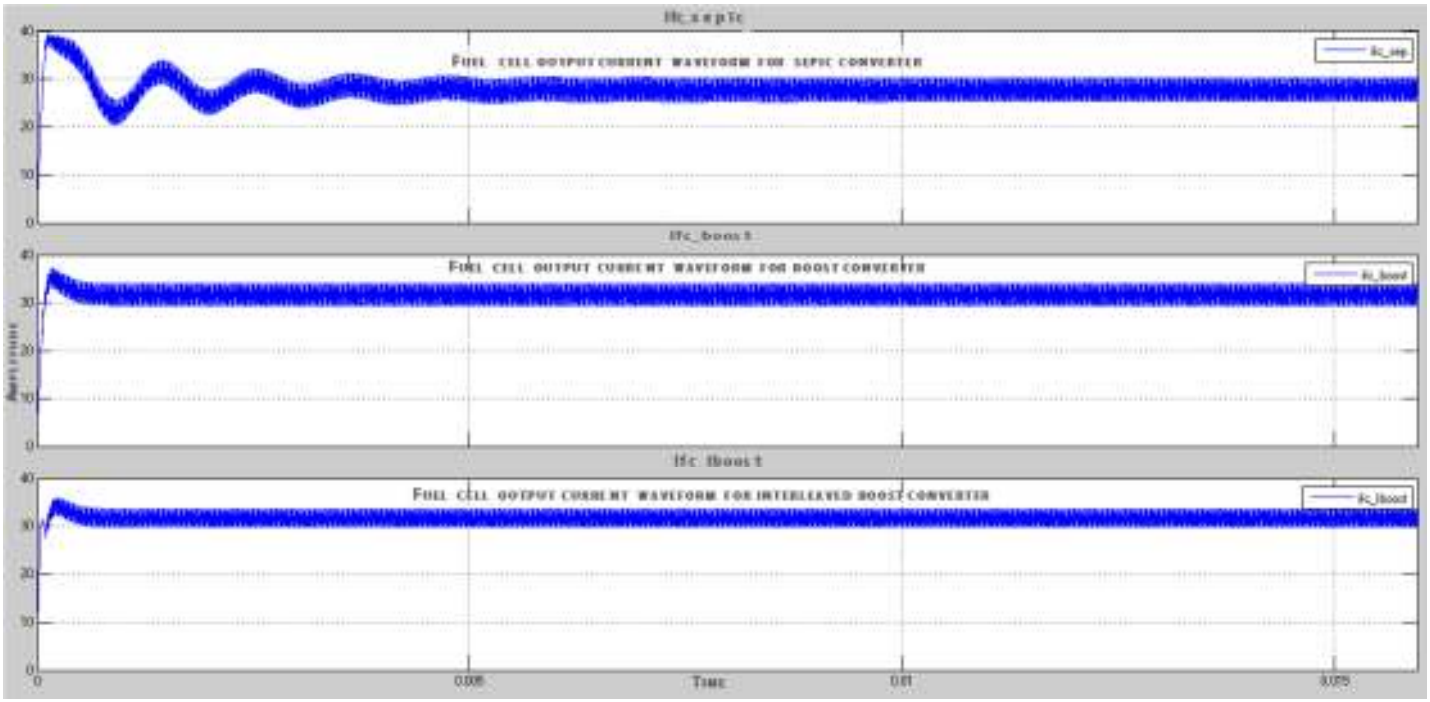

FIGURE 19: FUEL CELL OUTPUT CURRENT WITH ESD FOR DIFFERENT CONVERTER TOPOLOGIES

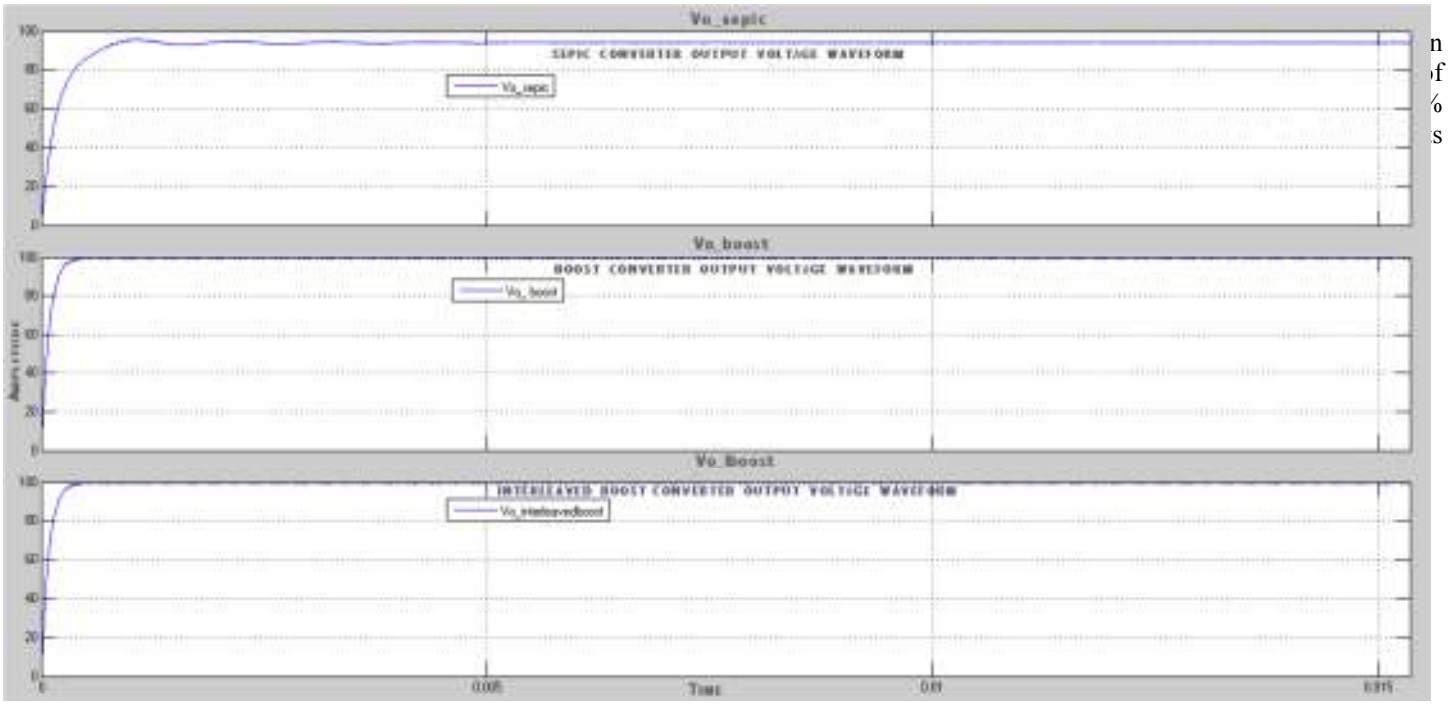

FIGURE 20: CONVERTERS OUTPUT VOLTAGE WITH ESD

The results from Fig.18 to Fig.20 show improvement in the system's dynamic response to load changes as well as a reduction in the magnitude of the FC output voltage ripple and FC input current ripple. It can therefore be concluded that ESD use improves system response time to load changes, reduces both voltage ripple and current ripple in the system. The simulation results are shown in figures 15 to 20 respectively.

A summary of the results for open-loop simulation of the converters in MATLAB/Simulink software is given in Table 5 and Table 6. The table displays various parameters extracted from the converters' performance for two scenarios: with an ESD and without an ESD.

TABLE 5: SIMULATION SUMMARY WITHOUT ESD

PAR	Converter Topologies without ESD					
	Boost converter		Interleaved boost converter		Sepic converter	
	Value	Unit	Value	Unit	Value	Unit
ΔV_{fc}	2.33	V	2	V	2.56	V
ΔI_{fc}	4.37	A	3.76	A	4.96	A
ΔV_O	0.95	V	0.93	V	0.45	V
V_{fc}	29.33	V	28.66	V	31.89	V
I_{fc}	31.66	A	32.96	A	26.68	A
V_O	96.09	V	96.22	V	90.36	V
I_O	8.649	A	8.66	A	8.13	A
P_{in}	928.59	W	944.63	W	850.83	W
P_{out}	831.03	W	833.27	W	734.90	W
η	89.49	%	88.21	%	86.37	%
T_S	0.0025	s	0.0026	s	0.0045	s

TABLE 6: SIMULATION SUMMARY WITH ESD

PAR	Converter Topologies with ESD					
	Boost converter		Interleaved boost converter		Sepic converter	
	Value	Unit	Value	Unit	Value	Unit
ΔV_{fc}	2.34	V	2.02	V	3.01	V
ΔI_{fc}	4.54	A	3.91	A	5.26	A
ΔV_O	0.89	V	0.88	V	0.63	V
V_{fc}	30.23	V	29.52	V	32.24	V
I_{fc}	29.91	A	31.28	A	25.97	A
V_O	100.1	V	100.1	V	94.22	V
I_O	9.01	A	9.01	A	8.48	A
P_{in}	904.18	W	923.39	W	837.27	W
P_{out}	902.10	W	902.01	W	798.99	W
η	99.7	%	97.7	%	94.35	%
T_S	0.0004	s	0.0004	s	0.003	s

Table 6 presents performance of the converters when an ESD is incorporated into the system. Some of the effects of adding an ESD into the system include: improved system efficiency, improved response time to load transients and reduced voltage ripple and current ripple.

In both Table 5 and Table 6, the efficiency of each Simulink converter model for both with ESD and without ESD scenario was determined by the following equation:

$$\eta = \frac{Pout}{Pin} = \frac{V_o \times I_O}{V_{fc} \times I_{fc}} \quad (14)$$

CONCLUSION

The simulation results for all topologies show that the fuel cell output voltage was stabilised. Furthermore, the results indicate that the interleaved boost converter is a better topology compared to the boost and sepic topologies in terms of conditioning a fuel cell output voltage and maintaining a low voltage ripple and current ripple and at the sometime ensuring high efficiency.

The future work will focus on the design, modelling, simulation and actual development of a fuel cell power conditioning system. The modelling will therefore be more detailed where the power losses and parasitic elements of the components will be taken into consideration. A detailed fuel cell stack model will also be considered, where the air and fuel flow rates into the fuel cell stack are subjected to variations corresponding to a changing demand of current by the load.

NOMENCLATURE

CCM	Continuous conduction mode
dc-dc	Direct current to direct current
dc-dc-ac	Direct current to direct current to alternating
ESD	Energy storage device
FC	Fuel cell
MOSFET	Metal-oxide-semiconductor field-effect transistor
PC	Power conditioner
PCS	Power conditioning system

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