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Quasi-Resonant Half-Wave Buck Converter with Non-Isolated High-Side Switching Techniques

Burak GÖRDÜK*[1], Elif TOPUZ[1], Deniz YILDIRIM[1]

Abstract

Power density of the power converters became one of the most important parameters in many applications. Power density is increased by reducing the losses through use of better performing components and circuit topologies. It can be increased further by reducing the size of filter components through increasing the switching frequency. In hard-switching converters however, losses due to switching will eventually render this method not applicable. Instead, resonant converters are utilized in many high-frequency switched power supplies. Soft-switching feature of these converters provide increased efficiency due to decreased switching losses. Such converters exploit the resonance of the specific inductors and capacitors in the circuit called as resonant tank elements. Resonance behavior is used in order to eliminate turn-on or turn-off losses. Existing power converter topologies can be modified to create the resonance during switching period. Such converters are called as quasi-resonant converters. This paper presents analysis and design of Zero Current Switching (ZCS) half-wave quasi-resonant buck converters. In this topology, high-side switching is required. Two different non-isolated high-side switching techniques are utilized. Experimental results are obtained for light load to full load operation. Both techniques are compared in detail.

Keywords: Half-wave Buck Converter, high-side switching, quasi-resonant converters, Zero-Current Switching.

1. INTRODUCTION

The working principle of the conventional pulse width modulated (PWM) converters are based on transferring the energy using capacitors and inductors with the help of semiconductor elements. These semiconductor elements are operated as switches either in fully on or off mode connecting energy transfer elements to source and load. Output voltage can be adjusted by the duty cycle of control signal. Unlike linear power supplies, switched-mode converters tend to generate ripple at their output due to switching action. This ripple can be reduced by increasing the switching frequency or increasing the size of filter elements. The latter is least demanded because of the increased cost and size of the converter [1].

The MOSFETs are semiconductor switching elements that are used in low to mid-range power

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supplies. They are suitable for high frequency operation up to couple of MHz depending on the ratings. However, increased switching frequency means increased switching losses due to the hard-switching behavior of the PWM converters. To overcome this issue, switched-mode power conversion technologies are transformed from simple PWM converters to resonant converters [2]. Beside low switching losses compared to PWM converters, they can eliminate electromagnetic interference (EMI) problems because of sinusoidal variations; they do not have sharp rising voltage/current waveforms [3]. The resonant converters were found out in early 1980s [4].

Many different configurations of resonant converters are available and quasi resonant converters are one of them. Quasi-resonant converters are derived from the conventional PWM converters, where, resonant tank elements are added to the circuit. Since quasi-resonant converters include LC tank circuit, it is possible to obtain zero current (ZCS) or zero voltage switching (ZVS) in semiconductor elements. While ZCS is used for eliminating turn-off losses of the switching element, ZVS is used for turn-on switching losses [5].

ZCS Quasi resonant converters are used in bidirectional battery equalizers to minimize switching loss. It is seen that efficiency is higher than around 20%~30% unlike conventional battery equalizers [6]. Quasi resonant converters can be half-wave or full-wave configuration. Analysis of the ZCS quasi-resonant converters is studied in [7, 8]. In ZCS quasi-resonant buck converter, high side switching is necessary because of buck converter topology. There are couples of techniques for high side switching [9]. For example, using of a P-channel switch or isolated gate drive circuitry.

On the other hand, ZVS quasi-resonant buck converter is also studied in [10, 11]. In [11], a 3 kW quasi-resonant buck converter is developed and maximum 98.7% efficiency is obtained using ZVS. Also, steady state analysis of ZVS quasi-resonant converter is studied in [12].

In this study, ZCS quasi-resonant (half-wave) buck converter is investigated, analyzed and experimentally verified. Two circuit boards are produced with different approaches on non-isolated high-side switching. Based on the experimental results, performances of these circuits are investigated.

2. HALF WAVE QUASI RESONANT ZCS BUCK CONVERTERS

The half-wave ZCS buck converter depicted in Fig. 1 is a type of quasi-resonant converter in which an LC resonant tank is added to switch element. L_r and C_r are resonant elements and the series diode D_1 prevents inductor current becoming negative. Since output filters L_f and C_f are large in value the output part can be represented by a current source with a value equals to load current as given in Fig. 2.

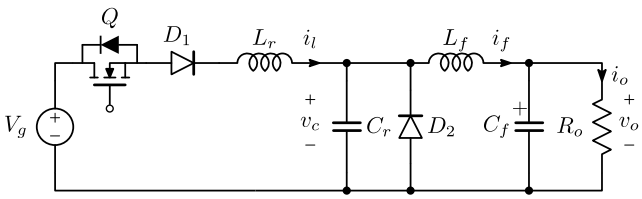


Figure 1 Half-wave ZCS buck converter

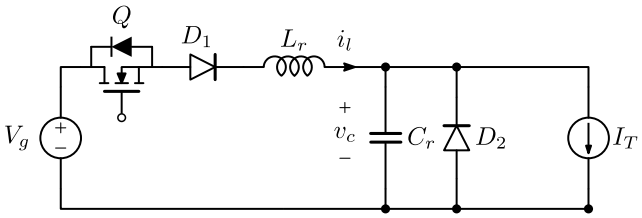


Figure 2 Half-wave ZCS buck converter with constant current source

2.1. Steady State Analysis of The Half Wave ZCS Buck Converter

In order to get an understanding of the relationship between input and output voltage with certain operating conditions of the circuit, the steady state analysis must be done. This analysis is done by normalizing voltage and inductor current equations. For the normalization approach, notations used are given in equations 1 to 8.

$$V_T = V_g \quad (1)$$

$$V_{base} = V_T \quad (2)$$

$$I_{base} = \frac{V_T}{R_0} \quad (3)$$

$$R_0 = \sqrt{\frac{L_r}{C_r}} \quad (4)$$

$$j_L = \frac{i_L}{I_{base}} \quad (5)$$

$$J_T = \frac{I_T}{I_{base}} \quad (6)$$

$$m_c = \frac{v_c}{V_{base}} \quad (7)$$

$$F = \frac{f_s}{f_o} \quad (8)$$

Where, f_s is the switching frequency, f_o is the resonant frequency, and F is normalized frequency, R_0 is effective load resistance, m_c, j_L, and J_T are the normalized capacitor voltage, inductor current, and load current respectively.

The first interval of the operation starts by turning on the switch Q. Before this interval, load current I_T is flowing through diode D_2. In this interval, series diode D_1 and freewheeling diode D_2 are also conducting. Equivalent circuit is given in Fig. 3.

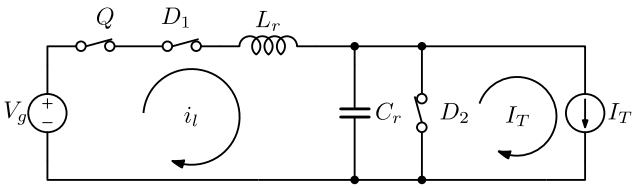


Figure 3 Equivalent circuit of interval I

Current flowing through the resonant inductor rises linearly from zero to steady state output current value. Interval I ends when inductor current reaches to steady state output current value. Therefore, interval I is called as inductor charging mode [5]. The normalized state equation is given in equation (9).

$$\frac{1}{\omega_0}\frac{dj_L}{dt} = 1 \quad (9)$$

With the initial condition of shown in equation (10).

$$j_L(0) = 0 \quad (10)$$

The interval has a length of angle α. When iL equals to IT, D2 turns off and interval ends. By solving the initial condition problem, final values are obtained in equations (11) to (13).

$$j_L(\omega_0 t) = \omega_0 t \quad (11)$$

$$m_c(\omega_0 t) = 0 \quad (12)$$

$$\alpha = J_T \quad (13)$$

Second interval is the ringing interval of the resonant tank. Equivalent circuit belongs to the second interval is given in Fig. 4. State equations are given in equations (14) and (15).

$$\frac{1}{\omega_0}\frac{dj_L}{dt} = 1 - m_c \quad (14)$$

$$\frac{1}{\omega_0}\frac{dm_c}{dt} = j_L - J_T \quad (15)$$

These equations belong to a circle with the center (1, J_T) in the state plane trajectory. This circle has the initial point of (0, J_T) and the final point of (Mc_1, 0). This interval lasts for the angle β and ends when inductor current goes to zero and hence series diode D_1 turns off.

The switch is turned off at third interval because of the inductor current being zero. In this interval series diode D_1 and freewheeling diode D_2 are also off, output current I_T discharges the tank capacitor linearly. Corresponding equivalent circuit is given in Fig. 5.

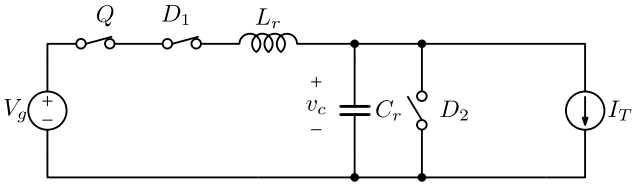


Figure 4 Equivalent circuit of interval II

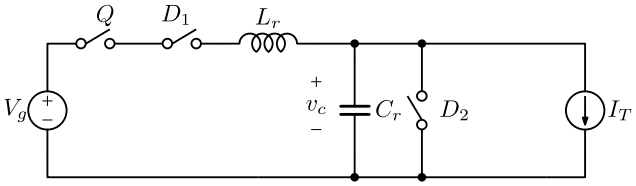


Figure 5 Equivalent circuit of interval III

Normalized state equation and initial conditions are given in equations (16) to (18).

$$\frac{1}{\omega_0}\frac{dm_c}{dt} = -J_T \tag{16}$$

$$m_c(\alpha+\beta) = M_{c1} \tag{17}$$

$$m_c(\omega_0 t) = M_{C1} - J_T(\omega_0 t - a - \beta) \tag{18}$$

Third interval lasts for an angle δ and ends when the resonant tank capacitor voltage goes to zero, and Interval IV begins as freewheeling diode D_2 turns on and output current flows through on it. Equivalent circuit is given in Fig. 6.

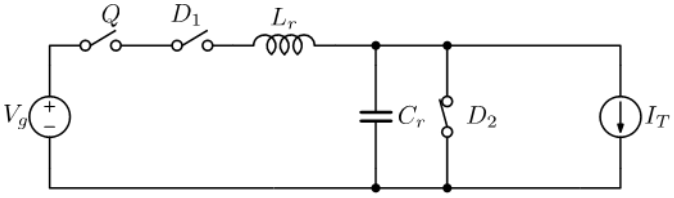


Figure 6 Equivalent circuit of interval IV

Both the capacitor voltage and the inductor current are zero. This interval lasts for the angle ξ and ends when switch Q is turned on again at the start of the first interval. For the whole switching period T_S waveforms of gate signals, resonant capacitor voltage and resonant inductor current along with the interval numbers and angles are given in Fig 7.

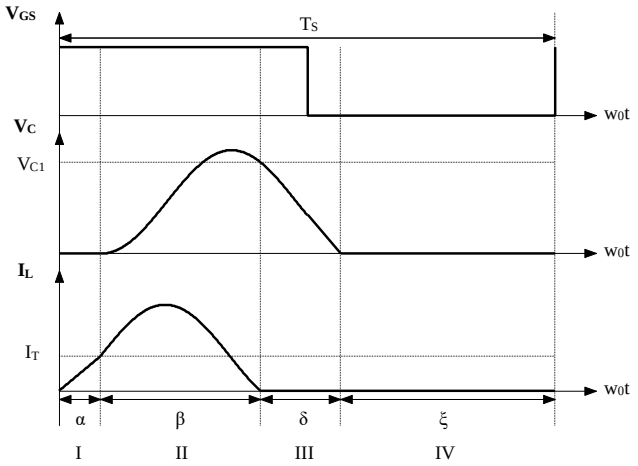


Figure 7 Waveforms for the half-wave ZCS quasi resonant buck converter

The state plane trajectory for these four intervals is given in Fig. 8.

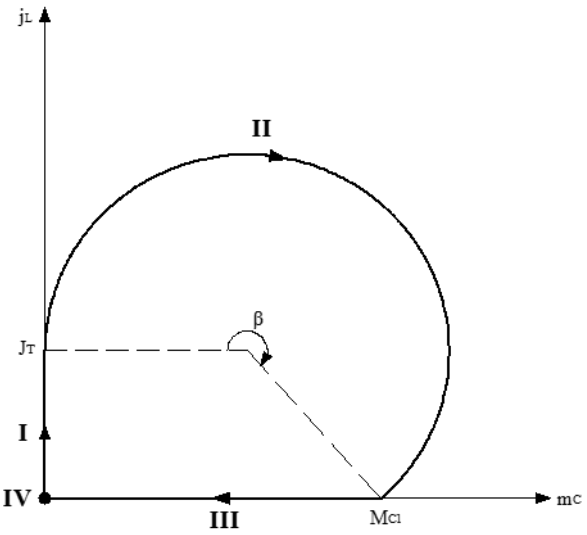


Figure 8 State plane trajectory of the converter

The conduction angles α, β, δ and ξ compose the switching period. Using state plane trajectory and circuit averaging techniques, conversion ratio of the converter can be expressed as given in equation (19).

$$\langle m_c \rangle = F\frac{1}{2\pi}[\frac{1}{2}J_T + \pi + \sin^{-1}J_T + \frac{1}{J_T}(1+\sqrt{1-J_T^{\,2}})] \quad (19)$$

Conversion ratio is controllable by F, but it also depends on J_T. Function of load current dependency is plotted in Fig. 9.

2.2. Mode Boundaries

Consequently, to obtain ZCS condition, some boundary conditions are shown in equations (20) to (23).

$$J_{out} < 1 \quad (20)$$

$$\xi > 0 \quad (21)$$

$$\langle m_c \rangle \le 1 - \frac{J_{out}F}{4\pi} \quad (22)$$

$$F << 1 \quad (23)$$

According to these mode boundaries, design parameters are determined.

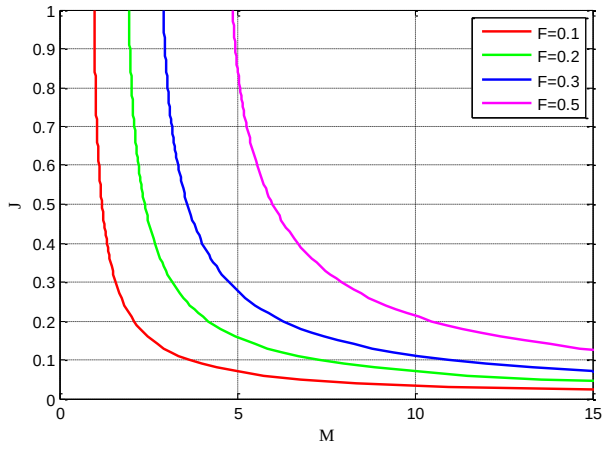


Figure 9 Load current dependency of M for different frequencies

3. DESIGN PARAMETERS

According to specification of the ZCS buck converter given in Table I, resonant elements' parameters (resonant inductance, resonant capacitance, and resonant frequency) are calculated. To calculate resonant elements' parameters two conditions given in equations (24) and (25) must be considered. Firstly, to obtain zero current switching, switching frequency must be much lower than the resonant frequency, and secondly normalized load current value must be lower than 1.

$$f_s << f_o \quad (24)$$

$$(J = \frac{I}{I_{base}} = \frac{I}{V_{in,\min}/R_o}) < 1 \quad (25)$$

Normalized load current value assumed as 0.85 for the worst-case scenario which is minimum input voltage (43V) because lower J_{out} value leads to higher peak resonant inductor current which is undesired for the converter. Using conversion ratio formula and normalized current, resonant tank inductor and capacitor values are calculated and nearest standard values are chosen.

With this equation, resonant frequency is then calculated as 677 kHz. Resonant frequency can be expressed using L_r and C_r as given in equation (26).

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = 677kHz \quad (26)$$

By using these equations, J_{Tmax} can also be expressed in terms of L_r and C_r as given in equation (27).

$$J_{T\max} = \frac{I_T}{I_{base\min}} = \frac{I_T}{\frac{V_{\min}}{R_0}} = \frac{I_T R_0}{V_{\min}} = \frac{5}{43}\sqrt{\frac{L_r}{C_r}} = 0.85 \quad (27)$$

By using these equations, L_r and C_r are calculated as follows.

$$L_r = 1.72\mu H$$

$$C_r = 32.2nF$$

Standard values of 1.8µH and 33nF are selected as resonant tank elements.

With the resonant elements selected, steady-state simulation of the converter was made in order verify ZCS ability. Circuit model shown in Fig. 10, is implemented in PSIM environment. Open-loop simulation is done with nominal input voltage and 60W output power at 168 kHz switching frequency. From the simulation results shown in Fig. 11, ZCS ability of the converter and the voltage conversion ratio is verified.

Table 1 Specifications of the designed converter

Parameter	Unit	Value
Input voltage range	[V]	48 ± 10%
Output voltage	[V]	12
Rated output power	[W]	60
Switching frequency	[kHz]	150 - 200

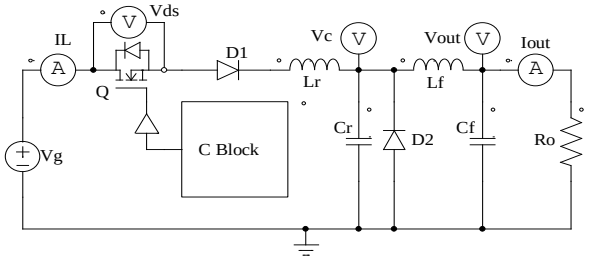


Figure 10 PSIM model of the converter

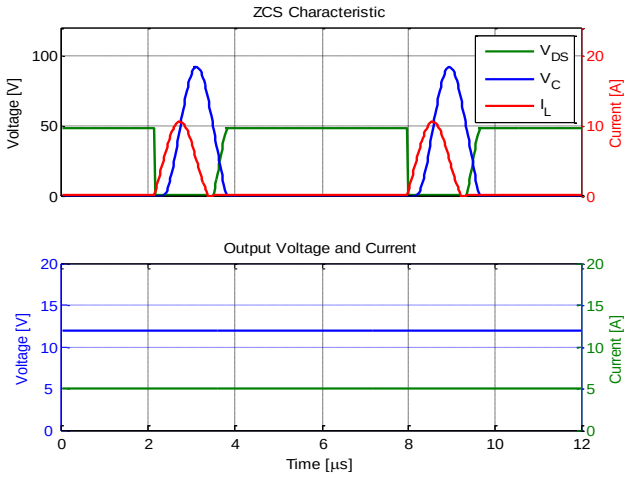


Figure 11 Simulation results at V_g = 48 V, R = 2.4Ω, f_s = 168 kHz

Since the designed converters will be controlled digitally by microcontrollers, closed-loop operation of the converter is also simulated. Necessary compensation function was implemented in "C Block" inside PSIM environment. Closed-loop operation of the system is then verified with the step changes in output load. It is observed that the system outputs the desired output voltage of 12V with no stability problems. Fig. 12 shows the converter response to no-load start and switch to full load when time equals to 40 ms. Transient loading caused output voltage to undershoot about 30% of the rated output voltage and it is recovered in 2 ms by the controller.

Actual implementation of the closed loop control is done for the MKL03Z32VFK4 microcontroller. Embedded software for this microcontroller is developed as a finite state machine with three states. Initialization state starts after power-on-reset. In this state, microcontroller peripherals are set according to the application. Then run state begins. Run state starts the operation of the converter. Voltage is controlled with 200 kHz control loop frequency. Run state flow diagram is given in Fig. 13. Fault state is the last state and it is activated only if the input voltage or current is out of the limits.

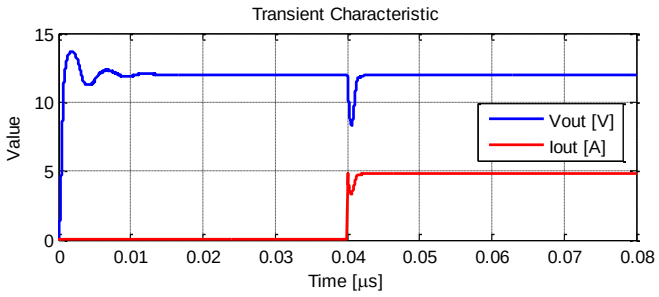


Figure 12 Step response of no load to full load condition

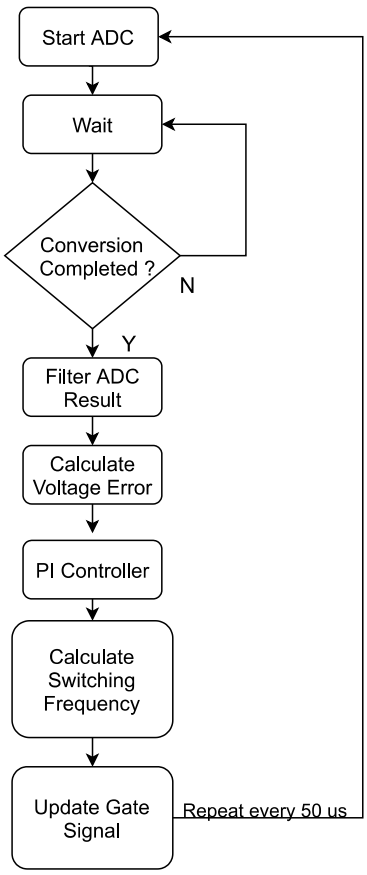


Figure 13 Run state flowchart diagram

4. GATE CIRCUIT DESIGN

After the open-loop and closed-loop operation of the converter is verified in simulation, necessary circuit boards were designed for experimental results. In the buck converter topology, switch element is placed at the high side, meaning that the drain pin of the MOSFET is directly connected to supply voltage. This causes the source pin to be floating. Thus, the applied gate-source voltage has to be floating with reference to ground as well. Two different high-side switching approaches are used in this study.

4.1. High-side Switching Design I

In the first circuit a half-bridge driver IC is used. These drivers have a channel for high side N channel switch. The source pin connection of the driver is floating with reference to ground. Gate-source drive voltage is generated using bootstrap method. However, in order to generate this bootstrapped voltage, source connection of the switch should have a direct reference to ground. In ZCS quasi-resonant buck converter topology, due to series diode and resonant inductor this is not the case. Thus, it can be problematic to use such technique because of possible charge – discharge issues of the bootstrap capacitor. Instead, an isolated DC-DC converter module is used as the floating switch voltage supply. In this topology, gate driver and the microcontroller are placed on the power ground. This provides a simple feedback path from the output by using only one voltage divider. The circuitry is given in block diagram in Fig. 14.

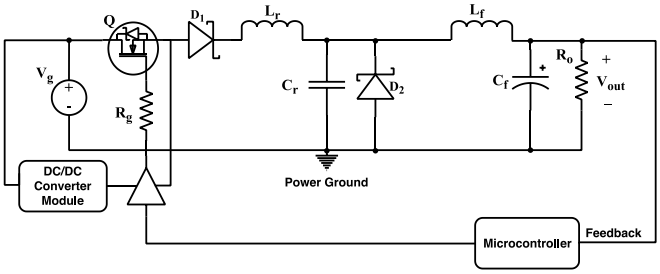


Figure 14 Circuit diagram of design I

4.2. High-side Switching Design II

For the second circuit a different approach is used to eliminate the need of a high side gate driver. Instead, a low side gate driver is used with its ground connected directly to the source pin of the N-channel switch and supplied from an auxiliary 12V input. Supply of the microcontroller is also referenced to this ground providing simple connection between the controller and the gate driver. This placement of the microcontroller ground has a drawback as well. Output voltage is floating with reference to the ground of the microcontroller. Moreover, the voltage difference between these two points is negative, making it not possible to measure the output voltage directly via microcontroller. Instead, an isolated amplifier is used to transfer output voltage with reference to floating ground point. The circuitry is given in block diagram in Fig. 15. Designed circuit boards are shown in Fig. 16. Both PCBs are designed to have a high-power density.

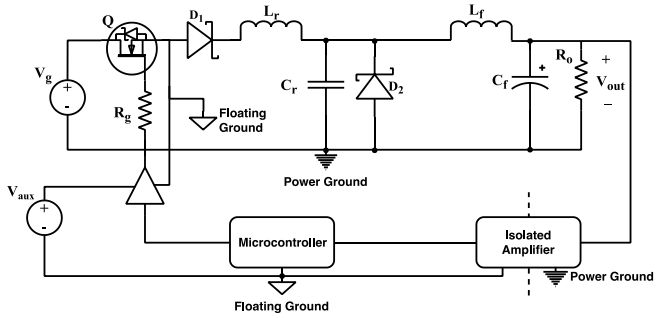


Figure 15 Circuit diagram of design II

a)

b)

Figure 1 (a) Converter I, (b) Converter II

5. EXPERIMENTAL RESULTS

Designed and assembled converter circuits are investigated in experimental operation. Both of the circuits were evaluated for open-loop and closed-loop operation at the nominal operation range. From the first results, a couple of adjustments had to be made. One of which is related to first topology. It is observed that under certain conditions like light load and low switching frequency, the converter works fine. Increasing the load and the switching frequency however, causes the gate driver to fail and get permanent damage on the output side. Reason for this is found as negative voltage spikes on the source pin caused by the parasitic inductance due to semiconductors and PCB layout. Source-to-ground voltage measurement on this point is given in Fig. 17. It can be seen that negative voltage spikes were as high as 6.8V in amplitude. Since there was no direct reference to ground at this point, these spikes were able to cause latch-up on the driver, which specified the maximum repetitive transients as -5V. In order to solve the problem, gate resistor is moved from gate path to source path of the driver. D_3 and D_4 are two schottky diodes placed in order to clamp the negative voltage spikes. Revised topology is given in Fig. 18. With these adjustments, converter was able to work for the whole operation range.

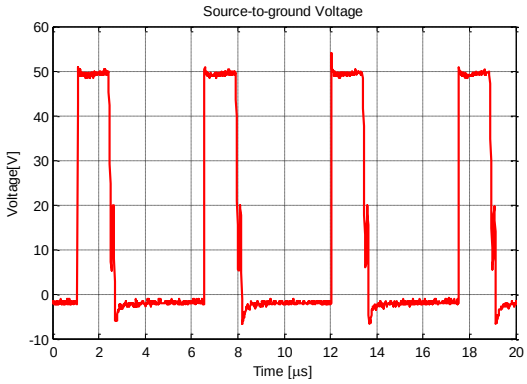


Figure 17 Negative voltage spikes on source connection

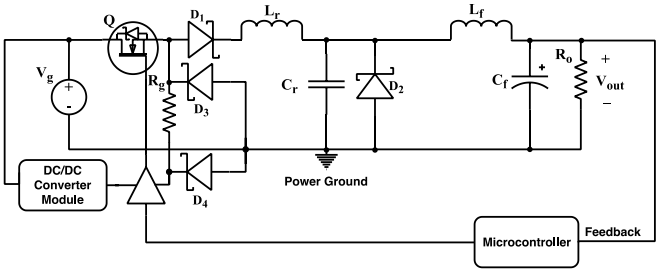


Figure 18 Modified circuit diagram of design I

The second switching topology was far smoother and easier regarding the switching and transients. The only issue was that the microcontroller is placed to the floating ground point that is actually the source connection of the switch. This ground reference has a lot of switching noise and analog measurements are highly affected from these

noises. This made the stable closed loop operation hard to achieve. In order to overcome this issue, embedded software in the microcontroller has adjusted accordingly. Analog Digital Conversion (ADC) is started every PWM cycle. Timing of the ADC is controlled via trigger output from PWM timer. Trigger point is adjusted to ensure conversions start when the switch is fully turned off. Therefore, switching noises could be eliminated from ADC results. First order digital low-pass filter is used to further smoothen voltage measurement. Fig. 19 shows the closed loop response of the system to zero load to full load transition.

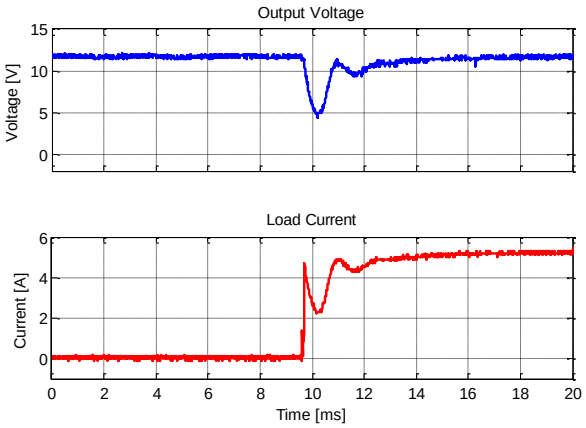
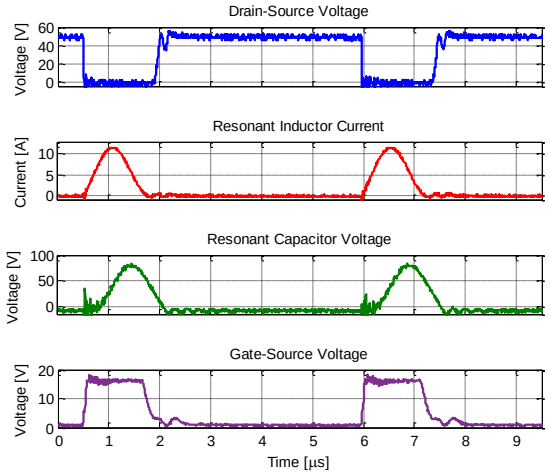


Figure 19 Closed loop response of zero load to full load transition

In the Fig. 20, full load operation waveforms of both converters are given. It can be seen that both converters operate in ZCS.

a)



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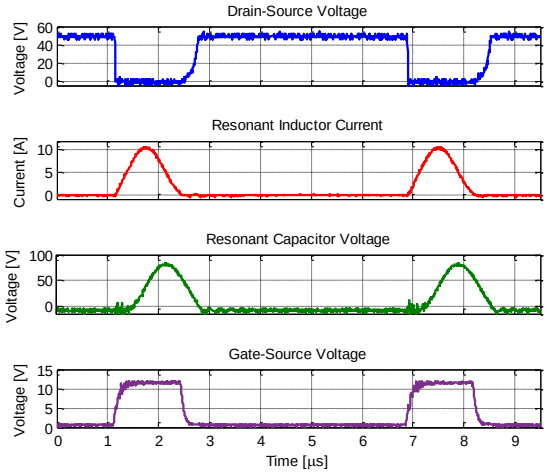

Figure 20 Full load operation waveforms of converter I (a) and converter II (b)

Gate-source and drain-source voltage of the first converter also indicates that the additional diodes placed on the circuit created a path for the circulating energy when the switch is off. Although this does not affect the operating properties of the converter, it decreases the overall efficiency. Especially in the light load operation, low frequency oscillations due to MOSFET's output capacitance and resonant inductance cause undesired currents to flow from the clamping diodes. This drawback can be seen in Fig. 21 that shows the efficiency graphs of both designs.

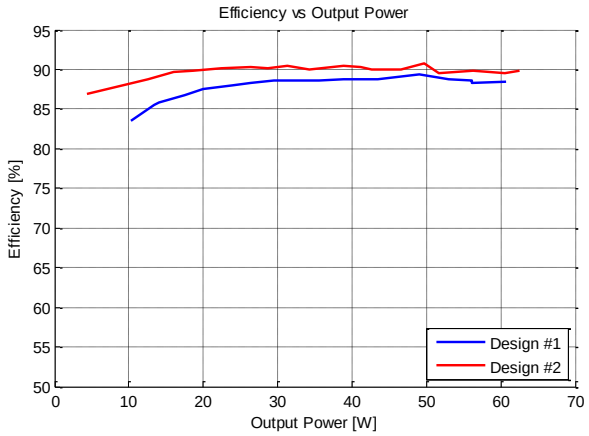

Figure 21 Efficiency curves of the designed converters

6. CONCLUSION

Zero current switching half-wave buck converters are investigated in this study. Steady-state

analysis of the converter is done for a 48V to 12V, 60W step down converter. Resonant tank element values are calculated and selected from standard values in order to provide the given conversion ratio and output power. Closed loop operation of the converter is done by designing a PI controller with the help of the small signal model. Digital type PI controller is simulated in PSIM environment. Two different approaches of non-isolated high side switching technique are utilized. Necessary circuit schematics and printed circuit boards were designed and manufactured. Embedded software for the MKL03Z32VFK4 microcontroller is developed. Experimental results show that both of the converters are able to supply 60W power up to 90% efficiency, having a peak power density of 13.66 W/in^3 zero current switching capability.

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The Declaration of Conflict of Interest/ Common Interest

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Authors' Contribution

Authors contributed equally to the study.

The Declaration of Ethics Committee Approval

This study does not require ethics committee permission or any special permission.

The Declaration of Research and Publication Ethics

The authors of the paper declare that they comply with the scientific, ethical and quotation rules of SAUJS in all processes of the paper and that they do not make any falsification on the data collected. In addition, they declare that Sakarya University Journal of Science and its editorial board have no responsibility for any ethical violations that may be encountered, and that this study has not been evaluated in any academic publication environment other than Sakarya University Journal of Science.

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