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Step-Up DC/DC Converter Based on Partial Power Processing

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ABSTRACT

This paper suggests a maiden topology of step-up dc/dc transformer-less converter on basis of the partial power processing concept which has been integrated with the classic boost converter structure. This converter has a high gain as compared to the conventional boost converter. The input dc power is directly connected to the output capacitors and load without being processed by the converter. Where-through, the voltage stress of semiconductors comes to be lower than output voltage. To verify and clarify the suggested converter, the simulation has been presented along with relevant mathematical principles. In this paper, the basic operating principles of the proposed converter are presented along with some experimental results in prototype lab to demonstrate the effectiveness of this converter.

Keywords*: Boost ability, voltage stress, high gain, dc/dc converter.*

1. INTRODUCTION

As generally identified, step-up dc/dc converters have been widely used in many applications, such as, electric car, photovoltaic (PV) system, fuel cell system, battery powering device, etc., requiring some circuits transferring low voltages to high voltages [1-3]. Generally, the energy conversion systems step-up dc/dc converters are used to provide input voltages to feed the dc/ac converters [4, 5].

Up to now, a number of scholars in their literatures have focused on high step-up dc/dc converters that are either based on (i) the converters with series connection of output voltages (ii) the coupling inductor concept (iii) the switched inductor concept. As whole, the high step-up dc/dc converters can be generally categorized in two groups: with transformer-based and transformer-less [6, 7]. In fact, this paper has dealt with and chased the transformer-less converter. It is worth mentioning that, aforementioned step-up converters encompass different drawbacks. Ref [8] had analyzed the quadratic boost converter that has high voltage conversion ratio. Major problem of this structure which is based on cascaded boost converter is being exposed of high voltage stress on semiconductors. Multilevel boost converter is nowadays regarded as an appropriate solution for very large conversion ratios [9, 10]. The multilevel boost converter needs to have many components such as

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capacitors and diodes that absolutely will result in high complexity and cost-price as well as less reliability. Ref [11] had presented a two-stage converter based on a high-voltage gain switched inductor. By one switch in switched inductor boost converter high gain to be earned. The main drawback of this converter is high PIV of some components. As a matter of fact, some deployed elements in this converter e.g. inductors and diodes are extra as comparison to conventional boost converter. As we know, semiconductor switches in: cascaded, multilevel and switched inductor boost converters tolerate higher current. Thereby, aiding the partial power processing can be taken in as a good solution to heighten the performance of the dc/dc converters [12-14]. Also, ref [13] suggested a dc/dc power converter for distributed photovoltaic (PV) plant architectures with simplicity and high efficiency. High proficiency of this structure will be earned by a portion of the input PV power which is directly fed forward to the output without being processed by the converter [12, 13].

Considering aforementioned topologies, this paper suggests a step-up transformer-less converter with high voltage conversion ratio, that its inductors are magnetized with the input voltage. The voltage stress of semiconductors comes to be lower than output voltage. Meantime, it has same behavior like to the conventional boost converter; hence, the control of this converter can be feasibly and easily realized. To verify and clarify the suggested converter, the experimental prototype has been presented along with relevant mathematical principles. Subsequently, both the MATLAB simulation and experimental results will have transparently corroborated the aforementioned expression regarding to suggested converter.

2. DC/DC CONVERTER

2.1. Analysis of proposed step-up dc/dc converter

The schematic of step-up dc/dc converter is shown in Figure 1. It contains two inductors L_1 and L_2, two diodes D_1 and D_2, two output capacitors C_1 and C_2, two MOSFET switches T_1 and T_2, and one output resistor R_o.

In this study, all the elements are presumed to be ideal, and the other related noisy parameters are ignored. Also, the ripples of the capacitor voltages aren't considered. It must be noted that, it is essential that the converter operates in continuous conduction mode (CCM) for the renewable power system applications, here, steady-state behavior of the converter have been analyzed in CCM.

The output voltage V_O can be presented by

$$V_o = V_{C1} + V_{C2} + V_{in} \quad (1)$$

In suggested converter, part of the input power is directly fed forward to the output. By controlling two switches of this structure four states will be revealed, i.e.: following stages:

Mode 1: triggering the T_1 and T_2, this causes the output diodes (D1 and D2) to be turned off, and inductors are charged in parallel. Considering Figure 2, Energy of output capacitors is rendered to load and capacitors will be located in discharge mode.

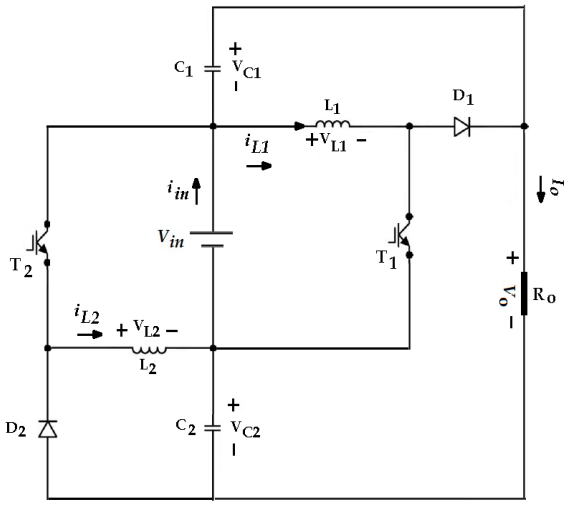


Figure1. The circuit of the proposed DC/DC converter.

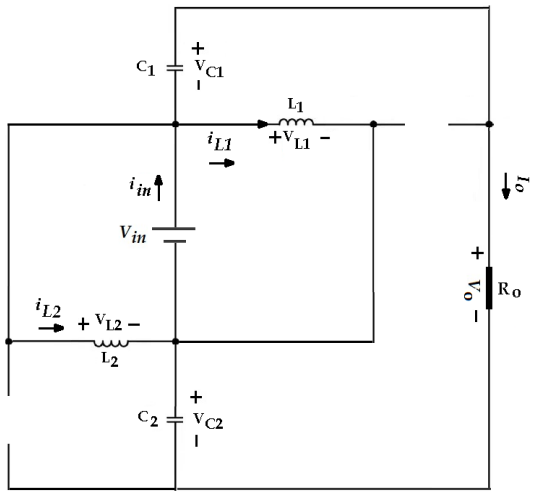


Figure 2. Mode 1.

$$V_{L1} = V_{L2} = V_{in} \quad (2)$$

$$i_{C1} = i_{C2} = -i_o \quad (3)$$

Mode 2: T_1 is triggered and T_2 is off, this mode $D_2$and D_1turned to be on off, respectfully. This operation leads to positive and negative values for the voltages of $L_1$and L_2, respectfully. Energy is transferred to C_2 while C_1gives its energy to load. Considering Figure 3, during mode 2, the voltage across the inductors is:

$$V_{L1} = V_{in} \quad (4)$$

$$V_{L2} = -V_{C2} \quad (5)$$

$$i_{C1} = -i_o \quad (6)$$

$$i_{C2} = -i_o + i_{L2} \quad (7)$$

Mode 3: this condition is reverse of Mode 2, i.e.: $T_2$and D_1 are on, and$T_1$and $D_2$are off.

This operation leads to positive and negative values for the voltages of $L_2$and L_1, respectfully. Energy is transferred to C_1while C_2gives its energy to load. Considering Figure4, during mode 3, the voltage across the inductors is:

$$V_{L2} = V_{in} \quad (8)$$

$$V_{L1} = -V_{C1} \quad (9)$$

$$i_{C1} = -i_o + i_{L1} \quad (10)$$

$$i_{C2} = -i_o \quad (11)$$

Mode4: this condition is reverse of Mode 1, i.e.: both the T_1 and $T_2$are off which causes D_1 and D_2 to be turned on, and subsequently the inductors will be discharged. The capacitors will be located in charge mode. Considering Figure 5 shows mode 4,during mode 4, the voltage across the inductors is:

$$V_{L1} = -V_{C1} \quad (12)$$

$$V_{L2} = -V_{C2} \quad (13)$$

$$i_{C1} = -i_o + i_{L1} \quad (14)$$

$$i_{C2} = -i_o + i_{L2} \quad (15)$$

Here, a constant frequency pulse-width modulation (PWM) shown in Figure 6 is appropriate for the presented converter.

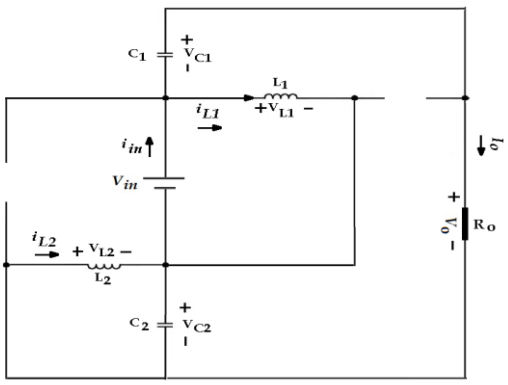


Figure3. Mode 2.

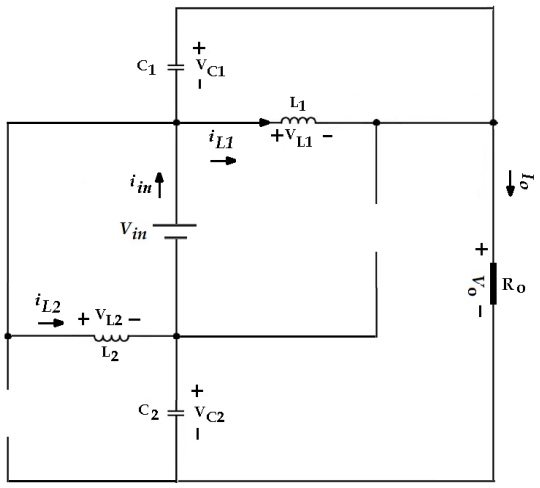


Figure4. Mode 3.

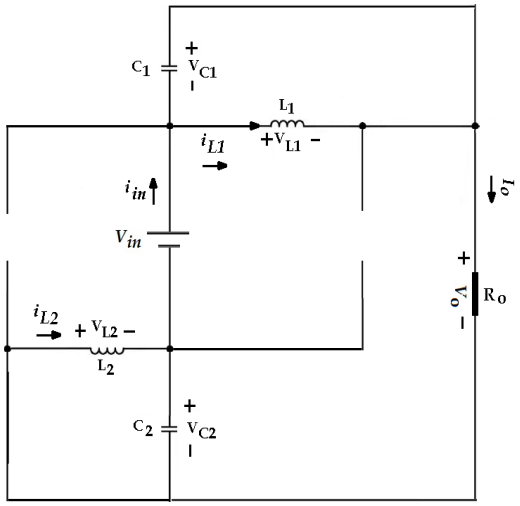


Figure 5. Mode 4.

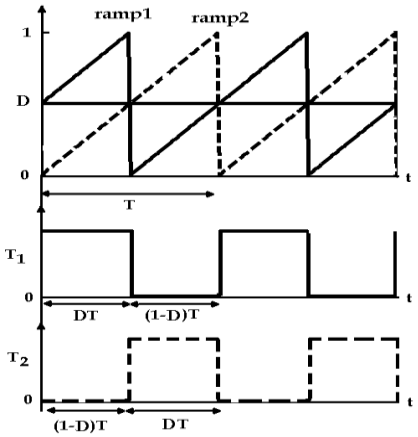


Figure 6. A constant frequency pulse-width modulation (PWM) scheme.

In Figure 6, D is the control signal and the saw-tooth ramp waveforms are the carrier waveforms of the modulation. While, one of the saw-tooth ramp waveforms is shifted by 180° with respect to another. The ramps have a period T and peak to peak voltage of 1 volt.

Applying voltage-second balance requirement on L_1 and L_2 and assuming $C_1=C_2$ and $L_1=L_2$, following equations are extracted [11]:

$$\overline{V_{L1}} = 0 = D.V_{in} + (1-D)(-V_{C1}) \Rightarrow \quad V_{C1} = \frac{DV_{in}}{(1-D)} \tag{16}$$

$$\overline{V_{L2}} = 0 = D.V_{in} + (1-D)(-V_{C2}) \Rightarrow \quad V_{C2} = \frac{DV_{in}}{(1-D)} \tag{17}$$

From (1), the static gain of the converter can be presented as follows:

$$V_o = \frac{(1+D)V_{in}}{(1-D)} \tag{18}$$

It is considered that the load current be constant. Likewise, with presence of capacitor charge balance yield the following equations for the proposed converter model

$$i_o = I_{oav} = I_{orms} = I_o \tag{19}$$

$$\overline{i_{c1}} = 0 = -D.I_o + (1-D)(I_{L1av} - I_o) \Rightarrow \quad I_{L1av} = \frac{I_o}{(1-D)} \tag{20}$$

$$\overline{i_{c2}} = 0 = -D.I_o + (1-D)(I_{L2av} - I_o) \Rightarrow \quad I_{L2av} = \frac{I_o}{(1-D)} \tag{21}$$

The voltage ripple of output capacitors are shown as:

$$\Delta V_{Ci} = \frac{D.T.I_o}{C_i} \qquad i = 1,2 \tag{22}$$

The current ripple of inductors can be expressed

$$\Delta i_{Li} = \frac{D.T.V_{in}}{L_i} \qquad i = 1,2 \tag{23}$$

The root mean square current of capacitors can be calculated as follows

$$I_{Cirms} = \sqrt{\frac{1}{(1-D)}} I_o \qquad i = 1,2 \tag{24}$$

Hence, the dc inductor current boundary between CCM and DCM is

$$I_{LB} = \frac{\Delta i_L}{2} = \frac{D.T.V_{in}}{2L} \Rightarrow \quad \frac{D.T.V_o(1-D)}{2L(1+D)} = \frac{I_o}{(1-D)} \tag{25}$$

The normalized magnetizing-inductor time constant of inductors is defined by:

$$\tau_{Li} = \frac{L_i}{T.R_o} = \frac{D.(1-D)^2}{2(1+D)} \qquad i = 1,2 \tag{26}$$

The curves of normalized magnetizing-inductor time constant of inductors are indicated in Figure 7.

2.2. Ratings of semiconductors

A challenging issue in power electronic converters is the ratings of semiconductors. In other word, voltage and current ratios of the semiconductors in a converter have a direct relationship with the cost-price.

The voltage Stress(VS) on semiconductor can be presented by:

$$VS_{T1} = VS_{T2} = VS_{D1} = VS_{D2} = \frac{V_{in}}{(1-D)} \tag{27}$$

As can be seen from (27), VS of semiconductor is lower than output voltage. Provided inductors to be adequately large, their currents will be constant in one period. The root mean square (rms) and average (av) current of semiconductors given as follows are based on current of inductors, presuming $I_{L1av}=I_{L2av}$.

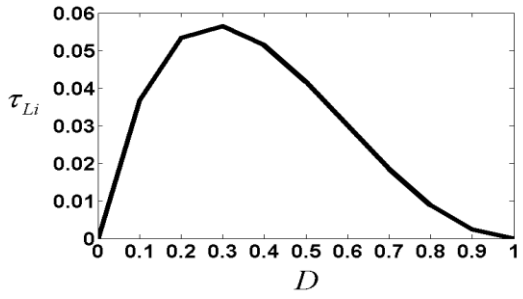


Figure 7. Curves of normalized magnetizing-inductor time constant of inductors.

$$i_{T1} = \begin{cases} I_{L1av} & DT \\ 0 & (1-D)T \end{cases} \tag{28}$$

$$I_{T1rms} = I_{T2rms} = \sqrt{D} I_{L1} = \frac{\sqrt{D} I_o}{(1-D)} \quad (29)$$

$$I_{T1av} = I_{T2av} = D I_{L1} = \frac{D I_o}{(1-D)} \quad (30)$$

$$i_{D1} = \begin{cases} 0 & DT \\ I_{L1av} & (1-D)T \end{cases} \quad (31)$$

$$I_{D1rms} = I_{D2rms} = \sqrt{\frac{1}{(1-D)}} I_o \quad (32)$$

$$I_{D1av} = I_{D2av} = (1-D) I_{L1} = I_o \quad (33)$$

2.3. Example to prove the equation

To confirm the correction of the analyses done above, a simulation is implemented in ideal state. The parameters of the circuit are given in Table 1. The duty cycles of the signals applied to power switches T_1 and T_2 are 50%. The output voltage and current are shown in Figure 8. Figure 8 proves (18) as:

$$V_o = \frac{(1+0.5)*30}{(1-0.5)} = 90 \quad (34)$$

Table 1: Parameters.

DC source	30 V
L_1 and L_2	2500 µH
C_1 and C_2	100 µF
Switching frequency	25 KHz
D	0.5
R_o	90 Ω

The output voltage and current of semiconductors are depicted in Figure 9 and 10. Figure 9 proves (27) as:

$$VS_{T1} = \frac{30}{(1-0.5)} = 60 \quad (35)$$

Figure 11 shows the voltage and current waveforms of the inductors. The current ripple of inductors are 0.24 A in Figure 10 that proves (23).

$$\Delta i_{L1} = \frac{0.5*30}{25000*2.5*10^{-3}} = 0.24 \quad (36)$$

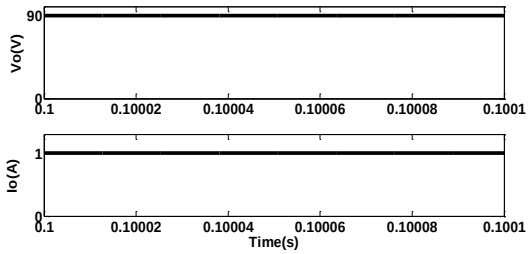


Figure 8. Output Voltage and current.

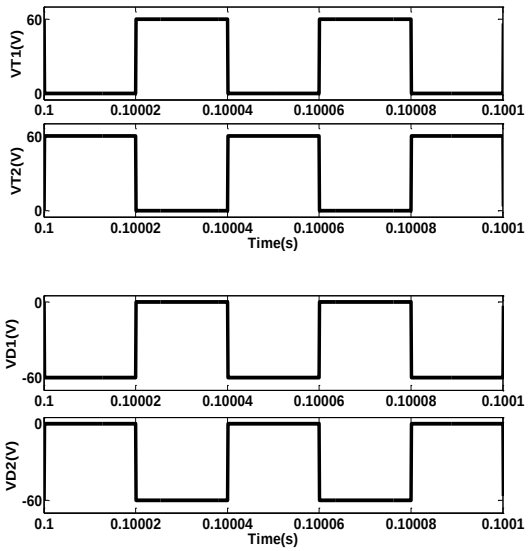


Figure 9. Voltage of semiconductors.

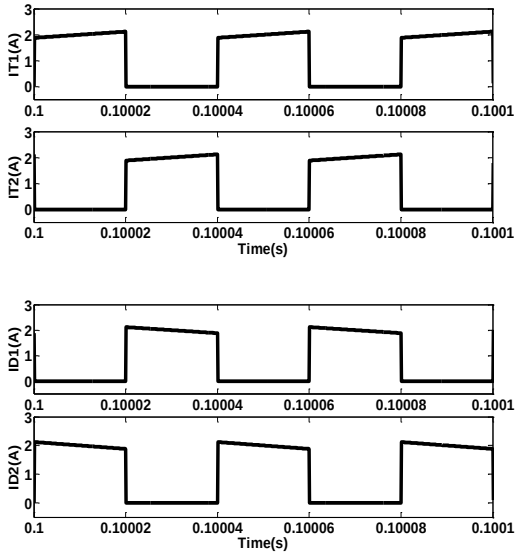


Figure 10. Current of semiconductors.

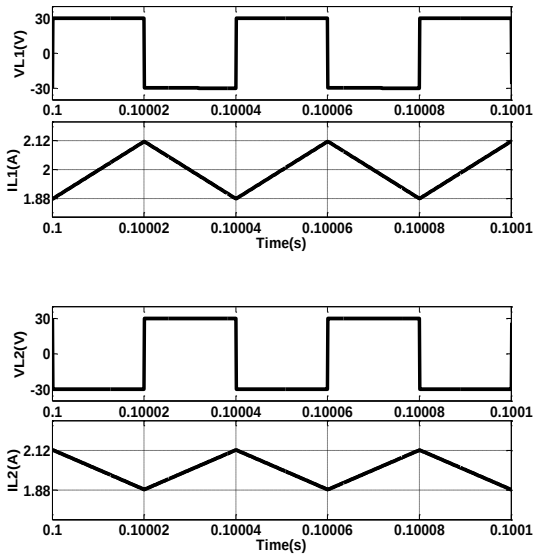


Figure 11. Voltage and current of inductors.

Figure 11 shows the voltage and current of the capacitors. The voltage ripple of capacitors are 0.2 V in Figure 11 that proves (22).

$$\Delta V_{C1} = \frac{0.5*1}{25000*100*10^{-6}} = 0.2 \quad (37)$$

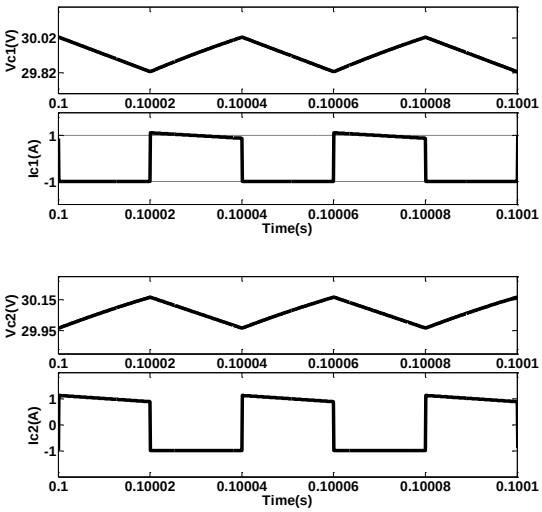


Figure 12. Voltage and current of capacitors.

2.4. Power loss calculation

What is evident, all elements in power electronic converters have losses. In proposed converter, the elements of inductors, capacitors and semiconductor create power losses [15, 16]. Considering passive components, capacitors and inductors have internal resistant [11], the conduction losses of inductors can be:

$$P_{RL} = R_L I_{Lav}^2 \quad (38)$$

Also, the power losses in capacitors:

$$P_{RC} = R_C I_{Crms}^2 \quad (39)$$

As well as the conduction losses of the diodes:

$$P_{RD} = R_D I_{Drms}^2 \quad (40)$$

$$P_{VD} = V_{FD} I_{Dav} \quad (41)$$

Where, R_D and V_{FD} are the diode resistance and threshold voltage, respectfully.

The conduction loss of the power switch is

$$P_{RT} = R_T I_{Trms}^{\ 2} \quad (42)$$

Where, R_T is switch on resistance. When switches have non-ideally operated, The switching losses appeared [16].

$$P_{swT} = (E_{on} + E_{off}) f \quad (43)$$

E_{on} and E_{off} indicate the energy losses in on and off conditions, and f indicates the switching frequency.

As whole, the total power loss of the converter can be presented by:

$$P_{Loss} = P_{RL1} + P_{RL2} + P_{RC1} + P_{RC2} + P_{RD1} + P_{VD1} + P_{RD2} + P_{VD2} + P_{RT1} + P_{RT2} + P_{swT1} + P_{swT2} \quad (44)$$

3. COMPARISON STUDY

As can be seen in Figure 13 comparison has been performed between the gain of the proposed converter and conventional boost converter in ideal case. It is obvious that the gain of the proposed converter is higher than the conventional boost converter by a factor of (1+D). The gain of suggested converter is the same as dc/dc converter of presented system in [11].

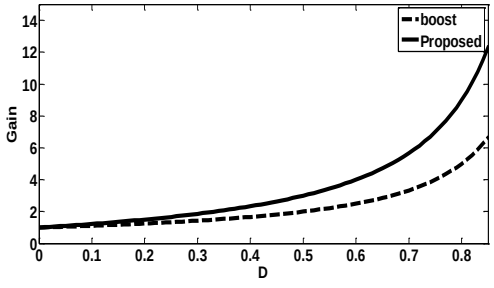


Figure 13. Comparison between the gain of the proposed and classic boost converters.

It must be noted that, the suggested converter engages two switches while presented dc/dc converter in [11]

has one switch nonetheless the voltage and current stress of switch and diode of [11] is higher than proposed converter. The salient advantage of suggested converter is high efficiency which is achieved by having a portion of the input dc power directly fed forward to the output without being processed by the converter.

The presented converter in [13] applies partial power processing technique while conventional boost converter and some of new dc/dc converters such as converter of [10] and [11] have no advantage. The gain of presented converter in [13] is lower than suggested converter, whereas, the voltage stress of switches is higher than suggested converter.

4. EXPERIMENTAL RESULTS

To scrutinize the performance of the suggested dc/dc converter regarding to the generation of a desired output voltage and subsequently to confirm above done analysis, the experimental prototype of this structure has been manufactured. The parameter values of experimental prototype of suggested converter are presented in Table 1. Figure 14 shows the circuit of prototype. MOSFETs of the prototype are IRF840. TLP250 has been used as IC driver. U1560 is engaged as fast diodes. The DSPTSM320F28335 microcontroller has created the switching patterns.

Figure 15 shows gate source voltage of switches. In each time, only one switch is turned on. The voltage of T_1 and D_1 is shown in Figure 16. The measured voltage phases of T_1 and D_1 are similar which are shifted by 180°, and also for T_2 and D_2. The voltage and current of inductors are presented in Figure 17. When positive voltage is located in the inductor the inductor is charged, and vice versa. Meantime, Figures 18 and 19 show the dc source current and output voltage.

Figure 14. Circuit of prototype.

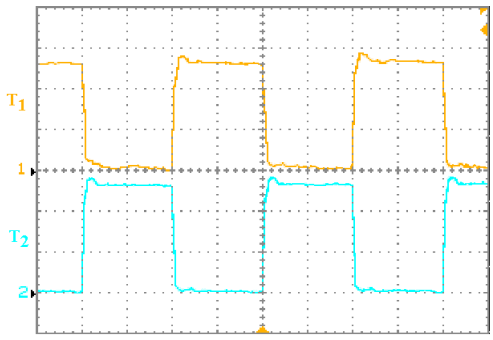


Figure. 15. Gate source voltage of switches (volt/div=5V and Time/div=10µs).

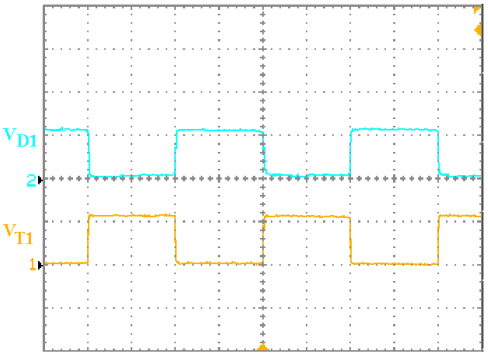
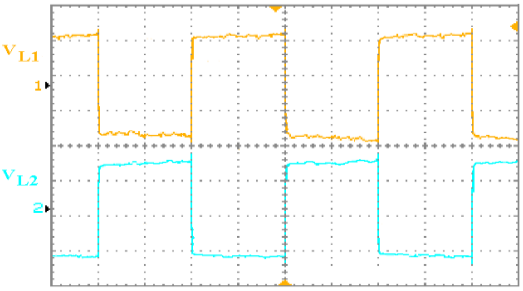
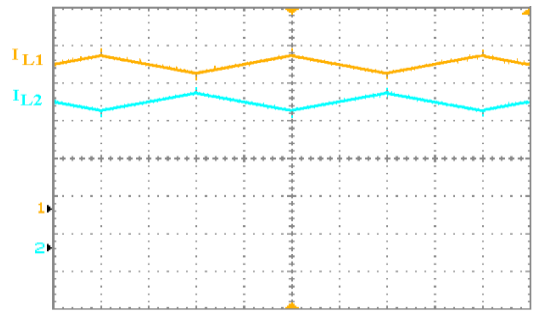


Figure 16. Voltage of T_1 and D_1(volt/div=50V and Time/div=10µs).



(a)



(b)

Figure. 17. Voltage and current of inductors (a) voltages (volt/div=20V) and (b) currents (Ampere/div=500mA) and Time/div=10µs.

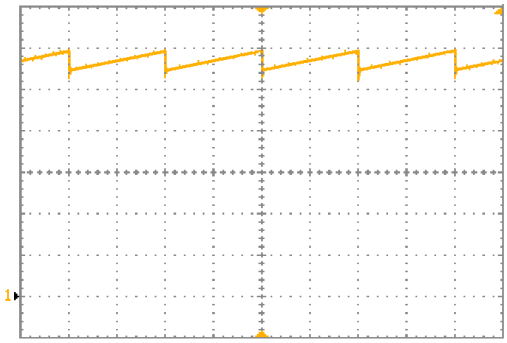


Figure. 18. Current of source (i_{in}) (Ampere/div=500mA and Time/div=10µs).

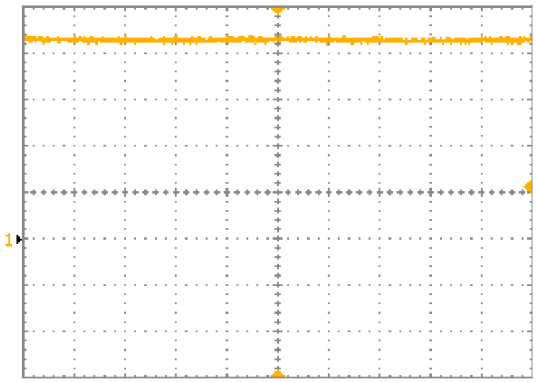


Figure. 19. Output voltage (volt/div=20V and Time/div=10µs).

5. CONCLUSION

A maiden topology of step-up dc/dc transformer-less converter has been presented in this paper. The salient advantage of suggested converter which is chased, scrutinized and confirmed is higher gain as compared too there conventional boost converter. Meantime, it is worth mentioning that, the suggested topology encompasses the switches and diodes with low standing voltage on semiconductors. The quasi-mathematical analysis that is performed in relevant section has confirmed the suggested system idea and its mentioned advantages. Furthermore, the results of experimental prototype of suggested converter have corroborated the results of MATLAB simulation.

CONFLICT OF INTEREST

No conflict of interest was declared by the authors.

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