Reduction of Output Impedance of Buck Converter with Genetic Algorithm

Farzin Asadi

***Abstract*—This paper introduces a technique to reduce the output impedance in the PWM buck converters with voltage-mode control (VMC) without requiring low Equivalent Series Resistance (ESR) output capacitors. Proposed technique uses the infinity norm (H_∞) to convert the problem into an optimization problem. Obtained optimization problem is solved with the aid of Genetic Algorithm (GA). The proposed technique is applied to a sample buck converter operating in Continuous Conduction Mode (CCM). Simulink simulation is used to test the suggested method. Simulation results showed a considerable decrease in the low frequency region of output impedance. Such a decrease in output impedance is very desired for low voltage high current loads like computer CPU's.**

Index Terms— **DC-DC converters, load transients, output impedance of buck converter, State Space Averaging (SSA).**

I. INTRODUCTION

MANY ATTEMPTS have been made to improve the dynamic response of PWM buck converters to a step change in load current. In [1] an averaged model of an active clamp buck converter was obtained. In this paper, output impedance of the active clamp buck converter has been modeled including the clamp capacitor effect. In [2] V2 control is used to achieve fast transient response. V2 control can take advantage of the instant feedback of the output voltage during the load transient and delay of the error amplifier is eliminated. In [3] the effects of various control techniques on the transient response of switching power supply have been discussed and compared. In this paper, transient response of switching power supply is improved by using double voltage loop control technique. In [4] the transient response of the Voltage Regulator Module (VRM) output voltage when the processor has a fast load change is analyzed. Effect of parasitic are considered in this paper. In [5] fast and efficient controller for a buck converter which supplies a microprocessor is developed and tested. Experimental data shows: tight static and dynamic regulation (± 55mV), fast transient response (within 1us), high efficiency (up to 90%), and stable operation with good noise immunity. [6] used hysteretic current-mode control in Continuous Conduction Mode (CCM) to control a Buck converter which feeds a low voltage microprocessor load. Experimental results for a 5.0 V input, 3.1V output, 13A Buck converter are included to verify the design. In [7] analytical equations are derived for a DC-DC converter at high slew-rate load current transients. The analyzed model includes synchronous buck converter, controller, output capacitor and supply bus parasitic. This paper studies the impacts of system parameters on output voltage transient response. [8] studied the role of the inductor on dynamic response of the converter and used optimization to determine the best value to obtain a fast response for loads like microprocessor. [9] presented a method to synthesis a zero-impedance converter. This method requires both a positive current feedback and a negative voltage feedback for synthesis as well as a current sensing device. [10] presented a method to achieve near optimum dynamic regulation by combining feed-forward of the output current and input voltage with current-mode control (CMC). A common method used in industry to control the output impedance is to use many output filter capacitors placed in parallel to reduce the ESR. In this approach, the feedback compensator is designed to provide the loop gain and phase margin for stability and the peak closed-loop output impedance is achieved through proper selection of low ESR output capacitors.

Feedback control is another technique to decrease the output impedance of a converter. [11] discussed the technical motivation behind compensation, derivation of analytical and design oriented transfer functions. It provides an illustrative example as well. [12] used loop shaping to design an optimum controller for a buck converter. Loop shaping method is easy and intuitive and the controller can be designed accurately for a specific phase margin and cross over frequency. [13] is a tutorial on how to design different types of classic controllers for a Buck converter. [14] presents the internal control loop operation of the BQ 2472x/3x Buck controller IC as well as the external compensator design guideline. It contains a design example based on practical specifications is demonstrated. [15-17] contains some guidelines to select the components of a second order compensation network which controls a buck converter. [18] discussed the digital PI controller design procedure for a buck converter. Experimental results showed the effectiveness of designed controller to keep the output voltage stable despite of disturbances like input voltage variations and output load changes. [19] discussed the procedure to extract the input and output impedance of dc-dc converters. Input and output impedance of buck, buck-boost and boost converters are studied there. Extraction of small

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signal model is the first step for designing a linear controller for a converter. [20] discussed the procedure to extract the small signal linear model of dc-dc converters. [21] used a synchronous buck converter with Gallium Nitride (GaN) to design a driver for a laser diode. Use of GaN based switch increased the efficiency to 96.6%.

In this paper effect of parasitic elements on the operation of the converter is studied. This paper introduces a technique to reduce the output impedance in the PWM buck converters. The technique translates the reduction of output impedance into an optimization problem. Obtained optimization problem is solved with the aid of GA.

This paper is organized as follows: Dynamics of buck converter is studied in the second section. Small signal transfer functions of buck converter are extracted with the aid of State Space Averaging (SSA). Third section introduces the suggested technique. Simulink simulations are done in the fourth section. Finally, suitable conclusions are drawn.

II. DYNAMICS OF THE BUCK CONVERTER

The circuit diagram of an open-loop buck converter is shown in Fig. 1. The buck converter composed of two switches, a MOSFET switch and a diode. In this schematic, Vg, rg, L, rL, C, rC and R shows input DC source, input DC source internal resistance, inductor, inductor ESR, capacitor, capacitor ESR and load, respectively. iO is a fictitious current source added to the schematic in order to calculate the output impedance of converter. In this section we assume that converter works in CCM. MOSFET switch is controlled with the aid of a Pulse Width Modulator (PWM) controller. MOSFET switch keeps closed for $D.T$ seconds and $(1-D).T$ seconds open. D and T show duty ratio and switching period, respectively.

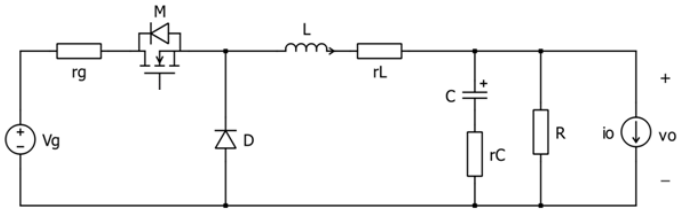

Fig. 1. Schematic of a buck converter.

When MOSFET is closed, the diode is opened (Fig. 2).

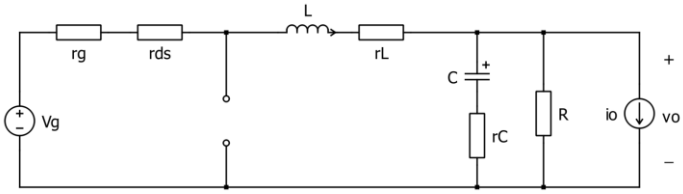

Fig. 2. Equivalent circuit of a buck converter for closed MOSFET.

The circuit differential equations can be written as:

$$\begin{cases}\dfrac{di_L(t)}{dt}=\dfrac{1}{L}\left(-\left(r_g+r_{ds}+r_L+\dfrac{R\times r_C}{R+r_C}\right)i_L-\dfrac{R}{R+r_C}v_C+\dfrac{R\times r_C}{R+r_C}i_O+v_g\right) & (1)\\ \dfrac{dv_C(t)}{dt}=\dfrac{1}{C}\left(\dfrac{R}{R+r_C}i_L-\dfrac{1}{R+r_C}v_C-\dfrac{R}{R+r_C}i_O\right) & (2)\end{cases}$$

$$v_o=r_C C\frac{dv_C}{dt}+v_C=\frac{R\times r_C}{R+r_C}i_L+\frac{R}{R+r_C}v_C-\frac{R\times r_C}{R+r_C}i_O \quad (3)$$

When MOSFET is opened, the diode is closed (Fig. 3).

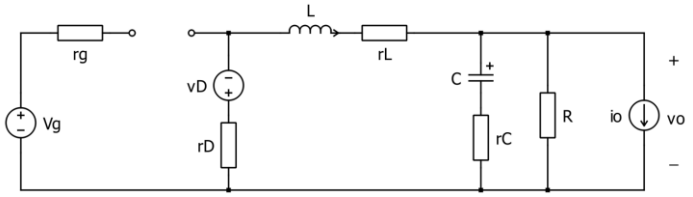

Fig. 3. Equivalent circuit of a buck converter for opened MOSFET.

The circuit differential equations can be written as:

$$\begin{cases}\dfrac{di_L(t)}{dt}=\dfrac{1}{L}\left(-\left(r_D+r_L+\dfrac{R\times r_C}{R+r_C}\right)i_L-\dfrac{R}{R+r_C}v_C+\dfrac{R\times r_C}{R+r_C}i_O-v_D\right) & (4)\\ \dfrac{dv_C(t)}{dt}=\dfrac{1}{C}\left(\dfrac{R}{R+r_C}i_L-\dfrac{1}{R+r_C}v_C-\dfrac{R}{R+r_C}i_O\right) & (5)\end{cases}$$

$$v_o=r_C C\frac{dv_C}{dt}+v_C=\frac{R\times r_C}{R+r_C}i_L+\frac{R}{R+r_C}v_C-\frac{R\times r_C}{R+r_C}i_O \quad (6)$$

State Space Averaging (SSA) can be used to extract the small signal transfer functions of the DC-DC converter. The procedure of state space averaging is explained in detail in [22] and [23].

The MATLAB program applies the SSA procedure to a buck converter with component values as given in Table 1. Component (the capacitor, the inductor and the load resistance) values shown in Table 1 are calculated with the aid of the procedure given in [22]. In this table, for the sake of simplicity, typical values are assumed for diode and MOSFET parameters.

TABLE I
THE BUCK CONVERTER PARAMETERS

	Nominal Value
Output voltage, Vo	1.5 V
Duty ratio, D	0.156
Input DC source voltage, Vg	12 V
Input DC source internal resistance, rg	0 Ω
MOSFET Drain-Source resistance, rds	15 mΩ
Capacitor, C	3290 µF
Capacitor ESR, rC	1.4 mΩ
Inductor, L	13 µH
Inductor ESR, rL	9 mΩ
Diode voltage drop, vD	0.39 V
Diode forward resistance, rD	15 mΩ
Load resistor, R	0.2-3 Ω
Nominal load resistor	1 Ω
Switching Frequency, Fsw	200 kHz

Following results are obtained after running the MATLAB code:

$$\frac{\tilde{v}_o}{\tilde{\imath}_o}=0.0476\frac{(s+6079)(s+1846)}{s^2+5799s+2.28\times10^7} \quad (7)$$

$$\frac{\tilde{v}_o}{\tilde{v}_g}=571.43\frac{(s+6079)}{s^2+5799s+2.28\times10^7} \quad (8)$$

$$\frac{\tilde{v}_o}{\tilde{d}}=45385\frac{(s+6079)}{s^2+5799s+2.28\times10^7} \quad (9)$$

Bode diagram of these transfer functions are shown in Figs. 4, 5 and 6. All of the obtained transfer functions are stable and minimum phase since they don't have any pole or zero in the Right Half Plane (RHP). Based on the obtained results, the dynamic model shown in Fig. 7 can be suggested to the studied converter.

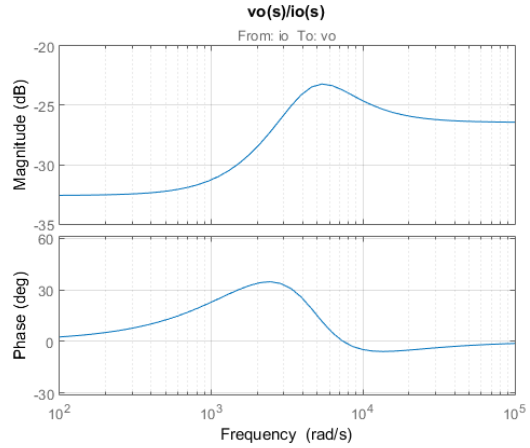

Fig. 4. Bode diagram of $\frac{\tilde{v}_o}{\tilde{\imath}_o} = 0.0476\frac{(s+6079)(s+1846)}{s^2+5799s+2.28\times10^7}$.

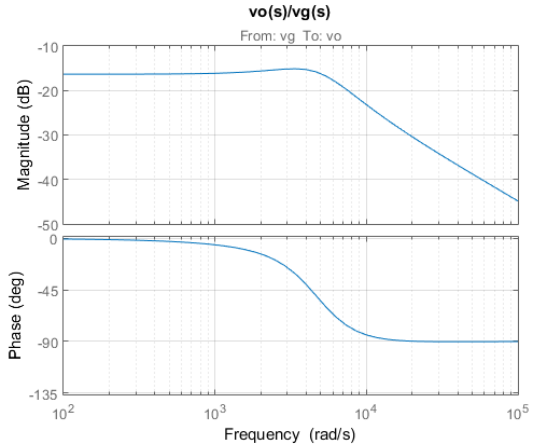

Fig. 5. Bode diagram of $\frac{\tilde{v}_o}{\tilde{v}_g} = 571.43\frac{(s+6079)}{s^2+5799s+2.28\times10^7}$.

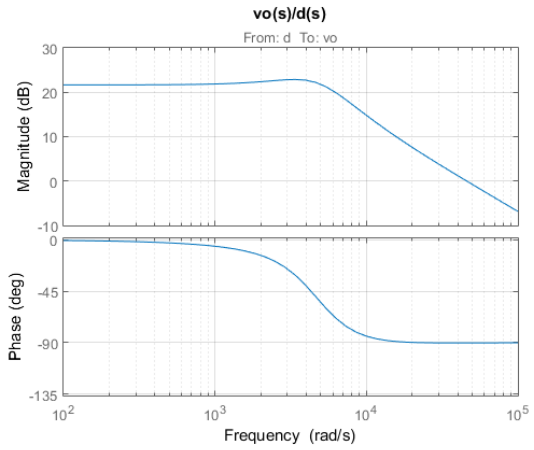

Fig. 6. Bode diagram of $\frac{\tilde{v}_o}{\tilde{d}} = 45385\frac{(s+6079)}{s^2+5799s+2.28\times10^7}$.

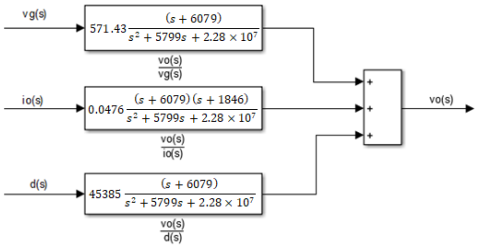

Fig. 7. Dynamical model of the studied buck converter.

III. SUGGESTED METHOD

This section introduces the suggested method. Infinity norm and genetic algorithm make the foundations of the proposed method and are studied briefly.

A. $\boldsymbol{H}_\infty$ *Norm*

The steady-state output of the SISO stable system,

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{10}$$

to the input function,

$$u(t) = asin(\omega t + \varphi) \tag{11}$$

with unknown $a \neq 0$, ω, $\varphi \in \mathbb{R}^1$ is

$$y_{ss}(t) = |G(j\omega)|.a.\sin\left(\omega t + \varphi + arg\left(G(j\omega)\right)\right) \tag{12}$$

where $G(s) = C(sI - A)^{-1}B$. The H_∞-norm is the maximal possible amplification, i.e.

$$\|G(.)\|_\infty = \frac{\underset{\omega \in \mathbb{R}^1}{sup}|G(s).U(s)|}{\underset{\omega \in \mathbb{R}^1}{sup}|U(s)|} = \underset{\omega \in \mathbb{R}^1}{sup}|G(j\omega)| \tag{13}$$

The H_∞-norm of a MIMO system is its maximum singular value [24].

$$\|G(.)\|_\infty = \underset{\omega}{sup}\,\bar{\sigma}\{G(j\omega)\} \tag{14}$$

The H_∞-norm of a scalar transfer function can be obtained graphically. Infinity norm of a SISO system G is the distance in the complex plane from the origin to the farthest point on the Nyquist plot of G, and it also appears as the peak value on the Bode magnitude plot of $|G(j\omega)|$. For instance, the infinity norm of $G(s) = \frac{10}{s+0.4s+10}$ is 7.91. Bode plot of $G(s) = \frac{10}{s+0.4s+10}$ is shown in Fig. 8. Maximum of the Bode graph occurs around 42 $\frac{\text{Rad}}{\text{s}}$ and its value is 17.96 dB which is equivalent to gain of $10^{\frac{17.96}{20}} = 7.91$.

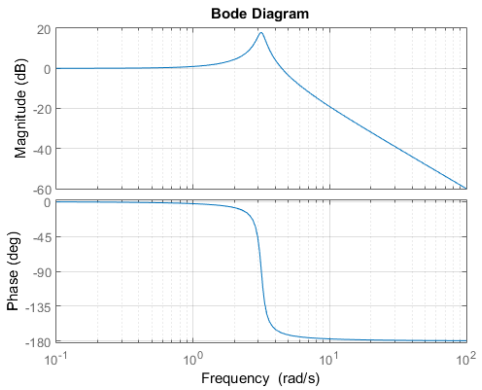

Fig. 8. Bode plot of $G(s) = \frac{10}{s+0.4s+10}$. Peak occurs at 3.15 Rad/s with magnitude of 17.96 dB.

B. Genetic Algorithm (GA)

In 1960 the first serious investigation into Genetic Algorithm (GA) was undertaken by John Holland. These search techniques are based on the process of biological evolution and are used to provide useful solutions to optimization and search problems. As they are based on biological evolution, they use techniques that are emulated from the concepts of inheritance, mutation and selection.

Genetic algorithms explore a parameter space while optimizing a function. The problem is broken down into a *population* of candidate solutions which are refined over a number of *generations*.

A single candidate solution is represented by a *chromosome* which essentially encodes all of the optimizable parameters into a single entity. Each candidate is ranked using a fitness function and those with the best fitness score are selected for further refinement. The refinement stage then operates on each of the chromosomes by

I) *breeding* - a process where a new population of improved candidates are generated using the present generation's population, and

II) *mutation* - in which chromosomes are modified in some way.

Both of these operations permit the parameter space to be more effectively explored. The whole process is iterated for many generations where the candidate solutions can be seen to evolve and, hopefully, converge towards a single solution. The use of natural evolution method for the optimization of control system has been of interest for the researchers since a long time. Fig. 9, illustrate the GA flowchart.

Ready to use implementation of GA is available in the MATLAB's optimization toolbox.

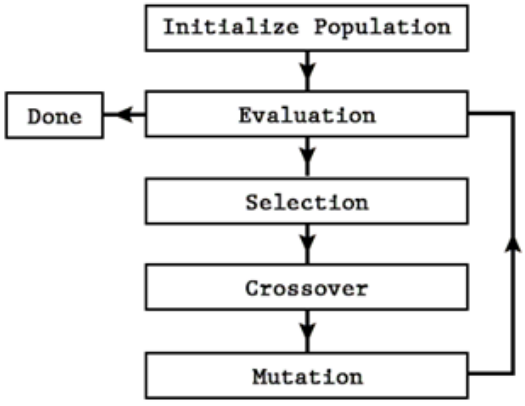

Fig. 9. GA flowchart.

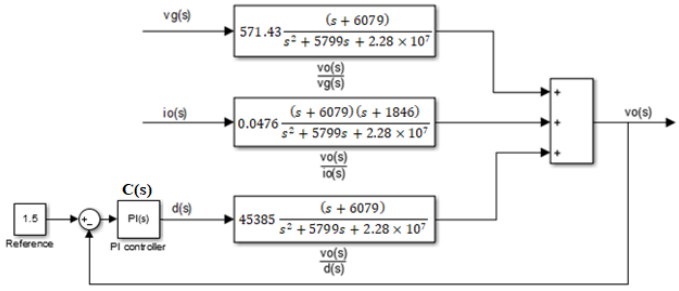

Fig. 10. Block diagram of the system with PI controller.

C. Suggested Method

The open loop dynamical model of the studied buck converter is shown in Fig. 7. Block diagram of closed loop voltage mode control of the converter is shown in Fig. 10. The controller is PI (Proportional Integral) since it is good enough for most of applications.

The PI controller must stabilize the loop. According to the Routh-Hurwitz stability test, following inequality must be satisfied in order to stabilize the loop.

$$(a.d + b.c)k_p + (a.c - b)k_i + c.d + a^2.k_p k_i + a.b.{k_p}^2 > 0 \quad (15)$$

where, $a = 45385, b = 45385 \times 6079 = 275895415,\ c = 5799, d = 2.28 \times 10^7$. $k_p > 0$ and $k_i > 0$ are unknown proportional gain and integral gain, respectively.

According to the Fig. 10, the closed loop output impedance is:

$$Z_{CL} = \frac{\tilde{v}_o(s)}{\tilde{\imath}_o(s)} \times \frac{1}{1 + C(s).\frac{\tilde{v}_o(s)}{\tilde{d}(s)}} \quad (16)$$

or,

$$Z_{CL} = 0.0476 \frac{(s + 6079)(s + 1846)}{s^2 + 5799s + 2.28 \times 10^7} \times \frac{1}{1 + (k_p + \frac{k_i}{s}).45385 \frac{(s + 6079)}{s^2 + 5799s + 2.28 \times 10^7}} \quad (17)$$

Equation (17) has two unknowns: k_p and k_i. We want to solve the following optimization problem:

$$min\ \|Z_{CL}\|_\infty \quad s.t.\ C(s)\ stabilize\ \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \quad (18)$$

Ideally Z_{CL} would be zero across the frequency bandwidth. However, since that would require an infinite loop gain, it is not practical for synthesis. The GA can be used to solve this optimization problem. GA changes the k_p and k_i values until the minimum is obtained. After running the GA, $k_p = 3.733$ and $k_i = 1.108 \times 10^4$ and $\min \|Z_{CL}\|_\infty = 0.476\ \Omega$.

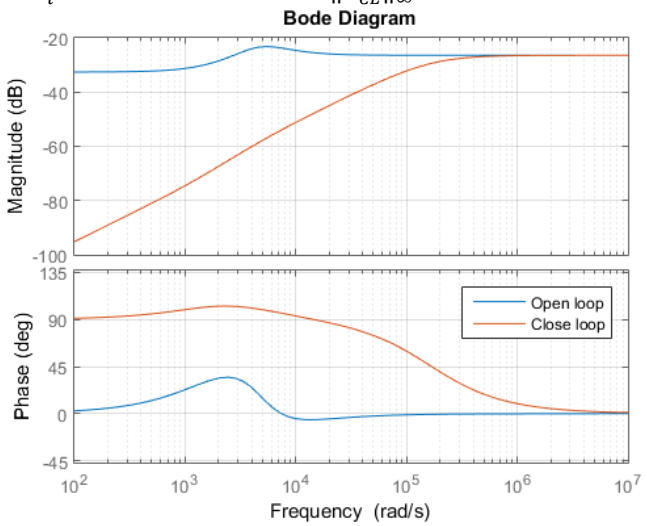

Fig. 11. Comparison between open loop output impedance and closed loop output impedance.

Fig. 11 compares the closed loop output impedance (Equation (17) with $k_p = 3.733$ and $k_i = 1.108 \times 10^4$) and open loop output impedance (Equation (7)). Closed loop output impedance decreased considerably in the low frequency range of the graph. Reduction of output impedance means a smaller voltage drop for larger currents. Such a property is highly desired in low voltage high current applications.

IV. SIMULATION RESULTS

Designed PI controller is tested in the Simulink environment. Simulation diagram is shown in Fig. 12. In the first test scenario, reference (Fig. 10) changes from 1.5 V to 3 V at t= 25 ms. Simulation result is shown in Figs. 13 and 14. Simulation result shows that the designed controller is able to follow the reference signal with zero steady state error. This is expected since the controller contains an integrator term.

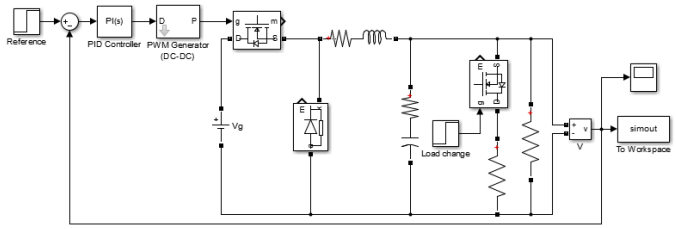

Fig. 12. Simulation diagram of the system.

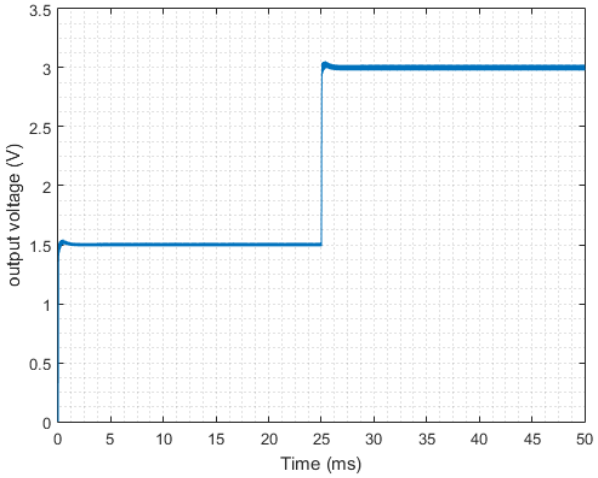

Fig. 13. Effect of change in reference.

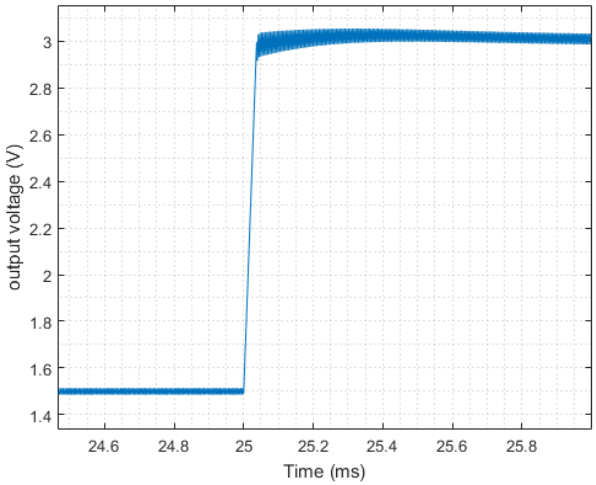

Fig. 14. Close-up Fig. 13 around t= 25 ms.

In the second scenario load current changes from 0.5 A to 5 A at t=25 ms. Simulation result is shown in Figs. 15 and 16. Simulation result shows that the controller is able to keep tracking the reference voltage even when the load changes. According to Fig. 16, maximum deviation for change of output current from 0.5 A to 5 A is 1.5-1.4=0.1 V. In other words, change of 900% in output current generates change of 6.66% in output voltage. Such a small change in output voltage shows that the designed controller decreased the output impedance considerably.

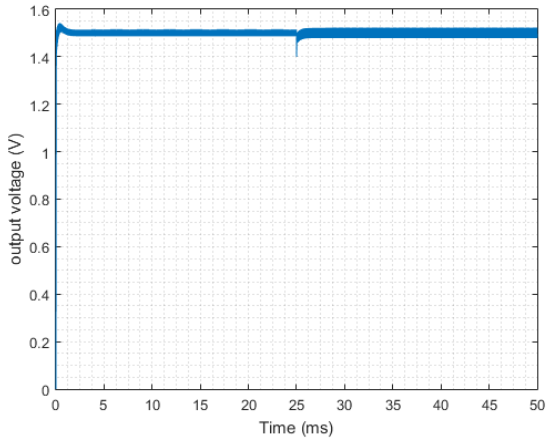

Fig. 15. Effect of change in output load.

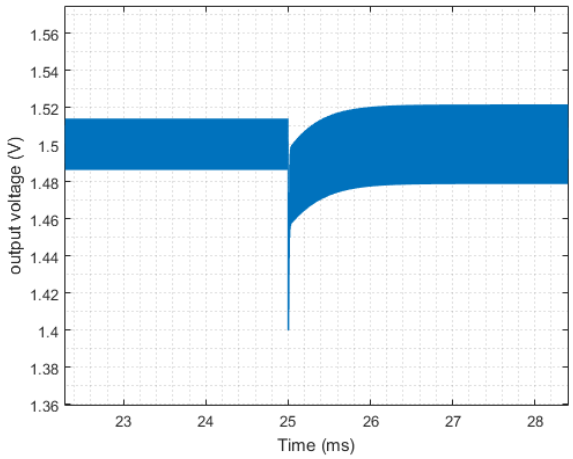

Fig. 16. Close-up Fig. 15 around t= 25 ms.

V. CONCLUSIONS

A technique to reduce the output impedance in the PWM buck converters with voltage-mode control is studied in this paper. Proposed technique used the H_∞ infinity norm to convert the impedance reduction problem into an optimization problem and use genetic algorithm to solve the obtained optimization problem. Suggested technique is cheaper in comparison to the classical solution of using the capacitors with lower ESR. Because in the suggested technique, there is no need to use any expensive low ESR capacitor and reduction of output impedance is done by good selection of controller parameters. Suggested technique is tested with the aid of Simulink simulations. According to the simulation results, the output impedance of converter decreased considerably in the low frequency region. Such a decrease is very desired for low

voltage high current loads like computer CPU's. Suggested method can be applied to other types of converters as well.

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