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Al-nSi SCHOTTKY DİYODLARININ İDEAL OLMAYAN I-V, C-V KARAKTERİSTİKLERİ VE ARAYÜZEY HALLERİNİN ENERJİ DAĞILIMI

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ÖZET

Metal ile yarı iletken arasında bir tabii (yerli) oksit tabakasının varlığını gözönüne alarak, Al-nSi Schottky diyodların ideal olmayan I-V ve C-V karakteristiklerini yorumladık. Doğru beslem ln [I/[1-exp (-qV/kT)]]-V ve dV/d(lnI)- Igrafiklerinden idealite faktörünün değerleri 1,48 ve 1,74 olarak elde edildi. Benzer olarak, engel yüksekliği için 0,54 eV'luk bir değer doğru beslem H(I)-I grafiğinden hesaplandı. Schottky diyodun seri direncinin doğru beslem I-V karakteristiklerinden çıkarılan Cheung'un fonksiyonları yardımıyla 1280-1510 Ω olduğu görüldü. C^{-2}-V grafiğinde aşağı doğru bükülen bir eğri gözlendi. Bu, arayüzey tabakası ve arayüzey hallerinin varlığına bağlandı. Bu ideal olmayan C^{-2}-V grafiği, lineer olan $(C-C_0)^{-2}$-V grafiğine dönüştürüldü, burada C_0, "ilave sığa" olarak adlandırılır ve $C-(V_d+V)^{-1/2}$ grafiğinin düşey eksen kesişiminden elde edilir. $(C-C_0)^{2}$-V grafiğinden engel yüksekliği 0,62 eV olarak hesaplandı. Ayrıca, arayüzey hallerinin yarı iletkenle dengede olduğu farzedildi. Arayüzey hal yoğunluğunun iletkenlik bandının tabanına doğru exponansiyel olarak arttığı görüldü ve onların enerji dağılımının daha önce yayınlanan sonuçlarla uyum içinde olduğu gözlendi.

NONIDEAL I-V, C-V CHARACTERISTICS and ENERGY DISTRIBUTION of INTERFACE STATES of Al-nSi SCHOTTKY DIODES

SUMMARY

We have interpreted non-ideal I-V and C-V characterisics of the Al-nSi Schottky diode by considering the presence of a native interfacial layer and interface states between metal and semiconductor. The values of 1.48 and 1.74 for the ideality factor was obtained from the forward bias ln[I / [1-exp(-qV/ kT)]] vs V plot and the forward bias dV/d(lnI) vs I plot, respectively. Likewise, a value of 0.54 eV for the barrier height was computed from the intercept of H(I)-I plot with vertical axis. The series resistance of the Schottky diode was also obtained from Cheung's functions derived from the forward characteristics. A downward curvature which is ascribed to the effects of the interfacial layer and the interface states was observed in the C^{-2} vs V plot. This non-ideal C^{-2} vs V plot was transformed into the linear $(C-C_0)^{-2}$ vs V plot by determining the "excess capacitance" C_0 which is the intercept of C vs $(V+V_d)^{-1/2}$ plot. The barrier height determined from the $(C-C_0)^{-2}$ -V plot was 0.62 eV. In addition, it was supposed that the interface states equilibrate with semiconductor, and their density was seen to have a slow exponential increase towards bottom of conduction band in the energy distribution plot and their energy distribution was observed to be in agreement with previous results.

1. INTRODUCTION

The Schottky diode is one of the most important semiconductor devices. According to Schottky model the barrier height is very dependent on the metal work function[1], but according to Bardeen's model, it is also dependent on the interface states which are continuously distributed in energy within the forbidden gap of semiconductor[2]. Under conditions of Schottky barrier formation or during surface preparation and metal evaporation , one essentially accepts that semiconductor surface is covered ordinarily with a thin layer of native oxide , and thus between the semiconductor and the thin oxide layer, the presence of interface states is expected with a high state density in forbidden energy gap[3-10] . Thereby , these interfacial layer properties such as the interfacial layer's thickness and the interface states play an important role on the electrical characteristics of Schottky diode and they cause results to extract more different from those expected . In a such case , the structure of Schottky barrier with an interfacial layer is the same as that of MIS diode[3-14] .

The first discussions and evaluations related to the presence of the interfacial layer and the interface states were by Cowley and Sze[5] and Turner and Rhoderick[6] , they showed that the barrier height depended on the characteristic parameters of the interfacial layer rather than work function of metal . Then , some workers determined the energy distribution and density of interface states from the I-V and C-V characteristics of Schottky diodes by following the previous works and making special assumptions on the interface states[4,8-17] . Furthermore , many detailed investigations were also carried out to interpret the interface state density and its energy distribution by means of photoemission spectroscopy[18,19] , admittance (Schottky capacitance) spectroscopy [12,20-26] , deep level transient spectroscopy(DLTS)[27] and electron paramagnetic resonance(EPR)[28] .

In this paper , we have discussed our results by assuming the presence of an interfacial layer, which introduces interface states, due to the nonideal I-V and C^2-V characteristics , and in addition to that , we have determined the energy distribution of the interface states in the band gap by using the forward bias I-V characteristics of our samples.

2 . THEORETICAL BACKGROUND

The basic current equation for Schottky barrier diode is given by thermionic theory[4,29]

$$I = AA^{*}T^{2}\exp(-q\Phi_{b} / kT)[\exp(qV / kT) - 1] \qquad (1)$$

where A is diode area , A^* is the effective Richardson constant , T is absolute temperature , k is Boltzmann constant, Φ_b is barrier height . However , the barrier height , Φ_b, is strongly dependent on the electric field in depletion region , and thus also on the applied bias . Therefore, the barrier height is reduced as a result of image force lowering and interfacial layer, in such a case the effective barrier height Φ_e is used in place of Φ_b and is defined as[4,29]

$$\Phi_e = \Phi_{bn,o} - \Delta\Phi_{bn,o} + \beta V \qquad (2.a)$$

or

$$\Phi_e = \Phi_{bn} + \beta V \qquad (2.b)$$

where Φ_{bn} is $\Phi_{bn,o} - \Delta\Phi_{bn,o}$, $\Phi_{bn,o}$ is the barrier height (at thermal equilibrium) at zero bias , $\Delta\Phi_{bn,o}$ is the barrier lowering due to image force at zero bias and β is the voltage coefficient of the effective barrier and is given by $\beta = \partial\Phi_e/\partial V$ = the change in the effective barrier with bias voltage and is assumed to be a positive constant . The current now becomes

$$I = AA^{*}T^{2}\exp[-q(\Phi_{bn} + \beta V)/ kT][\exp(qV/ kT) - 1] ,$$

$$= I_o\exp(-\beta qV/ kT)[\exp(qV/ kT) - 1] \qquad (3)$$

where

$$I_o = AA^{*}T^{2}\exp(-q\Phi_{bn}/ kT). \qquad (4)$$

Taking $1/n = 1 - \beta = 1 - (\partial\Phi_e/\partial V)$[4,14]. Eg.(3) can be expressed in the form

$$I = I_o\exp(qV/ nkT)[1 - \exp(-qV / kT)] , \qquad (5)$$

where n is the well known ideality factor , and is a measure of confirmity of the diode. n has usually value greater than unity and can be obtained from the slope of straight line part of the forward bias $\ln\{I/[1-\exp(-qV/ kT)]\}$ against V plot.

In addition , for the interface states in uquilibrium with the semiconductor , ideality factor n is equal to [7]

$$n = 1 + \delta/\varepsilon_i[(\varepsilon_s/w) + qN_s], \qquad (6)$$

where w is the depletion region width and N_s is the interface state density in equilibrium with the semiconductor , ε_s is permitivity of the semiconductor, ε_i is permitivity of the interfacial layer and δ its tihckness.

Furthermore , the energy of the interface satetes E_s relative to the bottom of conduction band, E_c, at the surface of semiconductor is given by

$$E_c - E_s = q\Phi_{bn} - qV \qquad (7)$$

The small-signal ac capacitance of the ideal Schottky diode(without any interfacial layer) as function of applied dc voltage is given by the relationship[30]

$$C = [q\varepsilon_s N_d / 2(V_d + V)]^{1/2}, \qquad (8)$$

where N_d is the donor density in the semiconductor, V_d is the diffusion potential. As can be seen from Eq.(8), C is proportional to $(V_d + V)^{-1/2}$ and the C vs $(V_d+V)^{-1/2}$ plot gives a straight line which goes through origin . However, when an interfacial layer and interface states with high density are present between the metal and semiconductor, C-V characteristics become functions of interfacial layer properties[3-10]. In such cases, a non-linearity or curvature arises in the reverse-bias region of C^{-2} vs V , and the straight line of C vs $(Vd + V)^{-1/2}$ plot does not now go through origin , therefore, the intercept of the plot gives an "excess capacitance, C_o , which is used to correct C-V characteristics[31-33] .

3.EXPERIMENT and EXPERIMENTAL RESULTS

The n-type (111) Si with a doping concentrations of about 2.98×10^{12} cm^{-3} (high resistivity) used in this study was obtained from Wacker-Chemitronic . Samples were mechanically polished and chemically etched , then ohmic contacts to one face of samples were made by the evaporation and the alloying of Au-Sb. Schottky contacts were made the other face by evaporation of Al . The evaporation processes were carried out at a pressure of 10^{-5} Torr . The area of Schottky contacts were about 0.78 mm^2.

Fig.1 shows the semilog I-V characteristics measured at 300 K of the Al-nSi Schottky diode. The curve (a) shown in Fig1 shows the forward bias ln{I/[1-exp(-qV/ kT)]} vs V plot . The value of ideality factor n calculated from the slope of the linear part of the plot is about 1.46 . Furthermore , the barrier height as well as other Schottky diode parameters , as the ideality factor n and the series resistance , were also calculated using a method developed by Cheung for the forweard bias characteristics[34] . In this calculation , the following functions of Cheung are used :

$$dV/d(\ln I) = R I + (kT/ q)n \qquad (9)$$

and

$$H(I) = V - n(kT/ q)\ln(I/A\ A^{*}T^{2}) \qquad (10.a)$$

$$H(I) = R I + n\Phi_{bn} \qquad (10.b)$$

As can be seen from Eqs.(9) and (10.b) , dV/d(lnI) vs I and H(I) vs I plots should give straight lines. Those plots drawn are given in Fig.2 . The values of the series resistance of the Al-nSi Schottky diode calculated from the slope of straight lines and the values of n and Φ_{bn}(=0.54 eV) obtained from their intercepts on the y-axis are given on Fig.2 .

The downward curvature in the I-V characteristics at high forward bias values is attributed to the series resistance and a continuum of the interface states [12,35] .The energy distribution of the interface states can be deduced from the downward curvature region without considering the effect of the series resistance (as will be discussed later). The forward I-V measurements (the experimental values of I for all the values of V) are well fitted to the equation

$$I/[1-\exp(-qV/ kT)] = 1.4 \times 10^{-8} \exp(qV/ nkT) \qquad (11)$$

with the ideality factor n values shown in Table 1 and Fig.3. Substituting in the Equ.(6) the values of n in Table 1 (using δ=20 A°[7], $\varepsilon_s=11.8\varepsilon_o$, $\varepsilon_i=4\varepsilon_o$[29]) and w=8.37 μm from C-V measurements (Fig.6) , the values of N_s as a function of applied voltage V were obtained and are given in Table 1. The results of voltage dependence of the N_s was converted to a function of E_s using Eq.(7). N_s vs E_c-E_s is also shown in Table 1 and Fig.4.

The C-V characteristics of the Al-nSi Schottky diode measured at 100 kHz, 300K, are shown in Fig.5 and Fig.6. The typical C^{-2} vs V characteristics (reverse bias) is shown by the solid circles in Fig.6. As seen from Fig.6, a downward curvature was observed in the 0-0.5 V region of the C^{-2}-V plot . This case can be due to presence of intercafe states, as will be discussed later [4,12,31,32], so " the excess capacitance ", C_0, appears to correct the C^{-2} -V characteristics. The values of C_0 can be determined by extrapolation of C vs $(V_d + V)^{-1/2}$ plot (Fig.5) . As seen from Fig.5 , C_0 was obtained as 9.97 pF. Fig.6 shows the non-linear C^{-2}-V plot and essentially the linear $(C-C_0)^{-2}$-V plot . Thus the non-linear C^{-2} -V plot was transformed into the linear $(C-C_0)^{-2}$ -V plot by determining the excess capacitance. As can be seen from Fig.6 , the extrapolated voltage intercept of $(C-C_0)^{-2}$ -V plot with V axis ,V_0, was found as 0.36 V . The donor concentration was also obtained as 5.6×10^{12} cm^{-3} from the slope of the plot . The values of the intercept voltage and the donor concetration will be corrected for the effect of interfacial layer in discussion section.

4. DISCUSSION

The value of n calculated from the linear region of the forward bias I-V characteristics was larger than one , this indicates that the Al-nSi Schottky diode does not obey ideal Schottky theory . In addition , a downward curvature observed at low reverse bias region of C^{-2} -V characteristics also indicates the deviation from ideality. Possible causes of deviaton from the ideal I-V characteristics can be the presence of the interfacial layer properties , the effect of the image force and the existance the recombination of electrons and holes in depletion region , but the last two effects are expected to be small[7,29,36]. Thus , it can be said that the most considerable cause of departures from ideal behavior is due to the presence of the interface sates and an interfacial layer[3-20,31-36] . The electrical measurements can be used to obtain interface parameters because the interfacial layer properties affect the electrical characteristics of the Schottky diodes. Therefore , the Al-nSi Schottky diode can be reported as an MIS diode . Likewise , non-ideality of C^{-2} -V characteristics of Al-nSi Schottky diode can also be attributed to the presence of the interface states , interface layer and, some deep level impurities which do not consider in this work .

The curves (a),(b) and (c) shown in Fig.1 show the semilog forward bias I-V , reverse bias lnI-V and reverse bias lnI-$V_r^{1/4}$ plots of Al-nSi diode, respectively . As can be seen from the Fig.1, the reverse bias saturation current I_r does not agree with that of forward bias, this confirms an additional current component of reverse

bias. This additional current can be attributed the voltage developed across the interfacial layer which give stronger voltage dependence than that predicted to image force lowering . It can breifly said that the presence of the interfacial layer in diodes causes the barrier height to decrease and the magnitude of the reverse current to increase with increasing reverse bias as a result of the increasing voltage drop across the interfacial layer [the curve (b) shown in Fig.1]. Therefore , in the reverse bias of the I-V plot , complete saturation has not been observed. Thereby , as also shown in Fig.1, to obtain the barrier height from the reverse bias lnI-V[the curve (b) shown in Fig.1]) and $\ln I$-$V_r^{1/4}$ plot[the curve (c) shown in Fig.1] it gives error conclusions .

The values of the ideality factor n was obtained as 1.46 from the straight line part of the forward bias $\ln(I/[1-\exp(-qV/kT)])$ vs V plot (Fig.1.a) and calculated as 1.74 from the plots of Cheung functions (Fig.2) obtained from the downward curvature part of the forward bias I-V plot[the curve (a) shown in Fig.1]. The difference between those two values of n can be explained as the fact that the first one only is under effect of the interfacial properties and the second one is under effect of both the interfacial properties and the series resistance because there also are both effects at the downward curvature region[4,12,33-37] . The same interpretation is also valid for the value of 0.54 eV of the barrier height Φ_{bn} deduced from Cheung's functions(Fig.2).

As seen in Fig.4 , a slow exponential increase of interface states exists from the midgap towards the bottom of cunduction band. The presence of such a high density of the interface states could be related to the existence of a thin native oxide layer on Si. Therefore , we believe that the presence of this thin native oxide(the interface layer) on Si causes a cosiderable amount of interface states especially in the energy range above the midgap . This is because of the growth of this oxide layer after etching and during thermal treatment for formation of ohmic contact . This is an expectionally high density of the states for an etched surface[7,20,29] . The energy distribution of the interface states we observed is very similar to the those reported by different authors[8,12,20,38-41] .

Moreover , the nonideal C^{-2}-V plot showing curvature concave downward due to effects mentioned above was transformed into linear $(C-C_0)^{-2}$-V plot(Fig.6) by determining the "excess capacitance"(C_0) which is intercept of a C-$(V+V_d)^{-1/2}$ plot .

In making this transformation (the reverse bias) it has been assumed that the density of interface states N_s remains constant as reverse bias voltage V changes[4,29,37,42]. For the stuation where the interface state capacitance was accepted as "excess capacitance", C^{-2} vs V plot is clearly not a straight line even if the interface states density is assumed constant and its slope is always less(in magnitude) than that of an ideal Schottky diode. Again, this stuation could lead bulk doping density computed from the slope of C^{-2}-V plot to deduce higher than that expected[42]. The capacitance of interfacial layer is not taken into account because it is very large for thin layers[12,31,42] . The intercept voltage V_o(=0.36V) and doping concentration N_d(=5.56x10^{12} cm^{-3}) are corrected by means of a factor of $(1+\alpha)^{-1}$(the case 2 in ref.42) for the case of the"excess capacitance", where the quantity α is given by $qN_s\delta/\varepsilon_i$[42]. Using the average value of N_s= 8.62x10^{16}/m^2-eV, it was obtained a value of 0.78 for α. Thus, the correct values of the diffusion potential V_d and doping concenration were determined as 0.21 V(thus the barrier height=0.62 eV) and 3.15x10^{12} cm^{-3} , respectively . The difference between the value we obtained and that given by the manufacturer may be due to the presence of an additional oxide-like interfacial layer, as aluminium oxide for Al contact[33] , and change in the effective area of the Schottky contacts .

Our discussion and calculations have been based on the assumption that an interfacial oxide layer which is caused by surface preparation , metal evaporation or post-deposition thermal treatment exists between semiconductor and metal, and that the interface states equilibrate with the semiconductor .

In summary , we studied to interpret non-ideal I-V and C-V characteristics which are due to undesirable causes and we attributed the departures from ideal Schottky theory to the interfacial layer properties . We compared with the results of different authors by extracting the energy distribution of the interface states from the non-ideal forward bias I-V characteristics of the Al-nSi Schottky diode and it was seen that our results are in agreement with the other results .

Table1. Energy distribution of the interface state density obtained from the forward bias I-V characteristics of the Al-nSi Schottky diode at 300K.

V(Volt)	n	E_c-E_s	$N_s(10^{16}\ m^{-2}eV^{-1})$
0.200	1.46	0.420	5.08
0.225	1.50	0.395	5.52
0.250	1.56	0.370	6.19
0.275	1.60	0.345	6.63
0.300	1.65	0.320	7.18
0.325	1.71	0.295	7.84
0.350	1.78	0.270	8.62
0.375	1.84	0.245	9.28
0.400	1.90	0.220	9.95
0.425	1.98	0.195	10.8
0.450	2.04	0.170	11.4
0.475	2.11	0.145	12.2
0.500	2.20	0.120	13.2

Figure Captions

Figure1. The Current-Voltage characteristics of the Al-nSi Schottky diode:
(a)-The forward bias $\ln\{I/[1-\exp(-qV/kT)]\}$ vs V ,
(b)-The reverse bias lnI vs V,
(c)-The reverse bias lnI vs $V_r^{1/4}$,

Figure 2. dV/d(lnI) vs I and H(I) vs I plots of the Al-nSi Schottky diode.

Figure 3. Bias dependence of n obtained from the downward curvature region of the forward bias I-V characteristics .

Figure 4. Density of the interface states N_S as a function of E_C-E_S .

Figure 5. Determination of the values of C_0 by extrapolation of C vs $(V_d+V)^{-1/2}$

Figure 6. Comparison of the C^{-2} vs V plot and the linearized $(C-C_0)^{-2}$ vs V plot of the Al-nSi Schottky diode at 100 kHz , 300K.

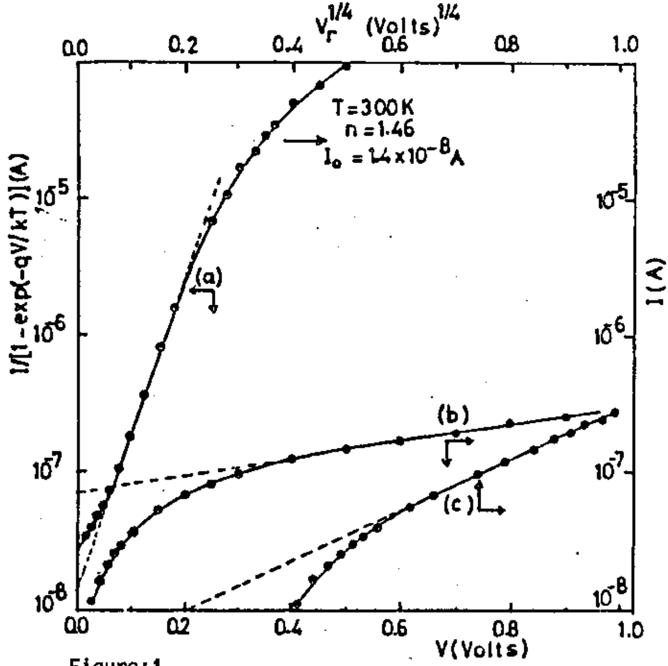


Figure:1

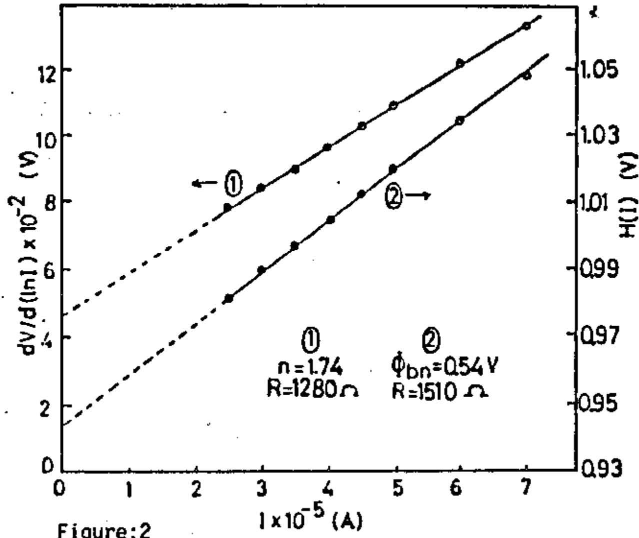
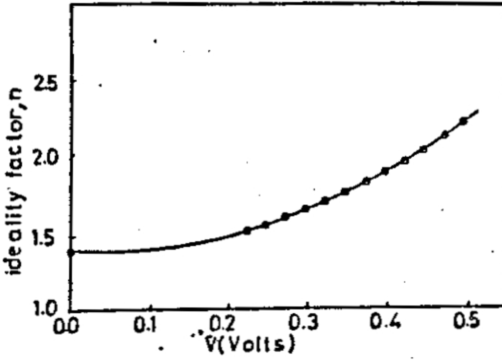


Figure:2



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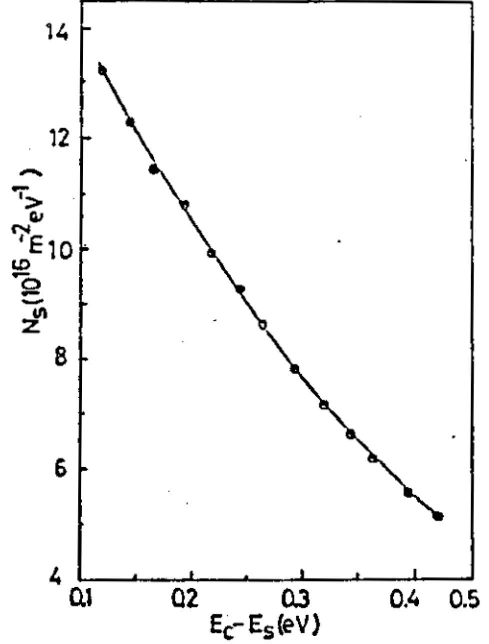

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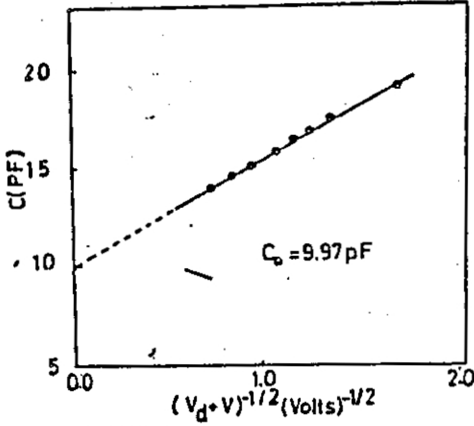

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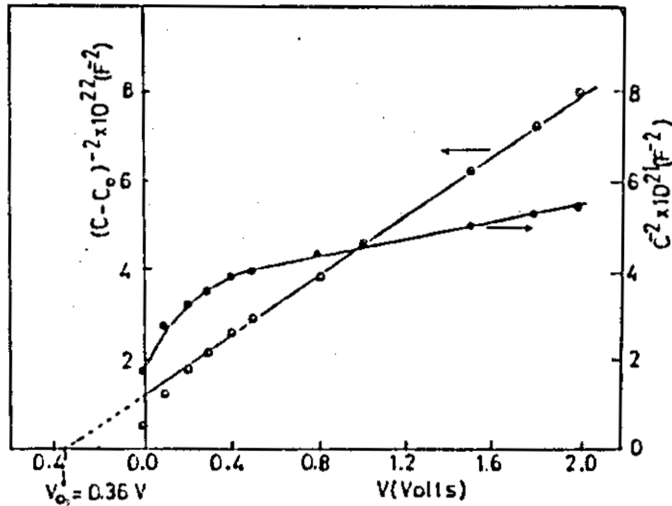

Figure: 6

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