GENERALIZED CURRENT-MODE CONFIGURATION WITH LOW INPUT AND HIGH OUTPUT IMPEDANCE

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Abstract: *In this paper, a new generalized current-mode configuration for the realization of first-order all-pass, second-order all-pass and notch filter is proposed. The presented configuration uses single multi-output dual-X second generation current conveyor and two impedances. The configuration uses two grounded resistors and one grounded capacitor for the realization of first-order all-pass filter, and two resistors and two grounded capacitors for realizing second-order all-pass/notch filter. Furthermore, a band pass filter can also be realized by making slight modifications to the notch filter. In addition, a current-mode quadrature oscillator as an application of the proposed circuit of all-pass filter is also given. All the proposed circuits enjoy the feature of low input and high output impedance. Low input and high output impedance of the proposed configuration enables cascadability to all the circuits without additional buffers. The theoretical results are validated with PSPICE simulations using TSMC 0.18µm CMOS process parameters.*
Keywords: *Current-mode, all-pass filter, dual-X second generation current conveyor, oscillator.*

1. Introduction

The current-mode (CM) circuits have received significant attention due to their particular advantages such as higher bandwidth capability, greater linearity, wider dynamic range, less circuit complexity, higher operating speed and low power consumption compared with voltage-mode (VM) circuits [1]. Current-mode filter circuits with low input and high output impedance features at input and output terminals respectively are used in interfacing and cascading to implement simpler and cost effective higher order filters [2]. Moreover, circuits with grounded capacitors are easy to integrate and benefitted with reduced parasitic effect [3]. All-pass (AP) filters are widely used in analogue signal processing in order to correct the phase of an electrical signal while keeping its amplitude constant over a frequency range of interest [4]. On the other hand notch filters are widely used to reject unwanted noise and allow the useful signals to pass. The topic has been researched for decades now but with a renewed interest and attention recently, resulting in more effective realizations. Some of the available current-mode (CM) all-pass/notch filters have the isolated feature(s) of single active element, grounded capacitors, low-input and/or high-output impedance [2, 5-24, 30-32]. The first order CM AP filter circuits reported in [5] employ single second generation current conveyor (CCII) and four passive components. The CM AP filter circuit reported in [6] employs single four terminal floating nullor (FTFN) and three passive components. In [7], a FTFN based generalized filter configuration is presented which utilizes six passive components to realize second order all-pass/notch filter. A single CCII or differential voltage current conveyor (DVCC) based CM filter circuits of [8, 9, 13, 24] can provide high output impedance however it employs a floating capacitor. The first order CM AP filter circuits reported in [10, 11] are canonical in structure but uses a floating capacitor. In [12], a single current differencing buffered amplifier(CDBA) based notch filter is presented employing four passive components. The circuit presented in [14] uses two current conveyors to realize a first order CM AP filter function with high output impedance. The modified current conveyor (MCC) based CM AP filter circuit employing one MCC and two passive components reported in [15] provides high output impedance. Moreover, this circuit [5-15] does not possess the low input impedance feature. The CM biquad filter circuit presented in [16] employs single dual output current differencing transconductance amplifier (DO-CDTA) and

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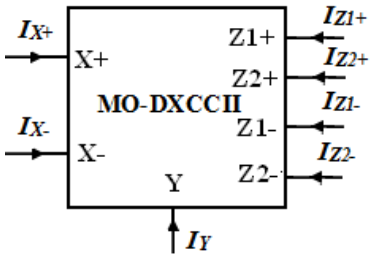
four passive components. However this circuit does not possess low input and high output impedance. Single dual-X second generation current conveyor (DX-CCII) based CM AP filters employing four passive components are reported in [17,18]. However, these circuits do not possess the advantage of low input impedance. The first-order CM AP filter circuit in [2] uses two current conveyors, one grounded capacitor and one grounded resistor with low input and high output impedance. Some most recent papers have presented CM circuit configuration with low input and high output impedance feature employing a single active element and two passive components but realize only a first order CM-AP filter [19, 20]. A CM biquad filter circuit reported in [21] employs a single voltage differencing transconductance amplifier(VDTA) and three passive components without low input impedance and high output impedance feature. But a careful survey reveals that none of the reported circuit realizes a first-order all-pass filter, second-order all-pass/notch filter using single active element, grounded capacitor(s), and providing low input and high output impedance feature simultaneously. To illustrate, a comparison between the proposed circuits and the previously reported current-mode filter circuits based on the above features are given in Table 1.

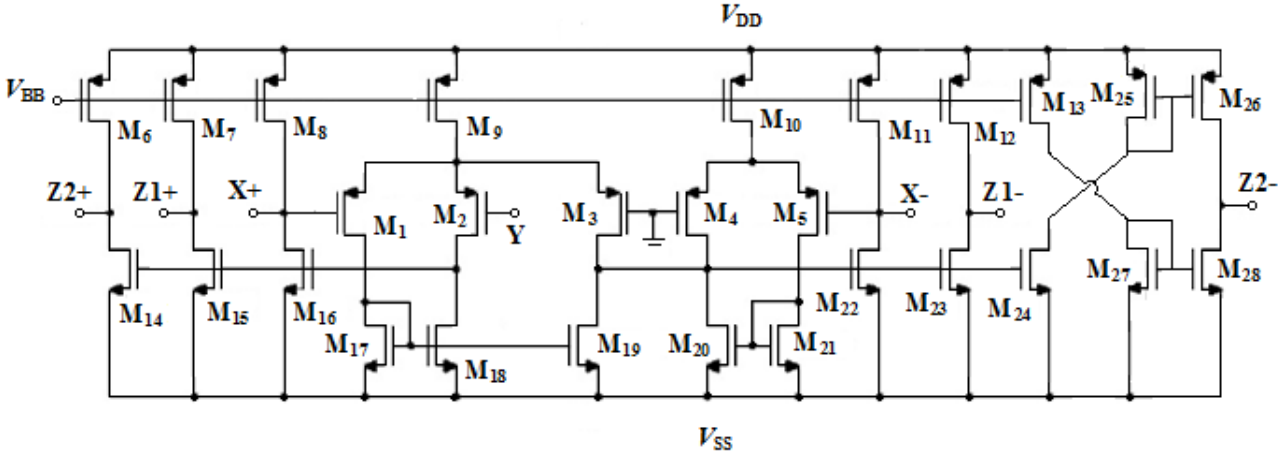
2. Proposed Circuits

The Symbol and CMOS implementation of MO-DXCCII is shown in Figure 1(a) and 1(b), respectively. Using standard notation, a MO-DXCCII is characterized by the following matrix equation

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \quad (1)$$



(a)



(b)

Figure 1. (a) Symbol of MO-DXCCII (b) CMOS Implementation of MO-DXCCII [25].

Table 1. Comparison of Various current-mode first-order APF, second-order APF and notch filter

Ref.	Active Element	Features						
		Single Active Element	First-order APF/No. of Passive Elements/Pole Frequency	Second-order APF/No. of Passive Elements/pole Frequency	Notch Filter/No. of Passive Elements/pole Frequency	All Grounded Capacitor	Low Input Impedance	High Output Impedance
2	DO-CCII	No	Yes/2/1.59MHz	No	No	Yes	Yes	Yes
5	CCII	Yes	Yes/4/1.59KHz	No	No	No	No	Yes
6	FTFN	Yes	Yes/3/1.59KHz	No	No	Yes	No	Yes
7	FTFN	Yes	No	Yes/6/NA	Yes/6/NA	No	No	Yes
8	CCII	Yes	Yes/2/NA	No	Yes/4/31.83KHz	No	No	Yes
9	CCII	Yes	Yes/4/1.59KHz	No	No	No	No	Yes
10	CCIII	Yes	Yes/2/100KHz	No	No	No	No	Yes
11	COA	Yes	Yes/2/1.59MHz	No	No	No	No	Yes
12	CDBA	Yes	No	No	Yes/4/79.6KHz	No	No	Yes
13	DVCC	Yes	Yes/3/1.06MHz	No	No	No	No	Yes
14	MO-CCII	No	Yes/2/358KHz	No	No	Yes	No	Yes
15	MCC	Yes	Yes/2/134KHz	No	No	Yes	No	Yes
16	DO-CDTA	Yes	No	Yes/4/NA	Yes/4/NA	Yes	No	No
17	DXCCII	Yes	Yes/4/1.59MHz	No	No	Yes	No	Yes
18	DX-MOCCII	Yes	Yes/4/1.59MHz	No	No	Yes	No	Yes
19	MO-DXCCII	Yes	Yes/2/6.36MHz	No	No	Yes	Yes	Yes
20	MO-DXCCII	Yes	Yes/2/1.59MHz	No	No	Yes	Yes	Yes
21	VDTA	Yes	No	Yes/3/NA	Yes/3/NA	Yes	No	No
22	DVCC	Yes	Yes/3/159KHz	No	No	Yes	No	Yes
23	CCIII	Yes	Yes/4/159KHz	No	No	No	No	Yes
24	DVCC	Yes	Yes/3/1.06MHz	No	No	No	No	Yes
Proposed work	MO-DXCCII	Yes	Yes/3/21.23MHz	Yes/4/11.26MHz	Yes/4/5.30MHz	Yes	Yes	Yes

Abbreviations: CCII: Second Generation Current Conveyor, FTFN: Four-Terminal Floating Nullor, CCIII: Third Generation Current Conveyor, CDBA: Current Differencing Buffered Amplifier, COA: Current Operational Amplifier , DVCC: Differential Voltage Current Conveyor , MO-CCII: Multi-Output Second Generation Current Conveyor, MCC: Modified Current Conveyor, DO-CCII: Dual Output Second Generation Current Conveyor, DXCCII: Dual-X Second Generation Current Conveyor, MO-DXCCII: Multi-Output Dual-X Second Generation Current Conveyor, DX-MOCCII: Dual-X Second Generation Multi-Output Current Conveyor, VDTA: Voltage Differencing Transconductance Amplifier, DO-CDTA: Dual Output Current Differencing Transconductance Amplifier, CDTA: Current Differencing Transconductance Amplifier, NA: Not Available

The proposed general configuration of a cascadable current-mode filter using a single MO-DXCCII and two impedances is shown in Figure 2. Routine analysis of the proposed circuit using (1) yields the following transfer function

$$\frac{I_{OUT}}{I_{IN}} = \frac{Z_1 - 2Z_2}{Z_1 - Z_2} \qquad (2)$$

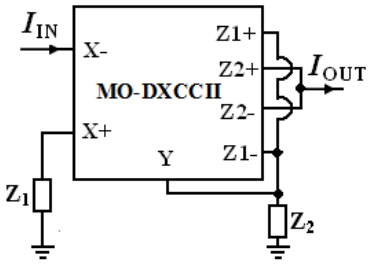
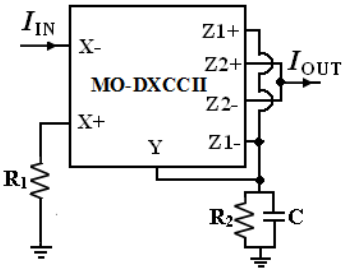
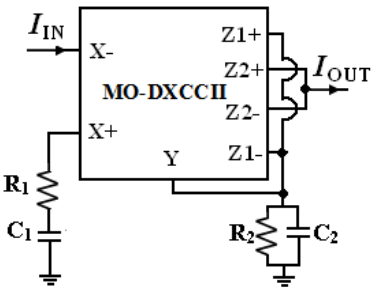


Figure 2. Proposed cascadable current-mode filter configuration.

The first-order and second-order filters are realized from Figure 2, with appropriate impedance selection and are listed in Table 2, along with their transfer functions. The circuits tabulated in Table 2 include first-order all-pass filter, second-order all-pass filter and notch filter. The circuit '1'of Table 2 realizes first order all-pass filter with single active element and three grounded passive components whereas the circuit '2'of Table 2 realizes second order all-pass filter and notch filter with single active element, and four passive components, which is an optimum component solution for an active RC second-order filter. The use of only grounded capacitors makes them suitable for integrated circuit (IC) fabrication. All the proposed circuits possess low input and high output impedance, which make them suitable for cascading.

Table 2. Proposed First-order and second-order filter circuits

Impedances/ Circuit number	Circuit diagram	Transfer function
$Z_1 = R_1$; $Z_2 = R_2/(1+sCR_2)$ Circuit '1'		$\frac{I_{OUT}}{I_{IN}} = \frac{sCR_2R_1 - (2R_2 - R_1)}{sCR_2R_1 + (R_1 - R_2)}$ For, $R_2 = R$, $R_1 = 1.5R_2 = 1.5R$ $\frac{I_{OUT}}{I_{IN}} = \frac{3sCR - 1}{3sCR + 1}$ (First-order all-pass filter)
$Z_1 = R_1 + 1/sC_1$; $Z_2 = R_2/(1+sC_2R_2)$ Circuit '2'		$\frac{I_{OUT}}{I_{IN}} = \frac{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - 2R_2C_1) + 1}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1) + 1}$ Second order all-pass filter **(a)** For, $R_1 = R$, $R_2 = 2R_1 = 2R$, $C_1 = C_2 = C$ $\frac{I_{OUT}}{I_{IN}} = \frac{2s^2R^2C^2 - sRC + 1}{2s^2R^2C^2 + sRC + 1}$ **(b)** For, $R_1 = R_2 = R$, $C_1 = C$, $C_1 = 2C_2 = 2C$ $\frac{I_{OUT}}{I_{IN}} = \frac{2s^2R^2C^2 - sRC + 1}{2s^2R^2C^2 + sRC + 1}$ Notch filter For $R_1 = R_2 = R$, $C_1 = C_2 = C$ $\frac{I_{OUT}}{I_{IN}} = \frac{s^2R^2C^2 + 1}{s^2R^2C^2 + sRC + 1}$

4. Non-ideal Analysis

Considering the non-idealities of MO-DXCCII into account, two parameters α and β are introduced. The port relationships of the terminal voltages and currents can be written as

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_1 & 0 & 0 \\ -\beta_2 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & \alpha_2 & 0 \\ 0 & 0 & \alpha_3 \\ 0 & 0 & -\alpha_4 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{3}$$

Here, α_1 and α_2 are the current transfer gains (deviate from unity by the current tracking errors) from X+ terminal to Z_{1+} and Z_{2+} terminals, α_3 and α_4 are the current transfer gains (deviate from unity by the current tracking errors) from X- terminal to Z_{1-} and Z_{2-} terminals, respectively, whereas β_1 and β_2 are the voltage transfer gain (deviate from unity by the voltage tracking errors) from input terminal Y to X+ and X- terminals, respectively. However, these transfer gains remain close to unity upto a very high frequency range (i.e. in GHz), the actual value depends upon the technology and the devices used in implementing the active element [29].

The circuit '1' of Table 2 is reanalyzed using (3). The modified transfer function is found as

$$\frac{I_{OUT}}{I_{IN}} = \frac{s - \left(\frac{R_2\beta_1(\alpha_1\alpha_4 + \alpha_2\alpha_3) - R_1\alpha_4}{CR_2R_1\alpha_4} \right)}{s + \left(\frac{R_1 - R_2\alpha_1\beta_1}{CR_2R_1} \right)} \tag{4}$$

From (4), the non-ideal pole frequency (ω_o) for the first order all-pass filter is calculated and given as

$$\omega_o = \frac{R_1 - R_2\alpha_1\beta_1}{CR_2R_1} \tag{5}$$

The active and passive sensitivities with respect to ω_o are

$$S_{R_1}^{\omega_o} = \frac{R_2\alpha_1\beta_1}{R_1 - R_2\alpha_1\beta_1}, S_{R_2}^{\omega_o} = \frac{R_1}{R_1 - R_2\alpha_1\beta_1}, S_C^{\omega_o} = -1,$$
$$S_{\alpha_1,\beta_1}^{\omega_o} = \frac{-R_2\alpha_1\beta_1}{R_1 - R_2\alpha_1\beta_1}, \; S_{\beta_2,\alpha_2,\alpha_3,\alpha_4}^{\omega_o} = 0 \tag{6}$$

The circuit '2' of Table 2 is reanalyzed using (3). The modified transfer function is found as

$$\frac{I_{OUT}}{I_{IN}} = \frac{s^2R_1R_2C_1C_2\alpha_4}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1) + 1} + \frac{s\left(R_1C_1\alpha_4 + R_2C_2\alpha_4 - R_2C_1\beta_1(\alpha_1\alpha_4 + \alpha_2\alpha_3)\right)}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1) + 1} + \frac{\alpha_4}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1) + 1} \tag{7}$$

From (7), the non-ideal pole frequency (ω_o) and quality factor (Q) for the second order filter is calculated and found as

$$\omega_o = \left(\frac{1}{C_1C_2R_1R_2} \right)^{\frac{1}{2}} \tag{8}$$

$$Q = \frac{\left(R_1R_2C_1C_2\right)^{\frac{1}{2}}}{(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1)} \tag{9}$$

The active and passive sensitivities of the second order filter with respect to ω_o and Q are as follows:

$$S_{R_1,R_2,C_1,C_2}^{\omega_o} = -\frac{1}{2}, S_{\beta_1,\beta_2,\alpha_1,\alpha_2,\alpha_3,\alpha_4}^{\omega_o} = 0,$$
$$S_{\beta_2,\alpha_2,\alpha_3,\alpha_4}^{\omega_o} = 0, S_{\alpha_1,\beta_1}^{Q} = \frac{R_2C_1\alpha_1\beta_1}{(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1)} \tag{10}$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = -\frac{1}{2}\frac{(R_1C_1 - R_2C_2 - R_2C_1\alpha_1\beta_1)}{(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1)},$$
$$S_{R_1}^{Q} = -S_{R_2}^{Q} = -\frac{1}{2}\frac{(R_1C_1 - R_2C_2 + R_2C_1\alpha_1\beta_1)}{(R_1C_1 + R_2C_2 - R_2C_1\alpha_1\beta_1)} \tag{11}$$

From (6), (10) and (11), it is evident that the sensitivities are less than or equal to unity in magnitude, thus ensuring good active and passive sensitivity performance.

5. Parasitic Effects

For a complete analysis of the proposed circuits, it is also important to include the study of various parasitics of the MO-DXCCII. These parasitics are the Y and Z terminals parasitic capacitances and the X-terminal resistances. For the circuits of Table 2, the Y, Z1+ and Z1- terminal capacitances (C_Y, C_{Z1+} and C_{Z1-}) appear in shunt with external C or C_2 and the X+ terminal resistance (R_{X+}) appears in series with external R_1, thus the modified transfer functions are as follows:

For Circuit '1':

$$\frac{I_{OUT}}{I_{IN}} = \frac{sC'R'R_2 + (R' - 2R_2)}{sC'R'R_2 + (R' - R_2)} \tag{12}$$

where $R' = R_1 + R_{X+}$ and $C' = C + C_Y + C_{Z1+} + C_{Z1-}$

For Circuit '2':

$$\frac{I_{OUT}}{I_{IN}} = \frac{s^2 R' R_2 C_1 C' + s(R' C_1 + R_2 C' - 2R_2 C_1) + 1}{s^2 R' R_2 C_1 C' + s(R' C_1 + R_2 C' - R_2 C_1) + 1} \quad (13)$$

where $R' = R_1 + R_{X+}$ and $C' = C_2 + C_Y + C_{Z1+} + C_{Z1-}$

From (12) and (13), most of the parasitic capacitances and resistances get absorbed with the external capacitor and resistor. Such absorption will cause slight deviations in the circuit parameters, which can be corrected by pre-distorting the passive element values to be used in the circuit. It may be further noted that the matching requirement (say for circuit '1'), as per Table 2 becomes $R' = 1.5R_2$, which is not really different from the ideal case (please refer to Circuit '1' of Table 2).

6. Simulation Results

The proposed circuits are simulated using the PSPICE simulation program. The MO-DXCCII [25] was realized as shown in Figure 1(b) and simulated using TSMC 0.18 μm process parameters as listed in Table 2. The supply voltages are ± 1.3 V and V_{BB} = -0.5 V.

6.1. First-Order All-Pass Filter

The proposed circuit '1' in Table 2 was designed with the passive elements C = 1 pF, R_1 = 1.5 kΩ, and R_2 = 1 kΩ. The theoretical pole frequency is found to be 21.23 MHz. The phase and gain response of the simulated circuit is shown in Figure 3, which shows a pole frequency of 21.07 MHz, thus close to the designed theoretical value. The proposed circuit provides phase shifting of 180^0 to 0^0 with frequency.

Table 2. TSMC 0.18 μm CMOS process parameters

NMOS: + LEVEL=7 VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3719233 +K1 = 0.5847845 K2 = 1.987508E-3 K3 = 1E-3 K3B = 3.846051 W0 = 1.00001E-7 NLX = 1.66359E-7 +DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 1.616073 DVT1 = 0.4422105 DVT2 = 0.0205098 +U0=276.4769418 UA=-1.287181E-9 UB=2.249816E-18 UC=5.695845E-11 VSAT=1.050018E5 A0=1.8727159 +AGS = 0.4223855 B0= -8.460618E-9 B1= -1E-7 KETA= -6.583564E-3 A1 = 0 A2 = 0.8925017 RDSW = 105 +PRWG =0.5 PRWB =-0.2 WR = 1 WINT = 0 LINT = 1.509138E-8 XL= 0 XW = -1E-8 DWG = -3.993667E-9 +DWB = 1.211844E-8 VOFF = -0.0926198 NFACTOR = 2.4037852 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 +CDSCB = 0 ETA0 = 2.64529E-3 ETAB = -1.113687E-5 DSUB = 0.0107822 PCLM = 0.7114924 +PDIBLC1 = 0.1861265 PDIBLC2 = 2.341517E-3 PDIBLCB = -0.1 DROUT = 0.708139 PSCBE1 = 8E10 +PSCBE2= 9.186022E-10 PVAG = 5.128699E-3 DELTA = 0.01 RSH = 6.5 MOBMOD = 1 PRT = 0 +UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1= 4.31E-9 UB1 = -7.61E-18 UC1= -5.6E-11 AT= 3.3E4 +WL= 0 WLN = 1 WW= 0 WWN = 1 WWL= 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 +XPART = 0.5 CGDO= 7.9E-10 CGSO = 7.9E-10 CGBO = 1E-12 CJ = 9.604799E-4 PB = 0.8 MJ= 0.3814692 +CJSW =2.48995E-10 PBSW= 0.8157576 MJSW = 0.1055989 CJSWG = 3.3E-10 PBSWG = 0.8157576 +MJSWG =0.1055989 CF= 0 PVTH0 = -4.358982E-4 PRDSW= -5 PK2= 2.550846E-4 WKETA = 1.466293E-3 +LKETA = -7.702306E-3 PU0 = 23.8250665 PUA = 1.058432E-10 PUB= 0 PVSAT = 1.294978E3 +PETA0= 1.003158E-4 PKETA = -3.857329E-3
PMOS: + LEVEL=7 VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3955237 +K1= 0.5694604 K2 = 0.0291529 K3 = 0.0997496 K3B = 13.9442535 W0 = 1.003165E-6 NLX = 9.979192E-8 +DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.5457988 DVT1 = 0.2640392 DVT2 = 0.1 U0=118.0169799 +UA=1.591918E-9 UB=1.129514E-21 UC=-1E-10 VSAT=1.545232E5 A0= 1.6956519 AGS = 0.3816925 +B0=4.590751E-7 B1=1.607941E-6 KETA=0.0142165 A1=0.4254052 A2= 0.3391698 RDSW = 168.2822665 +PRWG =0.5 PRWB=-0.5 WR=1 WINT=0 LINT=3.011839E-8 XL= 0 XW=-1E-8 DWG =-4.05222E-8 +DWB = 4.813652E-9 VOFF = -0.099839 NFACTOR = 1.8347784 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 +CDSCB=0 ETA0=0.201776 ETAB=-0.1409866 DSUB=1.0474138 PCLM=1.4195047 PDIBLC1=2.422412E-4 +PDIBLC2=0.022477 PDIBLCB=-1E-3 DROUT=1.228009E-3 PSCBE1=1.245755E10 PSCBE2= 3.598031E-9 +PVAG = 15.0414628 DELTA = 0.01 RSH = 7.5 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 +KT2=0.022 UA1=4.31E-9 UB1=-7.61E-18 UC1=-5.6E-11 AT= 3.3E4 WL= 0 WLN=1 WW=0 WWN=1 +WWL= 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO= 6.34E-10 +CGSO = 6.34E-10 CGBO = 1E-12 CJ = 1.177729E-3 PB = 0.8467926 MJ= 0.4063096 CJSW =2.417696E-10 +PBSW= 0.851762 MJSW = 0.3387253 CJSWG = 4.22E-10 PBSWG = 0.851762 MJSWG =0.3387253 CF= 0 +PVTH0=1.406461E-3 PRDSW=11.5261879 PK2=1.718699E-3 WKETA=0.0353107 LKETA= -1.277611E-3 +PU0=-1.4642384 PUA=-6.79895E-11 PUB=1E-21 PVSAT=50 PETA0=1.003152E-4 PKETA=-3.103298E-3

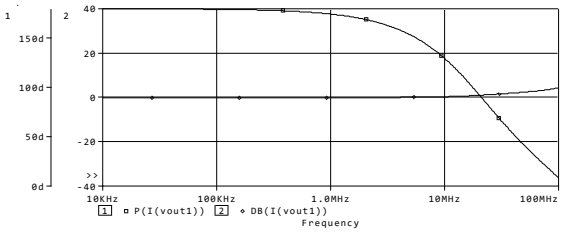


Figure 3. Simulated phase and gain responses of the first-order all-pass filter.

6.2 Second-Order All-Pass Filter

The circuit '2' of Table 2 is designed with the passive element values $C_1 = C_2 = 10$ pF, $R_1 = 1$ kΩ and $R_2 = 2$ kΩ to obtain all-pass filter with a pole frequency of 11.26 MHz. Gain and phase response of the simulated circuit is shown in Figure 4, which shows a pole frequency of 11.19 MHz. The simulation results are in agreement with the theoretical results.

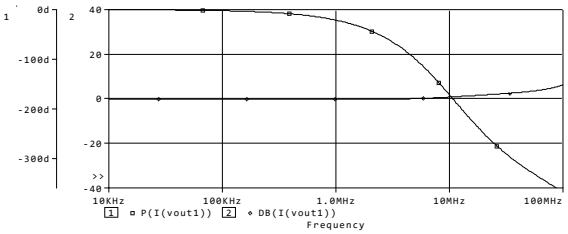


Figure 4. Simulated phase and gain responses of the second-order all-pass filter.

6.3. Notch Filter

The circuit '2' of Table 2 is designed with the passive element values $C_1 = C_2 = 30$ pF, $R_1 = 1$ kΩ and $R_2 = 1$ kΩ as for second order notch filter with a centre frequency of 5.30 MHz. The gain and phase responses for the notch filter are shown in Figure 5. The simulated notch frequency was found to be 5.23 MHz which agrees well with the theoretical analysis.

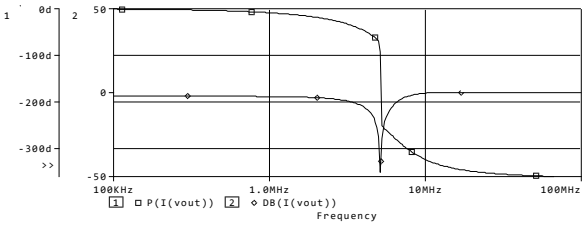


Figure 5. Simulated phase and gain responses of the notch filter.

7. Additional Band Pass Filter

It may be further noted that second-order band pass (BP) filter can also be obtained from the Circuit '2' of Table 2, by adding one extra Z3+ terminal i.e. $I_{Z3+} = I_{X+}$ as shown in Figure 6.

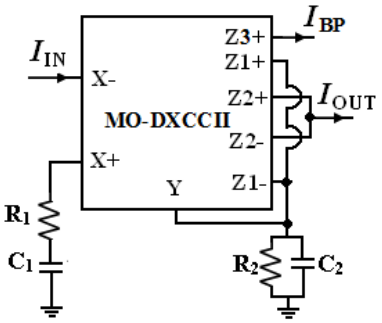


Figure 6. Additional band pass filter

Routine analysis of the Figure 6 using (1) yields the following transfer function

$$\frac{I_{BP}}{I_{IN}} = \frac{-sC_1R_2}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1) + 1} \qquad (14)$$

By selecting $R_2 = R_1 = R$, $C_1 = C_2 = C$ in (14) becomes

$$\frac{I_{BP}}{I_{IN}} = \frac{-sRC}{s^2R^2C^2 + sRC + 1} \qquad (15)$$

which is a second order band-pass function.

The circuit of Figure 6 is again designed with the same passive element values as for notch filter i.e $C_1 = C_2 = 30$ pF, $R_1 = 1$ kΩ and $R_2 = 1$ kΩ with a centre frequency of 5.30 MHz. The gain response for the band pass filter is shown in Figure 7. The simulated band pass frequency was found to be 5.27 MHz.

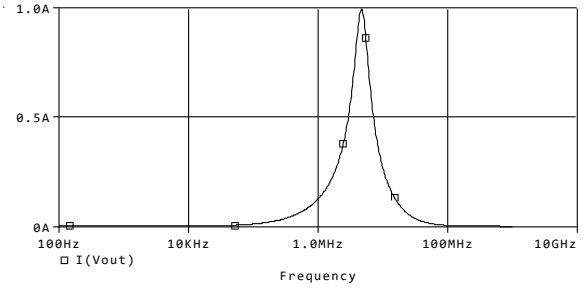


Figure 7. Gain response of the Band pass filter.

8. Current-Mode Quadrature Oscillator

As an application of the proposed circuit, a current-mode quadrature oscillator is further derived using the basic technique presented in [33-34]. The proposed circuit is realized using a second-order all-pass filter (Circuit-2) with a unity gain inverter as shown in Figure 8. It may be noted that a unity gain inverter is realized using MO-DXCCII with input and output connected at X- and I_{Z2-} terminals respectively. The analysis of the circuit yields the loop gain as

$$\frac{I_{OUT}}{I_{IN}}=(-1)\frac{s^2R_1R_2C_1C_2+s\left(R_1C_1+R_2C_2-2R_2C_1\right)+1}{s^2R_1R_2C_1C_2+s\left(R_1C_1+R_2C_2-R_2C_1\right)+1} \quad (16)$$

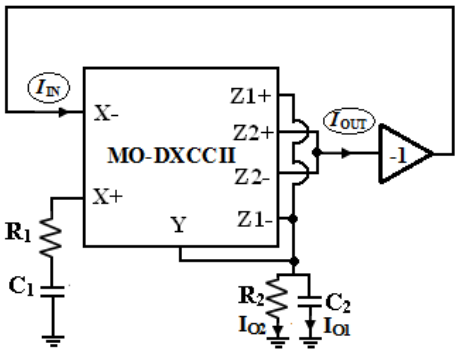


Figure 8. Current-mode quadrature oscillator

If the loop gain of the derived circuit is set to unity at $s = j\omega$, the circuit shown in Figure 8 can be set to provide two quadrature current outputs with condition of oscillation(CO) and frequency of oscillation(FO) as

$$\text{CO: } \left(R_1C_1+R_2C_2-1.5R_2C_1\right)\le 0 \quad (17)$$

$$\text{FO: } \omega_o=\left(\frac{1}{C_1C_2R_1R_2}\right)^{\frac{1}{2}} \quad (18)$$

Quadrature current outputs depicted in Figure 9 are related as

$$I_{O1}=I_{O2}\,j\omega C_2R_2 \quad (19)$$

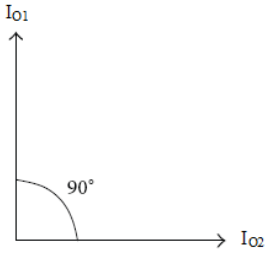


Figure 9. Phasor diagram depicting quadrature current outputs

The circuit was designed with $C_1 = C_2 = 10$ pF, $R_1 = 1k\Omega$ and $R_2 = 2\ k\Omega$, the theoretical frequency of oscillation was around $f_o = 11.26$ MHz, whereas the simulated values as found from the result was $f_o = 11.16$ MHz. Quadrature current outputs are shown in Figure 10.

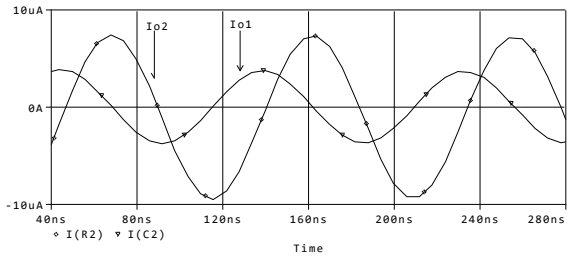


Figure 10. Current outputs of quadrature oscillator

9. Conclusion

This paper has presented a general cascadable current-mode configuration that can realize first-order all-pass, second-order all-pass and notch filter responses employing single MO-DXCCII and two impedances. The proposed configuration uses only two resistors and one capacitor for realizing a first-order all-pass filter, and two resistors and two capacitors for realizing second-order all-pass/notch filter. Furthermore, by making slight modification in the second-order notch filter, a band-pass filter is also reported. As an application, a current-mode quadrature oscillator is also presented. All the circuits of filters enjoy low-input and high-output impedance feature, which is a desirable feature for the current mode cascading. Besides, the circuit uses grounded capacitors, which are suited for IC implementation. The proposed circuit is validated through PSPICE simulation program and shown to be in good agreement with the theoretical results.

10. References

[1] C. Toumazou, F. J. Lidgey and D. G. Haigh, Analogue IC design: the current-mode approach, Peter Peregrinus Ltd., London, (1990).

[2] S. Minaei, and E. Yuce, “All grounded passive elements current-mode all-pass filter”, *Journal of Circuits, Systems and Computers*, vol. 18, pp. 31–43, 2009.

[3] M. Bhusan, and R. W. Newcomb, “Grounding of capacitors in integrated circuits”, *Electronics Letters*, vol. 3, pp. 148–149, 1967.

[4] A. M. Soliman, “Inductorless realization of an all-pass transfer function using the current conveyor”, *IEEE Transactions on Circuits Theory*, vol. 20, pp. 80–81, 1973.

[5] M. Higashimura, and Y. Fukui, “Realization of current mode all-pass networks using a current conveyor”, *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 660–661, 1990.

[6] M. Higashimura, “Current-mode all-pass filter using FTFN with grounded capacitor”, *Electronic Letter*s, vol. 27, pp. 1182–1183, 1991.

[7] M. T. Abuelma’atti, “Cascadable current-mode filters using single FTFN”, *Electronics Letters*, vol. 32, pp. 1457-1458, 1996.

[8] A. M. Soliman, “Theorems relating to port interchange in current-mode CCII circuits”, *International Journal of Electronics*, vol. 82, pp. 582–604, 1997.

[9] A. M. Soliman, “Generation of current conveyor-based all-pass filters from op-amp based circuits”, *IEEE*

Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, pp. 324–330, 1997.
[10] I. A. Khan, and S. Maheshwari, "Novel first order all-pass sections using a single CCIII", *International Journal of Electronics*, vol. 88, pp. 773–778, 2001.
[11] S. Kilinç, and U. Çam, "Current-mode first-order all-pass filter employing single current operational amplifier", *Analog Integrated Circuits and Signal Processing*, vol. 41, pp. 47 – 53, 2004.
[12] U. Çam, "A novel current-mode second-order notch filter configuration employing single CDBA and reduced number of passive components", *Computers and Electrical Engineering*, vol. 30, pp. 147–151, 2004.
[13] S. Minaei, and M. A. Ibrahim, "General configuration for realizing current-mode first order all-pass filter using DVCC", *International Journal of Electronics*, vol. 92, pp. 347–356, 2005.
[14] I. A. Khan, P. Beg, and M. T. Ahmed, "First-order current mode filters and multiphase sinusoidal oscillators using CMOS MOCCIIs", *The Arabian Journal for Science and Engineering*, vol. 32, pp. 119-126, 2007.
[15] S. Maheshwari, "Novel cascadable current-mode first-order all-pass section" *International Journal of Electronics*, vol. 94, pp. 995–1003, 2007.
[16] D. Prasad, D. R. Bhaskar and A. K. Singh, "Universal current-mode biquad filter using dual output current differencing transconductance amplifier", *AEU: International Journal of Electronics and Communications*, vol. 63, pp. 497-501, 2009.
[17] S. Minaei, and E. Yuce, "Unity/Variable-gain voltage-mode/current-mode first-order all-pass filters using single dual-X second-generation current conveyor", *IETE Journal of Research*, vol. 56, pp. 305-312, 2010.
[18] P. Beg, M. A. Siddiqi and M. S. Ansari, "Multi output filter and four phase sinusoidal oscillator using CMOS DX-MOCCII", *International Journal of Electronics*, vol. 98, pp. 1185-1198, 2011.
[19] J. Mohan, and S. Maheshwari, "Cascadable current-mode first-order all-pass filter based on minimal components", *The Scientific World Journal*, vol. 2013, 2013.
[20] J. Mohan, B. Chaturvedi, and S. Maheshwari, "Novel current-mode all-pass filter with minimum component count", *International Journal of Image, Graphics and Signal Processing*, vol. 5, pp. 32-37, 2013.
[21] D. Prasad, D. R. Bhaskar and M. Srivastava, "Universal current-mode biquad filter using a VDTA", *Circuits and Systems*, vol. 4, pp. 29-33, 2013.
[22] F. Kacar, M. Un, "DVCC based current-mode first order all-pass filter and quadrature oscillator", *Trakya University of Journal Science*, vol. 8, pp. 1-5, 2007.
[23] M. Un, F. Kacar, "Third generation current conveyor based current-mode first order all-pass filter and quadrature oscillator", *Istanbul University-Journal of Electrical and Electronics engineering*, vol. 8, pp. 529-535, 2008.
[24] S. Minaei, M. A. Ibrahim, H. Kuntman, "DVCC based currentmode first-order all-pass filter and its application", *Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems* ICECS 2003, vol. 1, pp. 276 – 279, 2003.
[25] A. Zeki, and A. Toker, "The Dual-X Current Conveyor (DXCCII): A new active device for tunable continuous-time filters", *International Journal of Electronics*, vol. 89, pp. 913-923, 2002.
[26] A. Zeki, and A. Toker, "DXCCII-based tunable gyrator", *International Journal of Electronics and Communications* (AEÜ), vol. 34, pp. 59-62, 2005.
[27] B. Chaturvedi and J. Mohan, "Single active element based mixed-mode quadrature oscillator using grounded components", *IU-Journal of Electrical and Electronics Engineering*, vol. 15, pp. 1897-906, 2015.
[28] S. Maheshwari, and B. Chaturvedi, "High-input low-output impedance all-pass filters using one active element", *IET: Circuits Devices and Systems*, vol. 6, pp. 103-110, 2012.
[29] A. Fabre, O. Saaid, and H. Barthelemy, "On frequency limitations of the circuits based on second generation current conveyors", *Analog Integrated Circuits and Signal Processing*, vol. 7, pp. 113-129, 1995.
[30] J. Mohan, "Single active element based current-mode all-pass filter." *International Journal of Computer Applications*, vol. 82, pp. 23-27, 2013.
[31] J. Mohan, S. Maheshwari, "Two active elements based all-pass section suited for current-mode cascading", *International Journal of Electrical Engineering*, vol. 7, pp. 1217 – 1221, 2013.
[32] B. Chaturvedi, S. Maheshwari, "Current mode biquad filter with minimum component count", *Active and Passive Electronic Components*, vol. 2011, pp. 1-7, 2011.
[33] S. J. G. Gift, "The application of all-pass filters in the design of multiphase sinusoidal systems", *Microelectronics Journal*, vol. 31, pp. 9–13, 2000.
[34] B. Chaturvedi, S. Maheshwari, "Current Mode Quadrature Oscillators using DVCC and grounded components", *National Conference at AMU, MTECS-08*, 2008.

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