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CURRENT-MODE ACTIVE-C PHASE EQUALIZERS OPERATED AT LOW VOLTAGE

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Abstract: *This paper presents two novel current-mode active-C phase equalizer circuits which are operated at low voltage. Both the proposed circuits employ single DXCCII as an active element, a NMOS transistor operated in the triode region as an active resistor and a capacitor. It is further been emphasized that the proposed structure of phase equalizers consists of active elements only along with a capacitor hence is named as active-C phase equalizer. Since the structure of the proposed circuits is based on active resistor, therefore both the proposed active-C phase equalizers can be easily tuned through gate voltage of active resistor. Moreover, the proposed phase equalizers enjoy the feature of high output impedance therefore it is easy to cascade the proposed circuits with other current-mode circuits. The proposed circuits also exhibit low active and passive sensitivities. Non-ideal analysis is further discussed. As an application, one of the proposed circuits is connected in cascade to get higher order active-C phase equalizer. The proposed circuits are verified through simulation results using PSPICE program on cadence tool.*
Keywords: *Current-mode, Low voltage, Phase equalizer, DXCCII.*

1. Introduction

In analog circuit design, there is often a large demand for circuits with some explicit performances for signal processing. Current-mode approach is defined by signals, which usually processed in the current domain and has some familiar advantages such as it does not require high precision passive components, so they can be designed almost entirely with active components. It makes the current mode circuits ideal for IC implementation. Finally, they confirm good performance in terms of accuracy, bandwidth and speed. Recently, with the increasing demand of the current-mode approach as a way to design low-voltage, low-power circuits, current conveyors have achieved an increased popularity [1].

With the use of current conveyors, current-mode filter circuits such as current mode all-pass filters are widely used in the field of analog signal processing. All-pass filters are linear systems which are used to correct the phase of an electrical signal while keeping its amplitude constant over a frequency range of interest. Moreover, all-pass filters provide an alternative realization of phase equalizers for analog signal processing applications. Such phase equalizers are very significant, since they permit adjustment in the phase of a signal without introducing any distortion in the amplitude of a signal. In the literature, a number of all-pass filters/phase equalizers based on different active elements are reported [2-5, 7-10, 12-24] and the references cited therein. A comparison study with existing works has been given in Table 1.

In this paper, two novel current-mode phase equalizers are proposed. Both employ a single dual-X second-generation current conveyor (DXCCII), a NMOS transistor operated in the triode region as an active resistor and a capacitor. Since the structure of the proposed circuits is based on active resistor hence the proposed circuits can be tuned easily by the gate voltage of active resistor. The proposed phase equalizers exhibit the feature of high output impedance thus the proposed circuits can be easily cascaded. The proposed circuits also enjoy low active and passive sensitivities.

Table 1 shows a comparison between the proposed phase equalizers and the recently reported works with the following advantages: (i) the reduced number of active element counts, (ii) the reduced number of passive element counts, (iii) availability of current output at high impedance terminal, (iv) no need to impose component matching constraints, (v) operating at low voltage, (vi) can operate at high frequency, (vii) low active and passive sensitivity performances, and (viii) active-C realization.

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Table 1. Comparison between the proposed phase equalizers and the recently reported works

References	Active element used	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)	(viii)
2	CCII	1	4	Y	Y	NA	1.59KHz	NA	N
3	FTFN	1	3	N	Y	NA	1.59KHz	NA	N
4	CDBA	1	2	Y	N	±2.5 V	1.59MHz	N	N
5	CCIII	1	2	N	N	NA	100KHz	Y	N
7	DVCC	1	3	Y	Y	±2.5 V	1.06MHz	Y	N
8	CCCII	1/2	2/1	N	Y	NA	110KHz	NA	Y
9	CCIII	1	2	N	N	±5 V	100KHz	Y	N
10	COA	1	2	Y	N	±2.5 V	1.59MHz	Y	N
12	DVCC	1	3	Y	Y	±2.5 V	1.06MHz	Y	N
13	MOCCII	1	2	Y	N	±2.5 V	358KHz	Y	N
14	DVCC	1	2	N	N	±2.5 V	134KHz	Y	N
15	CCII	2	3	Y	Y	±2.5 V	1.59MHz	Y	N
16	DVCC	1	3	Y	Y	±2.5 V	159KHz	NA	N
17	CCIII	1	4	Y	Y	±2.5 V	159KHz	Y	N
18	DVCC	1	2	Y	N	±2.5 V	1.59MHz	Y	N
19	DOCCII	2	2	Y	N	±1.25 V	1.59MHz	NA	N
20	DXCCII	1	4	Y	Y	±1.25 V	1.59MHz	Y	N
Proposed Circuits	**DXCCII**	**1**	**2**	**Y**	**Y**	**±0.9 V**	**40MHz**	**Y**	**Y**

Abbreviations: CCII: Second Generation Current Conveyor, FTFN: Four-Terminal Floating Nullor, CDBA: Current Differencing Buffered Amplifier, CCIII: Third Generation Current Conveyor, DVCC: Differential Voltage Current Conveyor, CCCII: Current Controlled Second Generation Current Conveyor, COA: Current Operational Amplifier, MOCCII: Multi Output Second Generation Current Conveyor, DOCCII: Dual Output Second Generation Current Conveyor, DXCCII: Dual-X Second Generation Current Conveyor, NA: Not Available, Y: Yes, N: No.

2. Proposed Active-C Phase Equalizers

Dual-X second-generation current conveyor [6,11] is very useful active building block, which has found a number of applications in the area of analog signal processing [20, 25-28]. The symbol and CMOS implementation of DXCCII are shown in Fig. 1. The terminals relationships of the DXCCII are characterized as:

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \quad (1)$$

The proposed circuits of current-mode phase equalizer are shown in Fig. 2. Both the proposed circuits consist of a single DXCCII, an active resistor and a capacitor. The transfer function of the proposed circuits of Fig. 2 using equation (1) is given as follows

$$\frac{I_{OUT}}{I_{IN}} = -\left(\frac{s - \dfrac{1}{R_{MOS}C}}{s + \dfrac{1}{R_{MOS}C}} \right) \quad (2)$$

where, R_{MOS} is the resistance of the NMOS transistor in Fig. 2 and is given by

$$R_{MOS} = \left[\mu C_{ox} \left(\frac{W}{L} \right) (V_G - V_t) \right]^{-1} \quad (3)$$

where, μ_n, C_{ox}, V_t, W and L are the surface mobility, oxide capacitance, threshold voltage, channel width and the channel length of NMOS.

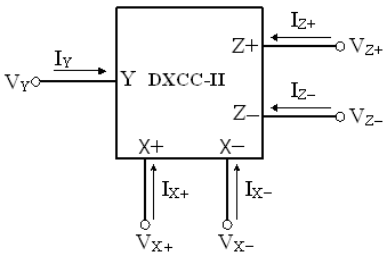
It is to be noted from equation (2) that no passive element matching constraints are required for the proposed circuits. The expressions for the gain (H) and frequency dependent phase angle (Φ) of the proposed circuits of phase equalizer are given as

$$H(\omega) = \left| \frac{I_{OUT}}{I_{IN}} \right| = 1 \quad (4)$$

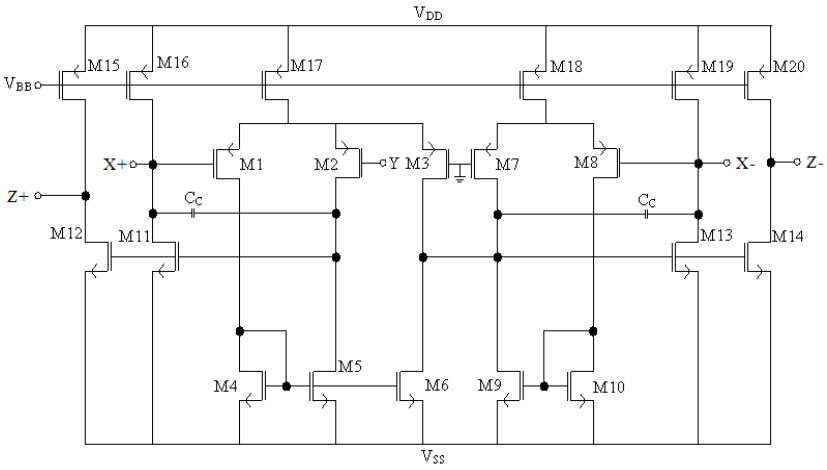
$$\angle\phi(\omega) = -2\tan^{-1}(\omega R_{MOS} C) \quad (5)$$

Note that

$$\angle\phi(\omega) = \begin{cases} 0 & if\ \omega = 0 \\ -90^\circ & if\ \omega = \dfrac{1}{R_{MOS}C} \\ -180^\circ & if\ \omega \to \infty \end{cases} \quad (6)$$



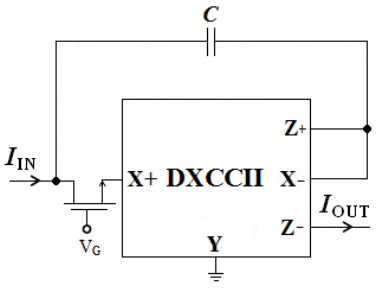
(a)



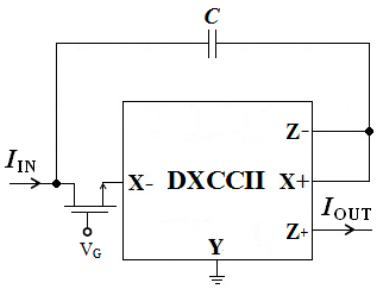
(b)

Figure 1. (a) Symbol of DXCCII (b) CMOS implementation of DXCCII [6, 11]

From equation (6), it is to be observed that the phase of the proposed circuits can vary from 0° to -180°. Therefore, the proposed phase equalizers provide frequency-dependent phase shift with unity gain.



(a)



(b)

Figure 2. (a) Proposed current-mode active-C phase equalizer, (b) Another circuit obtained by interchanging ports

3. Non-ideal Analysis

Taking non-idealities of the DXCCII into account, the port relationships of the voltages and currents modify to

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_1 & 0 & 0 \\ -\beta_2 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & 0 & \alpha_2 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix} \tag{7}$$

Here, α_1 and α_2 are the current transfer gains from X+ and X- terminals to Z+ and Z- terminals , respectively and β_1 and β_2 are the voltage transfer gains from Y input terminal to X+ and X- terminals, respectively. Moreover, the ideal value for these transfer gains is unity. Using equation (7), the proposed circuits are reanalyzed thus the modified current transfer functions yield as

For Fig. 2 (a): $$\frac{I_{OUT}}{I_{IN}} = -\alpha_2 \left(\frac{s - \dfrac{\alpha_1}{R_{MOS}C}}{s + \dfrac{1}{R_{MOS}C}} \right) \tag{8}$$

For Fig. 2 (b):

$$\frac{I_{OUT}}{I_{IN}} = -\alpha_1 \left(\frac{s - \dfrac{\alpha_2}{R_{MOS}C}}{s + \dfrac{1}{R_{MOS}C}} \right) \tag{9}$$

The expressions for current gain (H) and frequency dependent phase angle (Φ) are now changed as given below

For Fig. 2 (a):

$$H(\omega) = \left| \frac{I_{OUT}}{I_{IN}} \right| = \alpha_2 \sqrt{\frac{(\omega R_{MOS}C)^2 + {\alpha_1}^2}{(\omega R_{MOS}C)^2 + 1}} \tag{10}$$

For Fig. 2 (b):

$$H(\omega) = \left| \frac{I_{OUT}}{I_{IN}} \right| = \alpha_1 \sqrt{\frac{(\omega R_{MOS}C)^2 + {\alpha_2}^2}{(\omega R_{MOS}C)^2 + 1}} \tag{11}$$

For Fig. 2 (a):

$$\angle\phi(\omega) = -\left[\tan^{-1}\left(\frac{\omega R_{MOS}C}{\alpha_1} \right) + \tan^{-1}(\omega R_{MOS}C) \right] \tag{12}$$

For Fig. 2 (b):

$$\angle\phi(\omega) = -\left[\tan^{-1}\left(\frac{\omega R_{MOS}C}{\alpha_2} \right) + \tan^{-1}(\omega R_{MOS}C) \right] \tag{13}$$

It has now been emphasized that the ideal values for both the transfer gains are unity, hence equations (8) and (9) can be reduced to equation (2). Moreover, it can be seen from equations (10) to (13) that the non-idealities do affect the current gain as well as the phase angle but the pole frequency (ω_o) is not influenced by non-idealities of DXCCII. However, equations (10) and (11) can also be reduced to equation (4) and equations (12) and (13) can be reduced to equation (5) for the ideal values of transfer gains.

The active and passive sensitivities of pole frequency (ω_0) and current gain (H) are given as

For Fig. 2(a):

$$S_{R_{MOS},C}^{\omega_0} = -1,\ S_{\alpha_1}^{H} = \frac{\alpha_1^2}{\alpha_1^2 + (\omega R_{MOS}C)^2},\ S_{\alpha_2}^{H} = 1,$$

$$S_{R_{MOS},C}^{H} = \frac{(\omega R_{MOS}C)^2 (1 - \alpha_1^2)}{(\omega^2 R_{MOS}^2 C^2 + \alpha_1^2)(\omega^2 R_{MOS}^2 C^2 + \alpha_1^2)} \tag{14}$$

For Fig. 2(b):

$$S_{R_{MOS},C}^{\omega_0} = -1,\ S_{\alpha_2}^{H} = \frac{\alpha_2^2}{\alpha_2^2 + (\omega R_{MOS}C)^2},\ S_{\alpha_1}^{H} = 1,$$

$$S_{R_{MOS},C}^{H} = \frac{(\omega R_{MOS}C)^2 (1 - \alpha_2^2)}{(\omega^2 R_{MOS}^2 C^2 + \alpha_2^2)(\omega^2 R_{MOS}^2 C^2 + \alpha_2^2)} \tag{15}$$

It is clear from equations (14) and (15) that active and passive sensitivities of ω_o and H are less than unity in magnitude for ideal values of both the transfer gains and equal capacitor and resistor design.

4. Stability of the Proposed Phase Equalizers

The current transfer gain (α) and voltage transfer gain (β), for current conveyors such as DXCCII are not real, these are frequency dependent. Moreover, in most of the cases, the values of these transfer gains are taken as unity. However, if both the transfer gains are considered as frequency dependent then the frequency limitation has been added to DXCCII.

The expressions for α_j and β_j, where j = 1, 2 can now be modelled as

$$\alpha_j(s) = \frac{\alpha_{0j}}{1 + s\tau_{ij}};\ \beta_j(s) = \frac{\beta_{0j}}{1 + s\tau_{vj}} \tag{16}$$

where, $\tau_{ij} = \dfrac{1}{2\pi f_{ij}}$; $\tau_{vj} = \dfrac{1}{2\pi f_{vj}}$

where α_{0j} and β_{0j} for j = 1, 2 denote their lower frequency values, f_{ij} and f_{vj} denotes the 3-dB frequencies of the current and voltage transfer gains, respectively. Reanalysis of the proposed circuits of Fig. 2 yields the following transfer functions

For Fig. 2 (a):

$$\frac{I_{OUT}}{I_{IN}} = -\frac{\alpha_{02}}{1 + s\tau_{i2}} \left(\frac{sR_{MOS}C(1 + s\tau_{i1}) - \alpha_{01}}{sR_{MOS}C(1 + s\tau_{i1}) + \alpha_{01}} \right) \tag{17}$$

For Fig. 2 (b):

$$\frac{I_{OUT}}{I_{IN}} = -\frac{\alpha_{01}}{1+s\tau_{i1}}\left(\frac{sR_{MOS}C(1+s\tau_{i2})-\alpha_{02}}{sR_{MOS}C(1+s\tau_{i2})+\alpha_{02}}\right) \quad (18)$$

Equations (17) and (18) shows that some extra poles are appear in the phase equalizer characteristics. Furthermore, to test the stability of the proposed circuits, the characteristic equations of non-ideal transfer functions of equations (17) and (18) are expanded as given below:

For Fig. 2 (a):

$$D(s) = s^3R_{MOS}C\tau_{i1}\tau_{i2} + s^2R_{MOS}C(\tau_{i1}+\tau_{i2}) + s(R_{MOS}C+\alpha_{01}\tau_{i2})+\alpha_{01} \quad (19)$$

For Fig. 2 (b):

$$D(s) = s^3R_{MOS}C\tau_{i1}\tau_{i2} + s^2R_{MOS}C(\tau_{i1}+\tau_{i2}) + s(R_{MOS}C+\alpha_{02}\tau_{i1})+\alpha_{02} \quad (20)$$

Routh–Hurwitz stability criterion is now applied on the non-ideal characteristic equations to test the stability of the proposed circuits. After successfully applying the Routh–Hurwitz stability criterion, the results show that no stability problem is caused by the new poles. However, the transfer functions may be simplified by neglecting the effect of the far-off pole for specific values of the tracking error parameters.

5. P-Spice Simulations

To verify the theoretical analysis of the proposed phase equalizers, the PSPICE simulations, of Fig. 2(a), were performed with the component values: C = 4pF and gate control voltage (V_G) as V_G = 0.52V. The CMOS implementation of DXCCII as shown in Fig. 1(b) was realized using the TSMC 90nm process parameters with supply voltages of ±0.9V. The proposed phase equalizer of Fig. 2(a) is designed at pole frequency of 40MHz. The gain and phase response of the circuit of Fig. 2(a) are shown in Fig. 3 and Fig. 4 respectively, which shows that the pole frequency is 39.68MHz with the percentage error of 0.8%. It has been observed from Fig. 4 that the proposed circuit acts as a phase equalizer by introducing 90° phase shift. The input and output waveforms are therefore shown in Fig. 5 which verifies the circuit as a phase equalizer. The Fourier spectrum of the output signal, showing a high selectivity for the applied signal frequency (40MHz), is also shown in Fig. 6. The X-Y plot is further shown in Fig. 7, which supports the circuit performance as 90° phase shifter. The usefulness of new circuit is to be especially emphasized keeping in view the design frequency which is quite high. To further support the circuit practical utility, the pole frequency is made controllable through gate voltage (V_G) at 0.36V, 0.45V, 0.52V at constant value of capacitor (4pF). The pole frequency control through gate voltage (V_G) is shown in Fig. 8. It has been observed from Fig. 8, the pole frequencies at output are found to be 20MHz, 30MHz and 40MHz. This further confirms the practical utility of the proposed circuits.

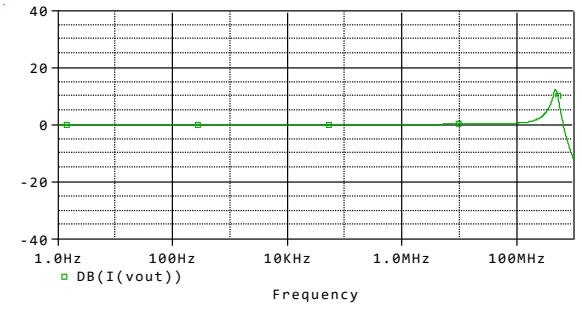


Figure 3. Gain (dB) plot at 40MHz

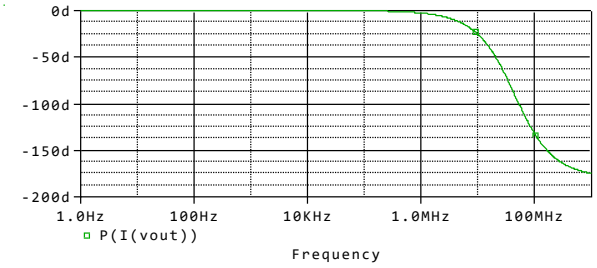


Figure 4. Phase (degree) plot at 40MHz

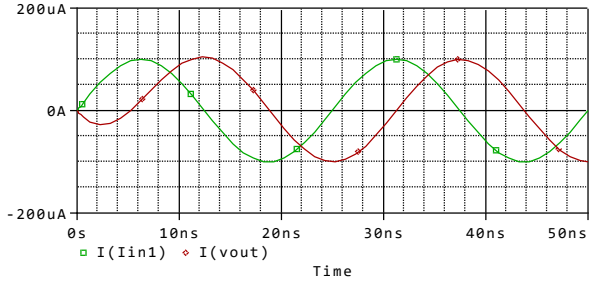


Figure 5. Input/output waveforms at 40MHz

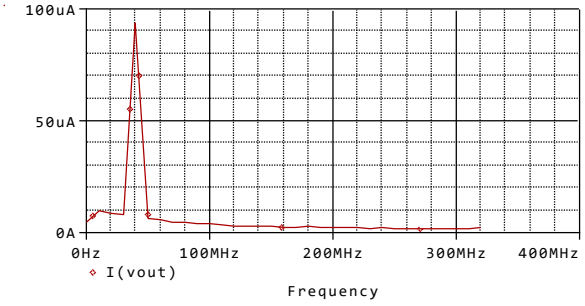


Figure 6. Fourier spectrum of output waveform at 40MHz

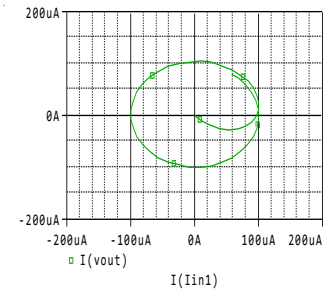


Figure 7. X-Y plot showing 90° phase shift

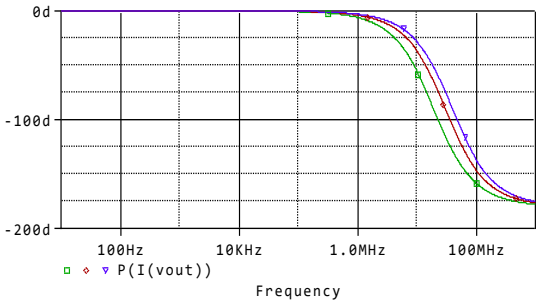


Figure 8. Phase variation at different values of V_G

6. n[th]-order Active-C Phase Equalizer

An n[th]-order active-C phase equalizer is also realized by utilizing the feature of cascadability of the proposed circuit of Fig. 2(a). The proposed n[th] order active-C phase equalizer consists of n-DXCCII, n-capacitors, and n-MOS resistors is shown in Fig. 9. The circuit analysis of Fig. 9 yields the following transfer function

$$\frac{I_{OUT(n)}}{I_{IN}} = (-1)^n \left(\frac{s - \frac{1}{R_{MOS1}C_1}}{s + \frac{1}{R_{MOS1}C_1}} \right) \times \left(\frac{s - \frac{1}{R_{MOS2}C_2}}{s + \frac{1}{R_{MOS2}C_2}} \right) \times \Lambda \times \left(\frac{s - \frac{1}{R_{MOSn}C_n}}{s + \frac{1}{R_{MOSn}C_n}} \right) \quad (21)$$

It may also be noted that such a cascade arrangement results in higher order functions with real poles and zeroes.

The pole frequency $\omega_o(n)$ is given by:

$$\omega_{o(n)} = \left(\frac{1}{(R_{MOS1}R_{MOS2}\Lambda\ R_{MOSn}) \times (C_1C_2\Lambda\ C_n)} \right)^{\frac{1}{n}} \quad (22)$$

To further illustrate the usefulness, a second order phase equalizer can be implemented from Fig. 9 by taking n=2 (2 DXCCII, 2 MOS resistors and 2 capacitors). By taking n = 2 in equation (21), the transfer function now becomes

$$\frac{I_{OUT(2)}}{I_{IN}} = (-1)^2 \left(\frac{s - \frac{1}{R_{MOS1}C_1}}{s + \frac{1}{R_{MOS1}C_1}} \right) \times \left(\frac{s - \frac{1}{R_{MOS2}C_2}}{s + \frac{1}{R_{MOS2}C_2}} \right) \quad (23)$$

The pole frequency (ω_o) from equation (22) is given as:

$$\omega_{o(2)} = \left(\frac{1}{R_{MOS1}R_{MOS2}C_1C_2} \right)^{\frac{1}{2}} \quad (24)$$

For verification purposes, the circuit of second order phase equalizer is designed at 40MHz, by taking C_1= C_2 = 4pF and V_{G1}= V_{G2}= 0.52V. The gain and phase plots are shown in Fig. 10. The phase is found to vary with frequency from 0 to -360° with a value of -180° at the pole frequency. Similarly, the variation of phase can be further controlled by deciding the order of n[th]-order phase equalizer. Moreover, Fig. 11 (a) shows that at the pole frequency, input and output waveforms are 180° phase shifted as expected. The Fourier spectrum of the output is shown in Fig. 11 (b).

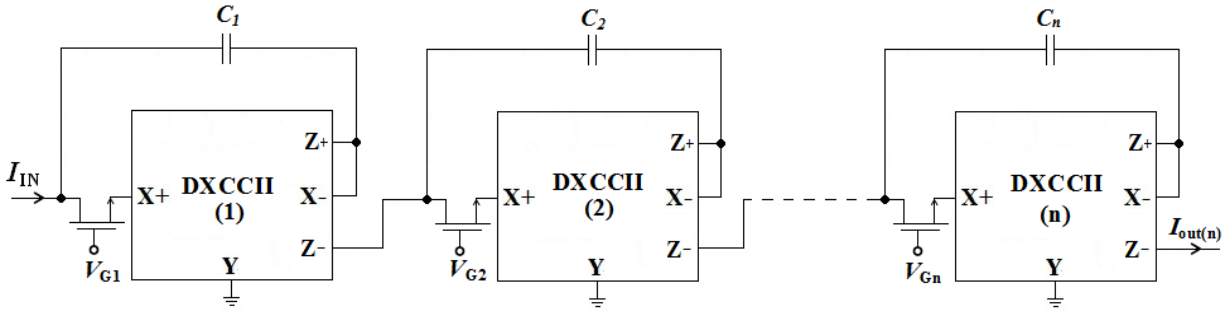
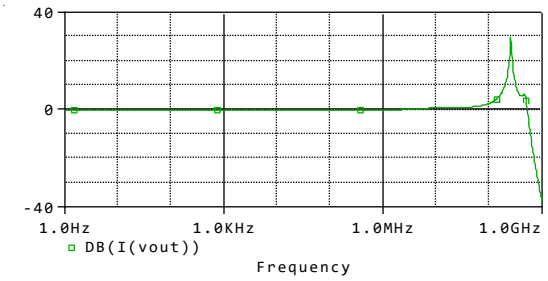
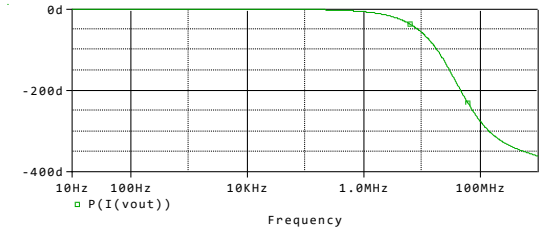


Figure 9. Proposed n[th] order current-mode active-C phase equalizer

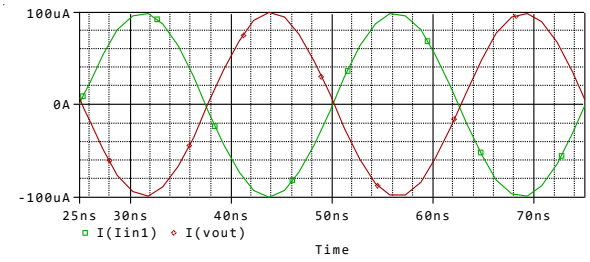


(a)

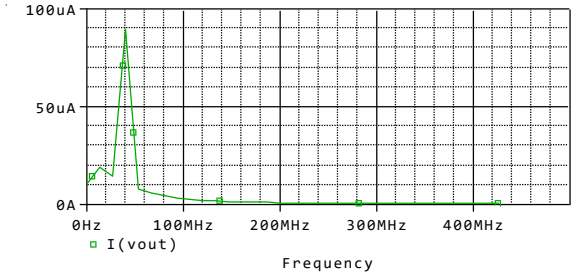


(b)

Figure 10. (a) Gain (dB) (b) Phase (degree) plot at 40MHz



(a)



(b)

Figure 11. (a) Input/output waveforms (b) Fourier spectrum of output at 40MHz

7. Conclusion

This paper presented two novel circuits of current-mode active-C phase equalizers which are operated at low voltage. Both the proposed circuits consist of single DXCCII, a NMOS transistor as an active resistor and a capacitor. By using the MOS transistor based active resistor, the feature of tunability and integrability has been added to the proposed circuits. The proposed active-C phase equalizers have an added advantage of tunability through external control voltage. Non-ideal analysis is also discussed. The proposed phase equalizers are also useful for cascading. For utilizing the feature of cascadability, an application of nth-order active-C phase equalizer realization is further given. All the proposed circuits are found to show good frequency performance. Simulation results are given to confirm the presented theory. Thus, the proposed circuits have enhanced the existing knowledge on the analog signal processing circuits.

8. References

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