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## A Comparison Electronic Specifications of the MS & MPS type Schottky Diodes (SDs) via Utilizing Voltage-Current (V-I) Characteristics

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Keywords	Abstract
(TeO <sub>2</sub> :Cu-doped PVP) Interlayer On Performance MS, MPS Type SDs Difference Between Calculation Methods Density of Surface States	The effects of the application of the (TeO <sub>2</sub> :Cu-PVP) interface to the Al/p-Si (MS) type SD on the performance of the new Al/(TeO <sub>2</sub> :Cu doped PVP)/p-Si (MPS) SD were reviewed using forward and reverse bias V-I measurements. The thermionic emission (TE) and Cheung & Cheung functions were employed to ascertain the influences of an additional organic interfacial layer on the comparative outcomes of this research. Thus, some essential electrical attributes such as saturation current (I <sub>s</sub> ), ideality factor ( <i>n</i> ), rectification-ratio (R.R.=I <sub>forward</sub> /I <sub>reverse</sub> ), barrier height B.H. (Φ <sub>bo</sub> ), and series/shunt resistances (R <sub>s</sub> /R <sub>sh</sub> ) were computed. Furthermore, the density of surface states (N <sub>ss</sub> ) was acquired from the V-I plots according to the Card & Rhoderick method. The observed experimental results indicated that the (TeO <sub>2</sub> :Cu-PVP) inter-layer enhanced the quality of MS type SD as respects obtained low reverse current, N <sub>ss</sub> , R <sub>s</sub> , and high R <sub>sh</sub> and R.R. values. All these results indicate that (TeO <sub>2</sub> :Cu-PVP) inter-layer can be used successfully instead of conventional insulators for its favored specifications like easy fabrication processes, low cost, and flexibility features.
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### 1. INTRODUCTION

Metal/semiconductor (MS) structures are critical emphasis in semiconductor technology. The interfacial layer added between the metal and the semiconductor changes the performance of the structure. When native or deposited inter-layer is performed between metal and semiconductor, MS type SD transforms to metal/inter-layer/semiconductor (MIS) type SDs. The functioning or quality of these structures is dependent on various parameters or factors like surface preparation, the nature of B.H. and inter-layer located M/S interface, their homogeneity, the concentration of donor/acceptor atoms, the existence of N<sub>ss</sub>/ D<sub>it</sub>, R<sub>s</sub> and R<sub>sh</sub>, and fabrication processes (Sze, 1981; Sharma, 1984; Rhoderick & Williams, 1988; Reddy et al., 2017; Tanrikulu et al., 2017). Although conventional SiO<sub>2</sub> is stable and abundant since it cannot passivate all unwanted surface states or dislocations, the leakage current and surface states are very high (Sze, 1981; Sharma, 1984; Rhoderick & Williams, 1988; Reddy et al., 2017). Therefore, in recent years, many researchers have started to use an organic/polymer interlayer instead of conventional SnO<sub>2</sub> or SiO<sub>2</sub> grown by a traditional method like thermal and wet-oxidation.

Organics/polymers are popular in semiconductor-based device technology with some outstanding advantages over insulators. Some of these prominent advantages can be listed as the easy grown process on the surface, low weight/cost/energy consumption, elasticity, high dynamic durability, ability to dissolve in water, and good charge-storage capacity (Altındal et al., 2019; Tataroğlu et al., 2020; Barkhordari et al., 2021). Among polymer materials, polyvinyl-pyrrolidone (PVP) has a semi-crystalline, high water-solubility, nontoxic-polymer, wide

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range of crystallinity, high dielectric strength, good charge storage capacity, interesting physical properties which arise from OH groups and formation of hydrogen bonding.

Known as a nonlinear optical material,  $\text{TeO}_2$  is widely preferred in optical device technology as tunable filters, deflectors, and modulators (Bindra et al., 2001). It is believed that an extra added thin organic layer with high-dielectric grown between metal and the semiconductor will increase the efficiency and quality of the designed device. Various basic techniques such as electro-spinning (Altındal et al., 2019), simple reactive thermal-evaporation, sol-gel (Coste et al., 2007), melt quenching (Shivachev et al., 2009), and ultrasound-assisted (Suslick & Doktycz, 1990) are used to create an organic interface with high dielectric permittivity. Due to its apparent advantages in the literature, the ultrasound-assisted method was used within this study to form the tellurium dioxide ( $\text{TeO}_2$ )-Cu doped PVP organic interface that has grown at M/S interface.

The main purpose of this study is to fabricate Al/p-Si (MS) and Al/( $\text{TeO}_2$ :Cu-PVP)/p-Si (MPS) SDs on the same p-Si wafer to determine this organic interlayer effects on the SD by utilizing the V-I measurements in wide range of voltage ( $\pm 5\text{V}$ ). For this aim, the basic electrical parameters of them were extracted from these data and compared each other. In addition, the values of  $N_{ss}$  as a function of energy were also extracted from the V-I data, regarding the ideality factor and the voltage dependence of BH. Experimental results show that there was a step-up in R.R. and Rsh values and a lessening in leakage-current,  $R_s$ , and  $N_{ss}$  values. These results were attributed to the used organic ( $\text{TeO}_2$ :Cu-PVP) thin film as an interfacial layer at the inter-surfaces of the SD (Card & Rhoderick, 1971; Çetinkaya et al., 2021; Demirezen et al., 2022; Ulusoy et al., 2023).

## 2. MATERIAL AND METHOD

Both the type-1 and the type-2 SDs were chemically grown on the selfsame p-Si substrate at identical status. Two same-quarter Boron-doped (p-Si) substrates were cleaned in the ultrasonic bath by using standard RCA method (5 units deionize-water ( $\text{H}_2\text{O}$ ), 1 unit ammonium hydroxide (27%  $\text{NH}_4\text{OH}$ ), 1 unit hydrogen peroxide (30%  $\text{H}_2\text{O}_2$ ) for 15 minutes, rinsed in deionize-water for prolonged time, and dried up with a high percentage of purity level dry nitrogen gas ( $\text{N}_2$ ). Secondly, high-pure Al (99.99%) was thermally evaporated onto the entire rear of two p-Si substrates at  $10^{-6}$  Torr and then annealed in the nitrogen-ambient at  $450^\circ\text{C}$  to get satisfactory ohmic contact. Copper acetate-dehydrates ( $\text{Cu}(\text{CH}_3\text{COO})_2$ ) sodium-telluride/hydroxide ( $\text{Na}_2\text{TeO}_3$ , NaOH) was purchased from the Rankem, Lobachemi, and Merck Company, respectively, and they used for the preparation of the ( $\text{TeO}_2$ :Cu) nanostructures. After that 0.2 M of the solution of copper acetate, 0.2 M of  $\text{Na}_2\text{TeO}_3$  solution, and 2 M NaOH solution were prepared by using deionize-water. The performed cationic and anionic solutions were added together and kept under exposure of 100 W ultrasonic-waves for 15 minutes and so the product was centrifuged and washed using an ultrasonic-bath and centrifuged devices for 5 times, and finally it dried at  $40^\circ\text{C}$  for 45 hours in an oven. The arranged ( $\text{TeO}_2$ :Cu-PVP) solution was grown onto front of first-quarter p-Si wafer by using ultrasonic assisted method. Finally, the same Al rectifier contacts with 1 mm diameter were grown onto the ( $\text{TeO}_2$ :Cu-PVP) and onto front of second p-Si wafer. More explanation both on the cleaning procedure, growing of organic interlayer, and ohmic/rectifier contacts can be seen in (Pirgholi-Givi et al., 2021) references. The schematic impression of two type SDs were provided in Figure 1. The V-I measurements of them were performed by utilizing the Keithley-2400 source-meter.

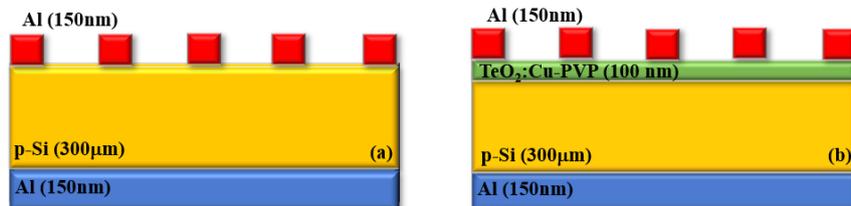


Figure 1. Schematic diagram of the a) M-S and b) M-P-S type SDs

## 3. RESULTS AND DISCUSSION

Some critical and fundamental electrical parameters, which are saturation-current ( $I_0$ ), ideality-factor ( $n$ ) and zero-bias B. H. ( $\Phi_{b0}$ ), and series resistance ( $R_s$ ) of the manufactured MS and MIS diodes are conventionally calculated from the forward bias V-I records by employing thermionic-emission (TE) model (Sze, 1981;

Sharma, 1984; Rhoderick & Williams, 1988). When these structures have  $R_s$  and ideality factor higher than unity, the correlation between  $I$  and  $V$  is provided as presented below for  $V_F \geq 3 \cdot (kT/q)$  (Sharma, 1984; Rhoderick & Williams, 1988):

$$I(V) = I_o \left[ \exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1 \right] \quad (1)$$

In Equation 1, the values of  $I_o$  and  $n$  can be calculated via using the intercept and slope changes in the linear section of  $\ln I$  vs  $V$  plot as given following relation, respectively.

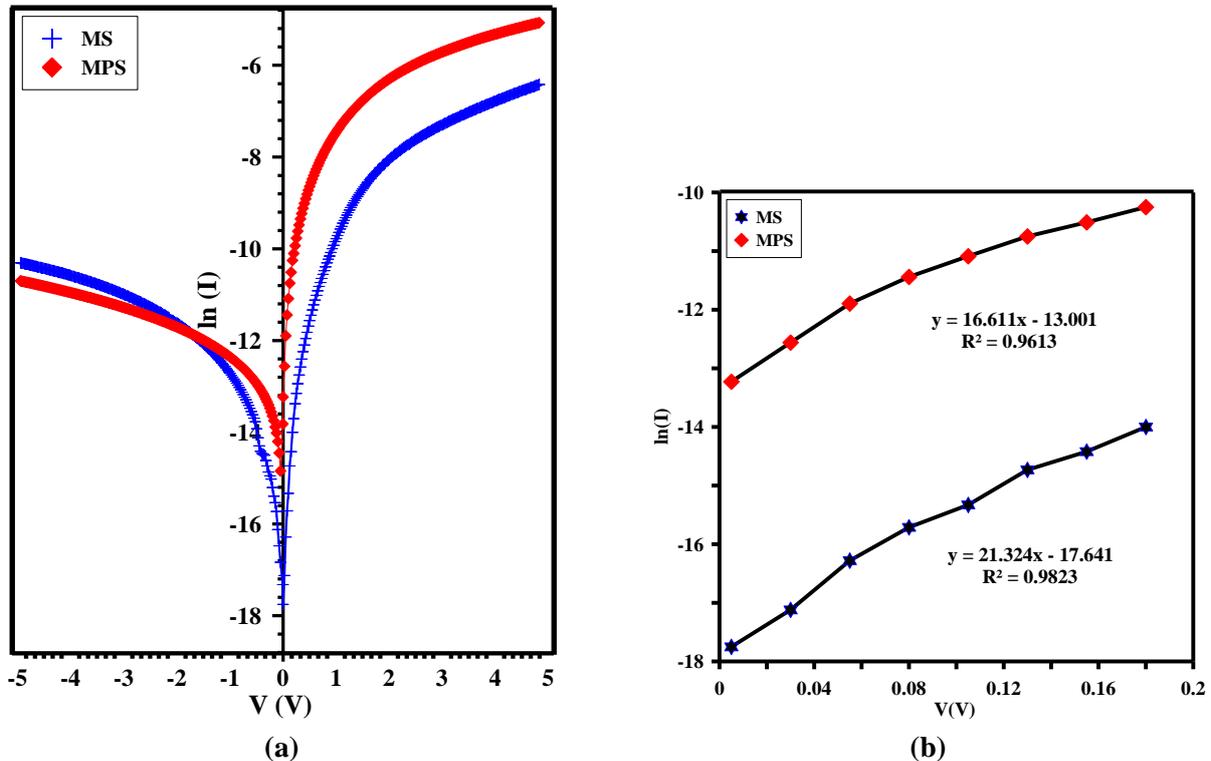
$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \text{ and } n = \frac{q}{kT} \left(\frac{dV}{d(\ln I)}\right) \quad (2)$$

Hence,  $\Phi_{b0}$  value was calculated using  $I_o$  and  $A$  values as given follows.

$$\Phi_{b0} = \left(\frac{kT}{q}\right) \ln \left[ \left(\frac{AA^*T^2}{I_o}\right) \right] \quad (3)$$

Figure 2 shows the  $\ln(I_F)$ - $V_F$  characteristics of the constructed type-1 and the type-2 SDs. It is seen that the  $\ln I$ - $V$  plots of these diodes have satisfying rectifying characteristic.

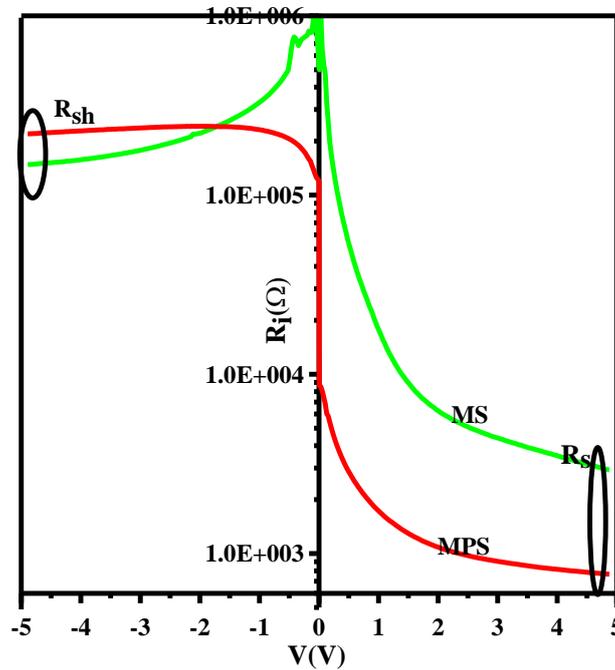
The value of R.R. is the ratio of the current at the exact same positive and negative voltages. Thus,  $I_o$ ,  $n$ ,  $\Phi_{b0}$ , and R.R. (at  $\pm 5V$ ) were obtained from the  $V$ - $I$  data as  $2.2 \times 10^{-8}$  A, 1.829, 0.692 eV, 51.1 for Al/p-Si type and  $2.3 \times 10^{-6}$  A, 2.348, 0.576 eV, 286.2 for Al/(TeO<sub>2</sub>:Cu-PVP)/p-Si type SDs, respectively. These structures series and shunt resistances also showed noteworthy effectuality in  $V$ - $I$  measurements. While the value of  $R_s$  leads to deviation from linearity at high enough voltages in positive bias,  $R_{sh}$  leads to non-saturated in the reverse bias  $V$ - $I$  plot, respectively (Çetinkaya et al., 2021; Ulusoy et al., 2023).



**Figure 2.** a) The  $\ln(I_F)$  -  $V_F$  curves for the two different kinds of fabricated SDs, b) The  $\ln(I_F)$  - zoom ( $0 V_F$  -  $0.2 V_F$ ) curves for the two different kinds of fabricated SDs

Both the existence of  $R_s$  and  $N_{ss}$  are more effective on the forward bias V-I characteristics. In general,  $R_s$  can be originated from the ohmic and rectifier contacts, the used probe wires to rectifier contact, the resistivity of bulk-semiconductor, and non-homogeneities of doping atoms in the semiconductor, the perform native or deposited interfacial layer at M/S interface. (Nicollian & Brews, 1982). There are different approaches to obtaining  $R_s$  in the literature, but Ohm's Law is the best (Sze, 1981; Sharma, 1984). According to this method, the structures resistance ( $R_i$ ) shows dependency on voltage ( $V_i$ ), but the actual  $R_s$  values for these structures show strong relations with high forward bias voltages. Obtained  $R_i$  values are shown in Figure 3 with  $R_i$  vs V graphs.

The voltage-dependent  $R_i$  ( $=dV_i/dI_i$ ) versus  $V_i$  profile corresponds to higher reverse voltages, while  $R_s$  corresponds to higher forward voltages.  $R_i$ -and- $R_s$  values for MS type are 2.86 k $\Omega$ , 0.15 M $\Omega$ , while 0.76 k $\Omega$ , 0.22 M $\Omega$  for MPS type SD. All basic electronic parameters ( $I_o$ ,  $n$ ,  $\Phi_{bo}$ , R.R.,  $R_s$ ,  $R_{sh}$ ) were also tabularized in Table 1. It is clear that there is an improvement in the MPS type SD compared to the MS type SD at room temperature.



**Figure 3.** The  $\ln(R_i)$  vs  $V$  records of the fabricated M-S , M-P-S type SDs

**Table 1.** Fundamental electronic attributes of the type-1 and the type-2 SDs using the TE and Cheung's method

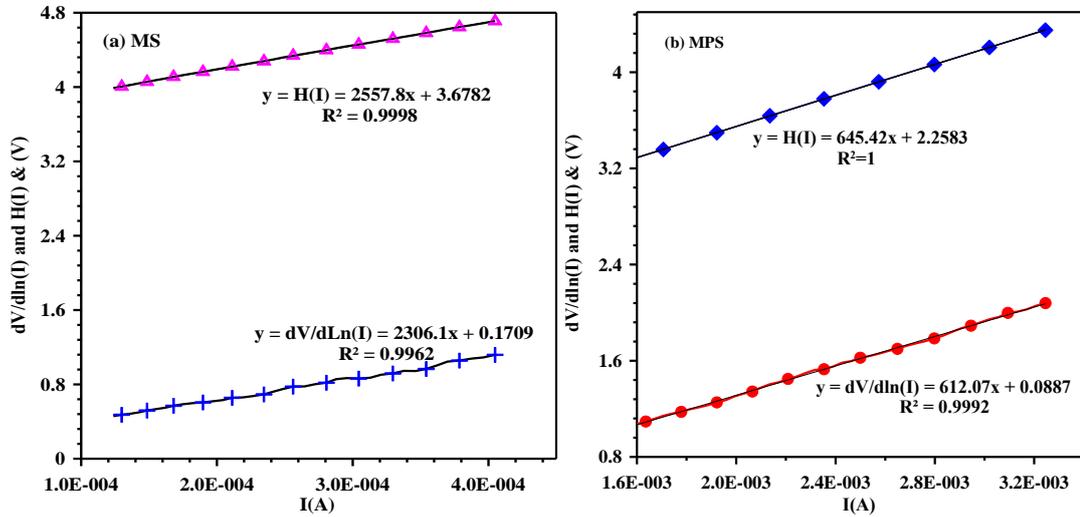
Samples	TE Theory				Cheung's Functions			
	$I_o$ (A)	$n$	$\Phi_b$ (eV)	R.R.	$n$	$R_s$ (k $\Omega$ ) $dV/d\ln(I)-I$	$\Phi_b$ (eV)	$R_s$ (k $\Omega$ ) $H(I)-I$
Al/p-Si	$2.2 \times 10^{-8}$	1.83	0.692	51.1	6.84	2.31	0.54	2.56
Al/(PVP-TeO <sub>2</sub> :Cu)/p-Si	$2.3 \times 10^{-6}$	2.35	0.576	286.2	3.55	0.61	0.65	0.65

Table 1 indicates the used structures and methods, which show organic interfacial layer grown between interfaces, the efficiency of the MS type SD is directly related to the growth in R.R. and  $R_{sh}$  values versus the lessening of leakage-current,  $R_s$ , and  $N_{ss}$  values. The fundamental electrical parameters ( $n$ ,  $\Phi_{bo}$ ,  $R_s$ ) for two SDs were also calculated from the Cheung's functions as a second way (Cheung & Cheung, 1986). According to Cheung and Cheung (1986), the  $n$ ,  $\Phi_{bo}$ ,  $R_s$  values were acquired alternatively by using I-V data in the light of following relations:

$$\frac{dV}{d(\ln I)} = n \left( \frac{kT}{q} \right) + R_s I \quad (4a)$$

$$H(I) = V - n \left( \frac{kT}{q} \right) \ln \left( \frac{I}{AA^*T^2} \right) = n\Phi_b + R_s I \quad (4b)$$

Figures 4a and 4b show the  $dV/d\ln(I)$  vs  $I$  and  $H(I)$  vs  $I$  plots of the type-1 and the type-2 SDs, in turn. As seen, these plots exhibit satisfying linear characteristics in a wide range of currents. The interception & inclination of the linear fit of  $dV/d\ln(I)$ - $I$  yielded the values of  $n$  &  $R_s$  as 6.84, 2.31 k $\Omega$  for MS and 3.55, 0.61 k $\Omega$  for MPS type SDs, respectively. After that by using these values of  $n$  in Equation 4(b),  $H(I)$  vs  $I$  yielded  $\Phi_b$  and  $R_s$  as 0.54 eV, 2.56 k $\Omega$  for type-1 SD and 0.65 eV, 0.65 k $\Omega$  for the type-2 SD, in turn. Both the  $R_s$  and B.H. values were calculated by Cheung and Rhoderick method and compared to Ohm's Law. The observed discrepancies are the result of the nature of the chosen method and its dependence on voltage (Orak et al., 2017; Tanrikulu et al., 2017; Altındal Yerişkin, 2019).



**Figure 4.** a), b) The scatter  $dV/d\ln(I)$  vs  $I$  and  $H(I)$  vs  $I$  graphs of the M-S and M-P-S type SDs

The effectiveness of surface states/traps ( $N_{ss}$ ) on the conduction mechanisms is significantly greater in the intermediate forward polarization region. Defects or traps that have occurred between the semiconductor/interface with energy during the manufacture of the devices correspond to the semiconductors' band gap. These traps are usually rooted from the interruption of the periodic lattice-structure of the surface, cleaning of surface preparation, some impurities in the semiconductor, and the organic pollution in the laboratory environment and the energy dependence of them was calculated by subtracting positive polarization V-I data by using the Card & Rhoderick method (1971). The  $N_{ss}$  vs energy curve was extracted from  $V_F$ - $I_F$  data by using following relations (Card & Rhoderick, 1971; Sharma, 1984; Altındal et al., 2019):

$$n(V) = \frac{qV_i}{kT \ln \left( \frac{I_i}{I_0} \right)} = 1 + \frac{d_i}{\epsilon_i} \left[ \frac{\epsilon_s}{W_D} + qN_{ss}(V) \right] \quad (5a)$$

$$\Phi_e - \Phi_{b0} = \left( 1 - \frac{1}{n(V)} \right) V_i \quad (5b)$$

In Equation 5 (a, b), the variables are presented successively as  $d_i$ ,  $\epsilon_s$ ,  $\epsilon_i$ , and  $W_D$  for the statements, the permittivity of the semiconductor, permittivity of the inter-layer, depletion layer breadth and the thickness of

inter-layer. Expression of  $N_{ss}$  in a dependency relation to energy is obtained from the following equation (5c) when considering the top of the  $E_v$  valence band (Card & Rhoderick, 1971).

$$E_{ss} - E_v = q(\Phi_e - V) \quad (5c)$$

For the MS and MPS type SDs,  $N_{ss}$  vs  $(E_{ss} - E_v)$  plots were obtained from Equation 5 (a-c) by using current-voltage measurements in forward bias voltage and given in Figure 5.

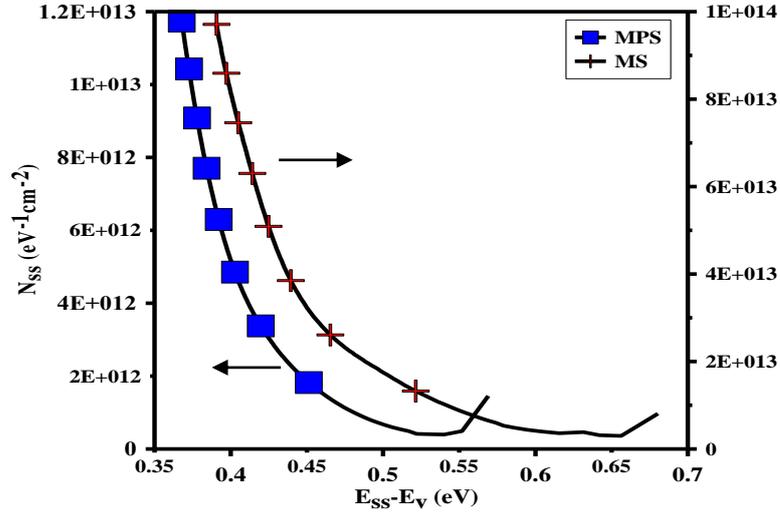


Figure 5. The  $N_{ss}-(E_{ss}-E_v)$  profile of M-S and M-P-S type SDs

The values of  $N_{ss}$  almost scaled up from the midgap of Si to the peak point of the valence-band  $E_v$ , as seen in Figure 5. While the value of  $N_{ss}$  changed between  $(9.71 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2})$  at  $(0.39-E_v)$  and  $(8.07 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2})$  at  $(0.68-E_v)$  for MS and  $(1.17 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2})$  at  $(0.368-E_v)$  and  $(1.46 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2})$  at  $(0.57-E_v)$  for MPS kind SD, in turn. These obtained values of  $N_{ss}$  are also suitable for the type-1 and the type-2 SDs. The  $N_{ss}$  value for the interlayered SD is about one order lower than the SD without an interfacial layer by virtue of the passivation effect of the  $(\text{TeO}_2:\text{Cu-PVP})$  inter-layer used. For this reason, organic  $(\text{TeO}_2:\text{Cu-PVP})$  can be a sufficient substitute for customary interfacial layers. Similar observations were also obtained by various researchers in the literature very recently (Demirezen & Altındal Yerişkin, 2020). Similar results on the  $R_s$ ,  $N_{ss}$ , and interfacial layer in the SDs were also reported in the recent years (Çetinkaya et al., 2021; Demirezen et al., 2022; Ulusoy et al., 2023).

#### 4. CONCLUSION

In this work, the MPS and MS-type SDs were fabricated onto a selfsame p-Si substrate to define the outcomes on fundamental electrical parameters of the  $(\text{TeO}_2:\text{Cu-PVP})$  structure as an inter-layer by utilizing the V-I measurements in a voltage scale of  $(\pm 5\text{V})$  at room temperature. Since TE is available at moderate bias voltage ranges, and Cheung's functions are effective at high enough forward bias voltages, to observe the voltage and method dependencies of the fundamental electrical attributes of these structures,  $(n, \Phi_{bo}, R_s)$  were acquired from both TE theory and Cheung's functions. Besides, the  $R_{sh}$  and rectification-ratio values of aforesaid structures were also calculated from V-I data records at  $\pm 5\text{V}$ . Finally, plots of surface state effects  $N_{ss}$ , highly related to energy, were also obtained from the  $V_F-I_F$  data, the voltage dependency of  $n(V)$  and B.H. The values of  $N_{ss}$  changed from  $9.71 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$  at  $(0.39-E_v)$  to  $8.07 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  at  $(0.68-E_v)$  for MS type SD and  $1.17 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$  at  $(0.368-E_v)$  to  $1.46 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  at  $(0.57-E_v)$  for MPS type SD, respectively. These spin-offs reveal that the  $N_{ss}$  value for type-1 SD is about one order higher than the type-2 SD because of the passivation effect of the organic  $(\text{TeO}_2:\text{Cu-PVP})$  inter-layer investigated in this study. In other words, the used inter-layer leads to improvement of the M/S type SD, taking into account low leakage current/ $R_s/N_{ss}$  values, and higher B.H., R.R., and  $R_{sh}$  values. For this reason, organic  $(\text{TeO}_2:\text{Cu-PVP})$  is a good candidate with satisfying electrical features for inter-layer replacements compared to traditional ones already in use.

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## CONFLICT OF INTEREST

The author declares no conflict of interest.

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