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Design and Implementation of 1-bit Comparator in Quantum-dot Cellular Automata (QCA)

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Abstract. For immense demand of speedy high-end gadgets, chips are becoming denser, but Moore's law is falling flat lately. Complementary Metal-Oxide-Semiconductor (CMOS) technology is on its brink. Quantum-dot cellular automata (QCA) has become a potential alternative technology to provide faster speed with low power dissipation at nano-scale extent. Here, we proposed an efficient QCA design of 1-bit comparator. The proposed comparator required 59% less area and dissipated 82% less energy. QCA Designer has been used to design and simulate the proposed comparator. Finally, QCAPro tool has been employed for estimating energy dissipation.

Keywords: Comparator, Energy dissipation, QCA Designer, QCAPro

Kuantum Noktalı Hücresel Otomasyonlarda 1 Bitlik Karşılaştırıcı Tasarımı ve Uygulanması

Özet. Hızlı üst düzey cihazların büyük talepleri için çipler yoğunlaşmakta ancak Moore yasası son zamanlarda düşmektedir. Tamamlayıcı Metal-Oksit-Yarı iletken (CMOS) teknolojisi eşiğe ulaşmıştır. Kuantum noktalı hücresel otomasyon (QCA), nano ölçekte düşük güç dağılımıyla daha hızlı bir hız sağlamak için potansiyel bir alternatif teknoloji haline gelmiştir. Bu çalışmada, 1 bitlik karşılaştırıcının verimli bir QCA tasarımı önerdik. Önerilen karşılaştırıcı,% 59 daha az alan gerektirir ve % 82 daha az enerji tüketir. QCA Tasarımcısı, önerilen karşılaştırıcıyı tasarlamak ve simule etmek için kullanılmıştır. Son olarak, enerji yayılımını tahmin etmek için QCAPro aracı kullanılmıştır.

Anahtar Kelimeler: Karşılaştırıcı, Enerji Dağılımı, QCA Tasarımcısı, QCAPro

1. INTRODUCTION

Reducing power dissipation and area density of circuits are the most concerning issue at present computing paradigm. The traditional CMOS technology faced many limitations such as high level scaling, high power consumption, heat generation and high lithography cost [1]. To overcome such limitations, a number of extensive researches have been taken place to find the alternatives [1-4]. One of the possible alternatives Quantum-dot cellular automata (QCA), was proposed by lent et al [2]. This technology ensures low energy dissipation with higher speed as well as parallel computing capability at nano-scale level [3-5]. A number of studies reported that QCA is suitable for designing different types of logical [6-14] as well as computational [15-19] devices.

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Its basic building block is a cell composed of four dots, operates by changing the position of two electrons. There's two possible arrangement of a cell as two electrons positioned diagonally for columbic repulsion force. Basic logic gates can be designed by arranging these cells in different ways. And one of the most basic building blocks in QCA is majority voter gate (MV) [2-6].

A reversible 1-bit QCA comparator was proposed in [20]. This Feynman gate based comparator required 319 cells and dissipated 762.8 (meV) energy at $\gamma=1.0\ E_k$. Another QCA comparator design has been proposed in [21]. This irreversible comparator required 117 cells to design and occupied 0.182μm^2 area. More efficient and coplanar comparator has been presented in [22]. In this paper, an exclusive-OR gate based optimized 1-bit comparator has been introduced. The QCA implementation of the proposed design used only 42 cells. This layout entails the lowest number of cells and less area as compared to the previous works [20-22].

2. PROPOSED DESIGN

Comparator is a combinational digital circuit that determines whether the two numbers are equal, greater or less than each other. If the inputs are A and B, and outputs are Output $_{(A<B)}$, Output $_{(A=B)}$ and Output $_{(A>B)}$ then the logical expressions of 1-bit comparator are given as:

$$Output_{(A<B)} = \bar{A}.B$$
$$Output_{(A=B)} = \overline{A \oplus B}$$
$$Output_{(A>B)} = A.\bar{B}$$

The majority gate based representation of the above equations is given by

$$Output_{(A<B)} = MV(\bar{A}, B, -1)$$
$$Output_{(A=B)} = \overline{XMV(A \oplus B)}$$
$$Output_{(A>B)} = MV(A, \bar{B}, -1)$$

Here, MV represents the three input majority gate, -1 represents logical “AND” operation and XMV is the three input exclusive-OR gate.

The proposed comparator is designed using three inverter gates, two majority gates and one exclusive-OR gate. The schematic block diagram and circuit layout of the proposed comparator in QCA are shown in Fig. 1 (a) and Fig. 1 (b) respectively.

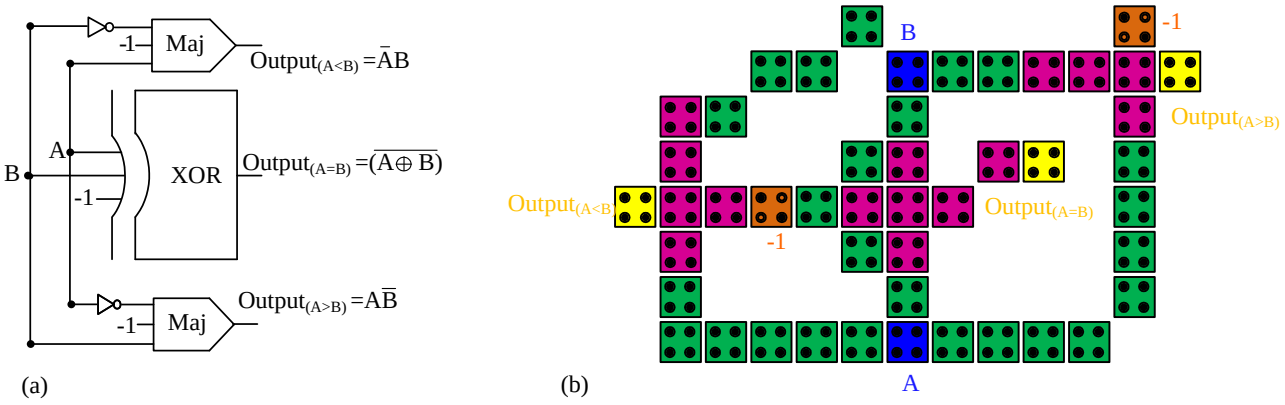

Fig. 1. (a) Schematic block diagram (b) circuit layout of proposed comparator in QCA

3. RESULT and ANALYSIS

The proposed 1-bit comparator is simulated and demonstrated by QCADesigner [24], a common QCA layout designing and simulation tools. The following default evaluation factors are considered for a Bistable Approximation [24] shown in Fig. 2.

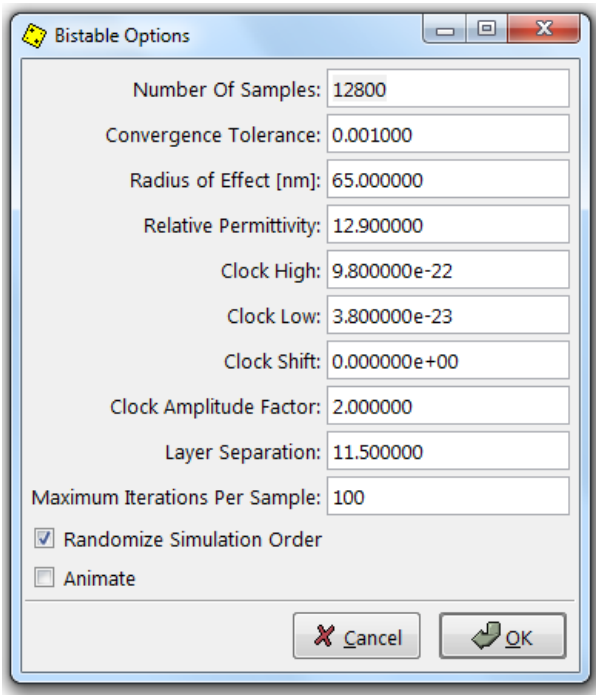

Fig. 2. Default parameters of Bistable approximation.

Table 1. Truth Table of 1-bit comparator.

Input		**Output**		
A	B	Output $_{(A<B)}$	Output $_{(A=B)}$	Output $_{(A>B)}$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

The input-output waveforms for the proposed 1-bit comparator are shown in Fig. 3. The simulation outcome is justified with theoretical values described in Table1. For the input *A=0* and *B=0*, the output will be *Output* $_{(A<B)}$ *=0*, *Output* $_{(A=B)}$ *=1* and *Output* $_{(A>B)}$ *= 0* as reflected in Fig. 3. Similarly, for input *A=0* and *B=1*, the output will be *Output* $_{(A<B)}$ *=1*, *Output* $_{(A>B)}$ *= 0* and *Output* $_{(A=B)}$ *=0*.

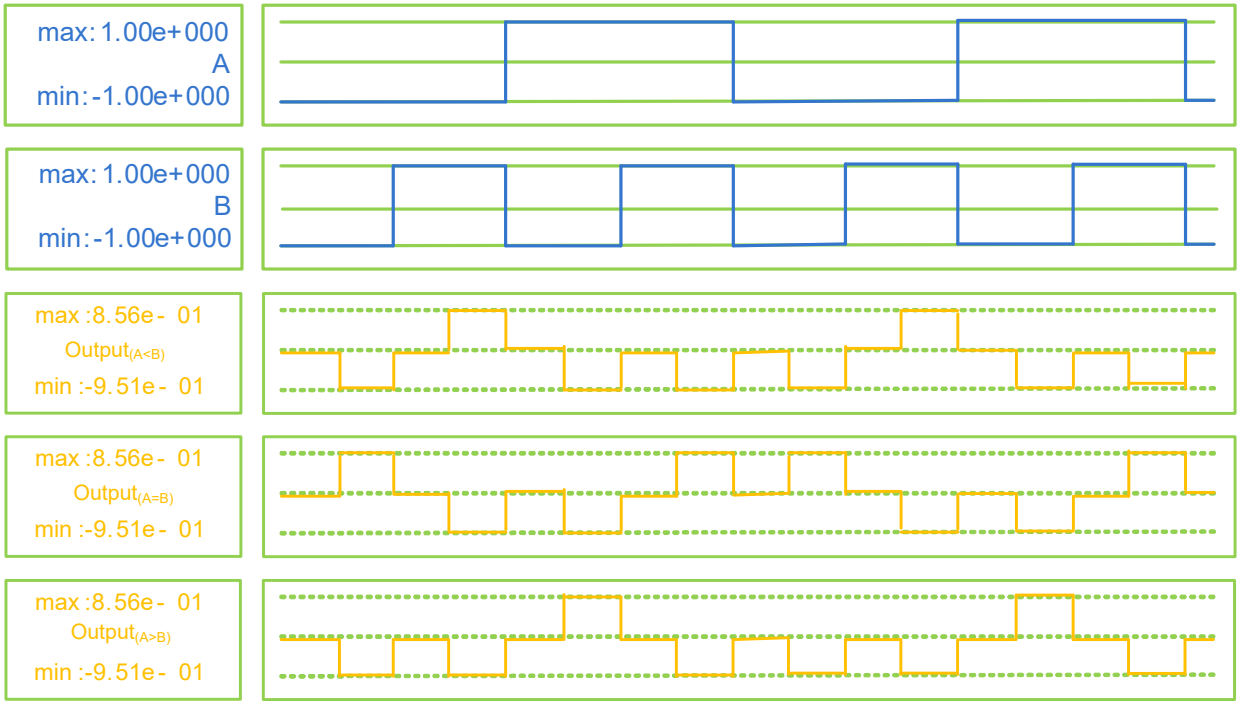

Fig 3. Simulated input-output waveform of proposed 1-bit comparator

As exposed in Table 2, the proposed comparator yields considerable improvements in terms number of cell count, occupied area and time delay. The proposed comparator has around 50% improvement in the cell count, around 59% improvement in covered area, and 60% improvement in time delay compared with the best previous design presented in [23].

Table 2. Comparison of 1 bit comparators.

Comparator design	Majority + Inverter gate	Cell count	Approximated area (μm^2)	Time delay (Clock cycle)
Comparator [20]	32	319	0.343	4
Comparator [21]	15	117	0.182	1
Comparator [22]	8	100	0.127	1.25
Comparator [23]	10	95	0.103	1.25
Proposed Comparator	8	47	0.042	0.50

During operation, every QCA cell dissipates same amount of energy in one clock cycle. The energy dissipation by the complete QCA design is anticipated by the upper bound power dissipation model [25]. The energy dissipation of the proposed QCA circuits is estimated using QCAPro [26] tools at temperature $T = 2.0\ K$ in different tunneling energy [27] level shown in Fig. 4. In Table 3, a comparative energy dissipation study of proposed 1-bit comparator and earlier design [20] is given.

Table 3. Energy dissipation comparison of proposed 1-bit comparator with earlier design at different tunneling energy level at $T=2K$

Circuit	Energy dissipation (meV)			
	$\gamma=0.25\ E_k$	$\gamma=0.50\ E_k$	$\gamma=0.750\ E_k$	$\gamma=1.0\ E_k$
Comparator [17]	629.9	660.5	707.9	762.8
Proposed comparator	113.45	117.81	126.87	151.56

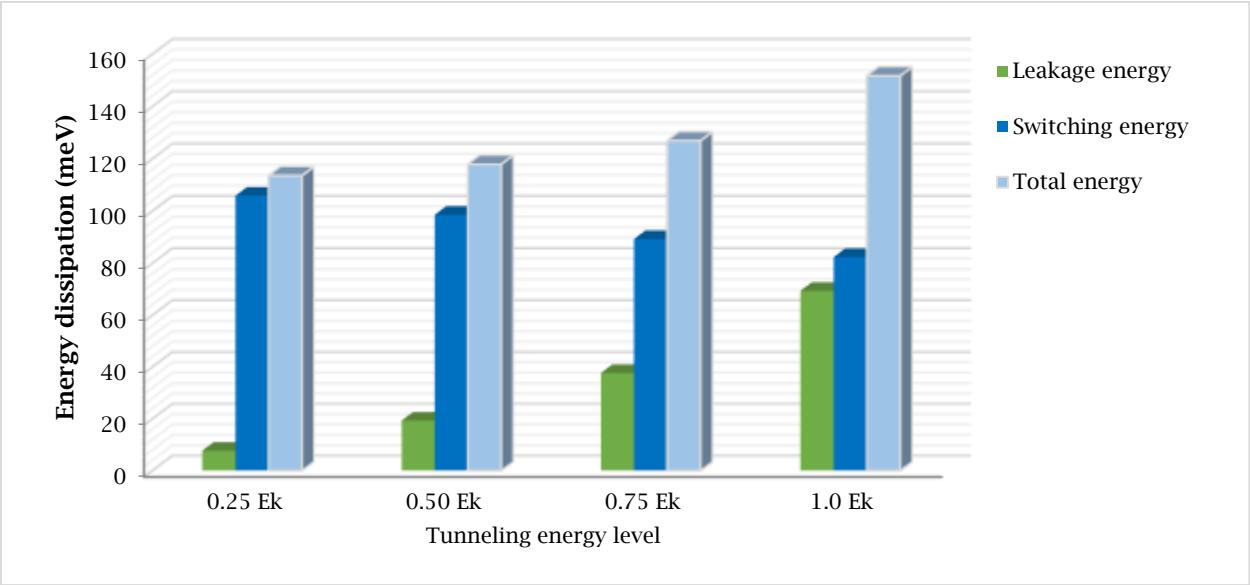

Fig. 4. Energy dissipation graph of proposed 1-bit comparator at different tunneling energy level at *T=2K*

4. CONCLUSION

An optimized design of 1-bit comparator is presented here. The proposed layout is simulated and verified using the QCADesigner tool and the simulation outcome illustrate that the logical function of proposed comparator is correct. This optimized design achieved a significant improvement in terms of energy dissipation, time delay, area and cell count. However, the proposed comparator dissipates 80% less energy at $1.0E_k$ tunneling energy level at *T=2K*. Moreover, in comparison with the best earlier reported comparator design, our proposed comparator has 50% and 59% enhancement in the cell count and occupied area, respectively. Finally, this design can be employed in several calculative applications, which may be performing as a vital unit of a general purpose nano processor.

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