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Research Article

A Single Source Thirteen Level Switched Capacitor Boost Inverter for PV Applications

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Abstract : This work proposes a module unit (MU) based single-source thirteen-level inverter (SSTLI) for solar PV applications. The proposed topology is a 13-level design with a single MU and 1.5 voltage gain. This work describes its operational modes at various output levels. Due to their symmetric functioning within a cycle, two capacitors were series-connected. with MU, the topology achieves self-voltage balancing, which reduces the complexity of control compared to typical Multilevel inverters (MLIs). The single-source generalized structure with additional MUs can be utilized to boost voltage levels for the output. With more MU, voltage gain increases, in addition, the output levels are greatly enhanced. The merits of the proposed SSTLI are fewer components, self-balance, and voltage stress. A comparison between the proposed topology and other MLIs is shown in this work. To determine the viability and dynamic performance of the proposed SSTLI, MATLAB simulation results are presented for dynamic values of the modulation index (M) for different loads along with the harmonic analysis. Experimental results also have been presented for the practicality of SSTLI topology.

Keywords : Multilevel inverter, Switched capacitor, Harmonic distortion, DC-AC inverter, Voltage balancing.

1 Introduction

A variety of MLIs have been presented for industrial applications, in the field of power distribution, transportation, and other applications. For example, Electric vehicles (EVs) with renewable energy generation (REG) systems [1, 2], and so on. MLI offers merits over basic two-level inverter, such as lower harmonic distortion, lowered voltage stress, reduced switching frequency and losses, and so on [3, 4]. The three basic categories of conventional MLIs [5, 6] are Diode Clamped Multilevel inverter (DCMI): Multilevel inverters that use diodes to clamp the voltage of each level to a constant reference voltage are known as "diode clamped" inverters. The second one is the Flying Capacitor Multilevel Inverter (FCMI): In this sort of multilevel inverter, energy is stored and moved between various levels of output waveform using capacitors. The final one of the basic categories of conventional MLIs is the Cascade H-Bridge Multilevel Inverter (CHBMI): This sort of multilevel inverter creates a multi-level output waveform by combining H-bridge circuits. The output waveform of DCMI may not be as smooth as required due to the relatively few levels available. As a result of the more diodes, there is also a higher power loss and higher component cost as a result of the increased diode count.

One of the reasons is that designing and implementing a complicated circuit layout can be challenging. Additionally, the increasing requirement for capacitors drives up component costs, and it might be difficult to attain the high voltage rating needed for the capacitors. Additionally, the output waveform's quality could be impacted by issues with capacitor balance Another reason is that a complicated circuit arrangement necessitates more switches and diodes, which increases power loss owing to more switching. A more complex design and greater component prices are other results of the increased switch and diode count [7]. Therefore, the development of MLIs has focused on aspects like voltage balancing, and decreased power electronic devices, particularly the non-dependent sources. The modified circuits with more output levels are introduced for

high or medium-voltage applications, and active neutral-point-clamped (ANPC) converters that combine the adaptability of FCMIs and DCMIs for generating multilevel output have also been determined in [8, 9]. The voltage and current sensors assist capacitors in maintaining voltage balance with strong dynamic response, but they also add to the complexity of design and operation for these ANPC converters. The seven-level inverters that have been suggested each use a similar approach of voltage balancing with sensors. Control is made simpler with a self-balancing system with a single capacitor. In the absence of sensors, the capacitor's voltage is maintained at half of the input DC source, allowing the overall system cost to be decreased. Additional symmetric isolated DC sources are yet required. Higher output levels result in decreased total harmonic distortion (THD), which allows for output filter needs and lower switching frequency. Additionally, two other switched-source MLI types are suggested as a replacement for the CHBMIs topology, to produce MLI output with reduced switches. A transistor-clamped H-bridge (THB) is often first presented [10]. Due to their similar functioning in negative and positive half cycles, two capacitors in a DC connection may keep their voltages at half of the input, allowing for the realization of a five-level output. It is recommended that the THB units be run in series when powered by asymmetric separated DC sources. This will allow for a higher number of output levels. The voltage level of the experiment is 41 levels with two THB units that have been cascaded incorrectly. The total harmonic distortion (THD) of the line voltage may be as low as 1.2% even in the absence of any filters. Because of its capacity to self-balance voltage and provide expandable output levels, the switched-capacitor MLI (SCMLI) has also emerged as a competitive threat in recent years. For applications that include cascading, the fundamental MLI that is based on switched capacitors has been developed [11, 12]. The series-parallel configuration allows the capacitor to achieve its internal equilibrium. The five-level module has a boost factor that is twice as high as the seven-level module's [13], which only has a voltage gain of 1.5. It is recommended that a quasi-resonant switched-capacitor MLI be used for high-frequency alternating current (HFAC) microgrids [14]. A single DC supply can increase the output level of the device. It cannot, however, increase ability. This work introduces SCMLIs, which are devices made up of several switched-capacitor units. Adding more switched-capacitor units will enhance their output levels and boost factor [15, 16]. However, the switches with their maximum voltage stress see a significant rise. To address this problem, another self-balance SCMLI is recommended. While a few switches are required, the voltage stress at its highest point remains low [17]. Multiple modulation methods for preventing and controlling a variety of MLIs in different applications have been presented in [18, 19, 20, 21, 22, 23, 24, 25, 26, 27].

The proposed SSTLI of module type unit (MU) with only one source and inherent balancing capability is presented in this article. Applications are satisfied by the large number of output levels and its simplicity for voltage balance. In Section 2, a 13-level proposed SSTLI based on MU is initially described. Additionally, a detailed explanation is provided for its various operating levels. The simulation output for differential phase voltages, load current for R-load and RL-load based on modulation index and the comparison analysis with different MLIs shows its advantages in terms of fewer devices, and lower voltage stress are shown in Sections 3 & 4. The experimental analysis is shown in section 5. In Section 6, the result based on the study is concluded.

2 Proposed Single Source Thirteen-Level Inverter (SSTLI) Topology

Figure 1 describes the suggested 13-level proposed structure. It is made up of a single MU each of which has an H-bridge. A diode in cascade with a switch or switch linked end-to-end may also be used to produce the clamping transistor without an antiparallel diode in MU at S_5 (see Figure 1). S_5 is the bi-directional switch. MU functions as the transistor-clamped H bridge. The series capacitors C_4 and C_3 are coupled to the single input source ($2V_{dc}$), and Van produces the multilevel output. C_4 and C_3's voltages naturally remain at V_{dc}, whereas C_1 and C_2's voltages remain at $0.5V_{dc}$. The 13-level SSTLI that is proposed has a 1.5 voltage gain. Figure 3 shows the working modes of the described SSTLI for thirteen-level at various output levels during a negative half-cycle, whereas Figure 2 displays them during a positive half-cycle. As described in Figures 2 and 3, a boost factor of $1.5V_{dc}$ may be reached during $3V_{dc}$ peak output voltage. Complementary power electronic switch pairs (S_4, S_{11}), (S_3, S_{10}), and (S_2, S_9) lessen the complexity of control. Table I provides a summary of the switching states.

An analysis of the 13-level SSTLI with MU that exhibits self-balancing and voltage gains of 1.5 has been provided above. With a single DC supply, the output level may be raised and voltage gain may increase. Beneath the circumstance of n-MU, the following equation can be used to represent the number of output levels MLevel and the voltage boost factor m: $Mlevel = 2^{n+3} - 3$ and $m = 2 - (1/2^n)$.

3 Simulation Results

In this work, to confirm the presented SSTLI topology, MATLAB simulation analysis has been done. The sinusoidal PWM method is used to produce pulses to an inverter switch in SSTLI as shown in Figure 4. For obtaining thirteen levels, 12 carrier signals and 01 reference signal are required. The in-phase carrier-based PWM logic is employed for obtaining gate pulses. The simulation parameters are considered as RL load (R=100Ω & L=110mH), DC supply is 200V, and sampling time is 1/2500sec. As the modulation decreases, voltage levels number in the phase output voltage also decreases. Table 2 shows output phase voltage levels for the 13L inverter for the variation of modulation index (M). Table-2 shows the comparison of Total harmonic distortion (THD), RMS Voltage (V_{RMS}), and Peak voltage (V_{PEAK}) of the proposed SSTLI according to the Modulation index(M)

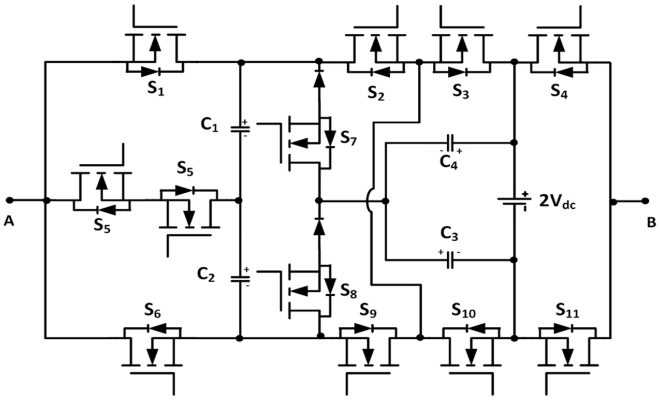


Figure 1: Proposed Single-Source Thirteen-Level Inverter (SSTLI) Topology

Table 1: Switching logic of proposed SSTLI Topology

Switching State	3V	2.5V	2V	1.5V	V	0.5V	0	-0.5V	-V	-1.5V	-2V	-2.5V	-3V
S_1	1	0	1	0	1	0	0	0	0	0	0	0	0
S_2	0	0	1	1	0	0	0	1	1	0	0	1	1
S_3	1	1	1	1	0	0	0	1	1	0	0	0	0
S_4	0	0	0	0	0	0	0	1	1	1	1	1	1
S_5	0	1	0	1	0	1	0	1	0	1	0	1	0
S_6	0	0	0	0	0	0	1	0	1	0	1	0	1
S_7	0	0	0	0	1	1	1	0	0	1	1	0	0
S_8	0	0	1	1	0	0	0	1	1	0	0	0	0
S_9	1	1	0	0	1	1	1	0	0	1	1	0	0
S_{10}	0	0	0	0	1	1	1	0	0	1	1	1	1
S_{11}	1	1	1	1	1	1	1	0	0	0	0	0	0

variation. The change in the number of levels due to variation in the modulation index is also determined in the following table. The THD of the proposed SSTLI increases with the decrease of modulation index as the number of step levels in output phase voltage decreases concerning the decrease in M. From the following table we can observe the changes in amplitude of V_{PEAK} and V_{RMS} for the M.

Fig. 5. shows the change in the amplitude of the waveforms for modulation index(M). The modulation used here in the above simulation is dynamic type. The simulation is respective to the modulation index and time. As the modulation index value is reduced the number of step levels in the output waveform keeps on reducing. The rate of change of levels with the rate of change of the modulation index is recorded in Table III. For a modulation index value of unity, we get a total number of 13 levels and the THD value is 7.58%. The minimum levels obtained are 3 levels with a modulation value of 0.1.

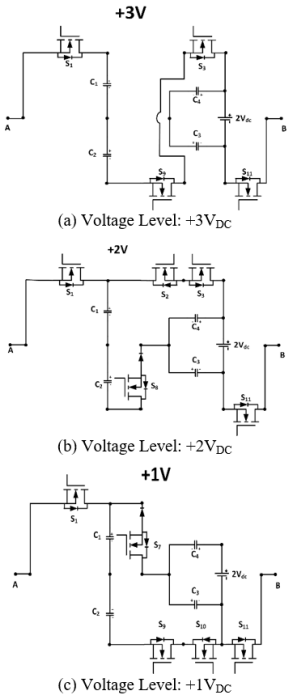
Figure 6. shows the output waveforms of the proposed SSTLI of phase voltage, load current for R-load, and output load current for the RL-load for unity modulation index. When M is set to 1, the output of SSTLI has 13 levels, the rms voltage is 211.4V, and the total harmonic distortion is 7.58. Figure 7 illustrates the frequency spectra of the load voltage as well as the load current when M = 1.0.

4 Comparison of SSTLI with existing MLIs

In this section, the SSTLI MU architecture is compared to MLIs that may extend output levels to highlight the benefits and drawbacks associated with each option. The total standing voltage stress for all power electronics switches is included as one of the comparison items, along with the number of components Ncom and the number of capacitors NCf. It is only appropriate

Table 2: Switching logic of proposed SSTLI Topology

Modulation Index	No. of levels	$V_{PEAK\ [V]}$	$V_{RMS\ [V]}$	THD%
1	13	299	211.4	7.58
0.9	13	269	190.2	9.02
0.8	11	239.1	169.1	10.3
0.7	11	209.2	147.9	10.7
0.6	9	179.4	126.8	14.13
0.5	7	149.6	105.7	14.95
0.4	7	119.4	84.45	20.3
0.3	5	89.71	63.43	28.15
0.2	5	59.72	42.23	34.85
0.1	3	29.72	21.02	92.28

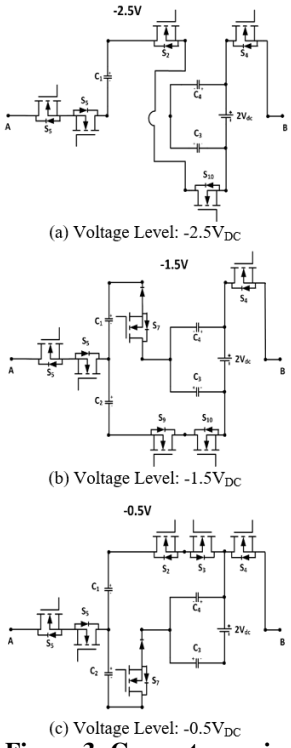


(a) Voltage Level: +3V_{DC}

(b) Voltage Level: +2V_{DC}

(c) Voltage Level: +1V_{DC}

Figure 2: Current carrying paths and conduction modes of SSTLI for positive voltage levels.



(a) Voltage Level: -2.5V_{DC}

(b) Voltage Level: -1.5V_{DC}

(c) Voltage Level: -0.5V_{DC}

Figure 3: Current carrying paths and conduction modes of SSTLI for negative voltage levels.

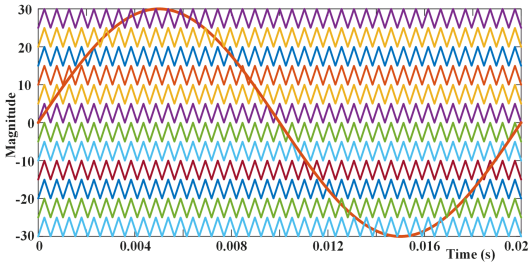


Figure 4: SPWM modulation scheme for thirteen-level inverter.

to calculate TSV as the ratio of total voltage stress on all switching power electronic devices to the topology's output peak voltage since certain topologies are unable to boost. In Table 3, the specific numerical values are presented. As can be observed, to achieve voltage balance, the topologies of [8] must function with a certain modulation. Additionally, closed-loop control and sensors are needed [10] for voltage balance. These additional balancing techniques make the system more complicated. In comparison, the suggested SSTLI design uses the fewest power switches and capacitors with existing MLIs. The biggest benefit of suggested SSTLI is the number of components is reduced with the same output levels. However, it is known that MLI employs the greatest number of power electronic switches to lessen voltage stress. In conclusion, the specific benefits of the suggested topology have been extensively shown. To assess the topology's dependability for practical applications, many factors might be taken into account. First, there is a link between greater control complexity and decreased dependability. To cope with several voltage/current sensors, signal processing circuits, voltage balance of capacitors, complicated control algorithms, and expensive controllers are required for the traditional FC and ANPC topologies, NPC topologies, as well as converters. These will increase the system's complexity and decrease its dependability. In contrast, the suggested SSTLI can self-balancing without the need for complex control or sensors, thereby decreasing the risk of dependability. After that, compared to conventional and alternative inverters, the suggested topology needs fewer devices to produce 13 output levels, which implies a reduced failure probability and quicker reconditioning for the actual operation. The modules (half-bridge and full-bridge) with reliability and design integration may also implement the suggested MU. Last but not least, to further increase the dependability of the suggested prototype, it is encouraged to execute the over-current and overvoltage protection techniques for output and input in real applications.

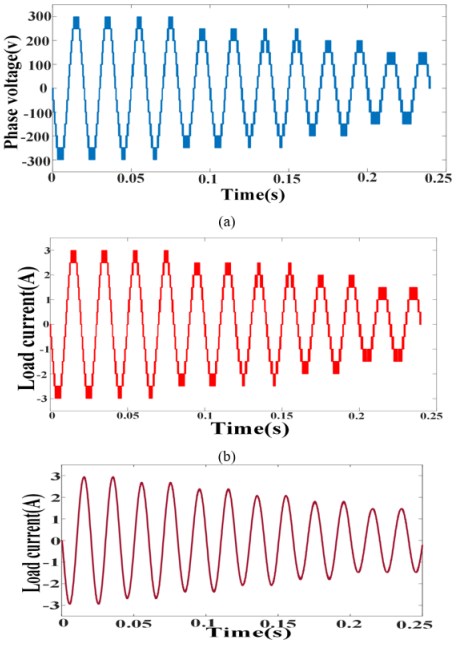


Figure 5: Output waveforms for dynamic modulation index(M). (a) Output phase voltage waveform. (b) Output Load Current of R-load waveform. (c) Load current for RL-Load waveform

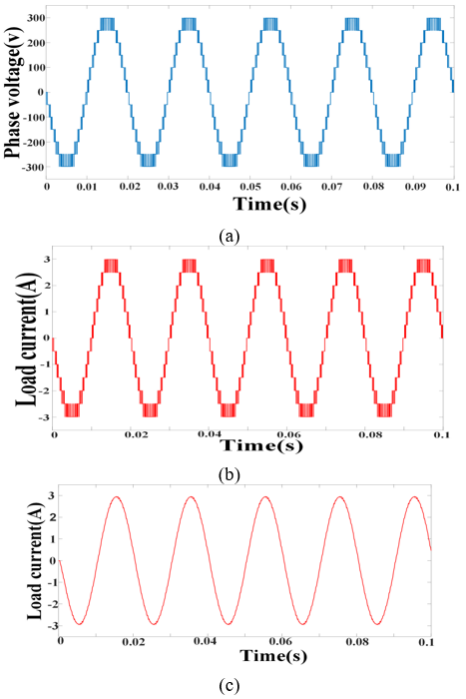


Figure 6: Output waveforms for unity modulation index. (a) Output phase voltage.(b) Output Load current for R-load. (c) Output Load current for RL-load.

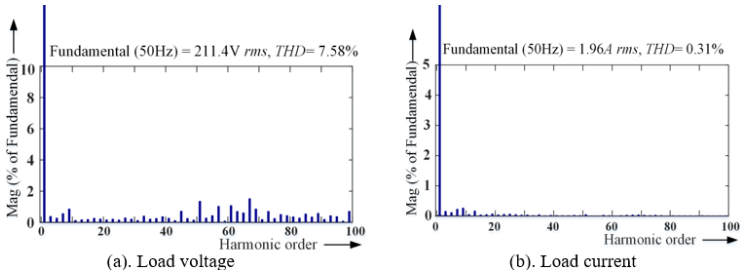


Figure 7: Frequency spectra at unity modulation index.

N_{com} = Number of semi-conductors and N_{cf} = Number of capacitors

5 Hardware Results

An experimental result for each of the different modulation indices (M) has been reported as part of the process of validating a single-source thirteen-level inverter (SSTLI). The parameters of the modulation scheme and the load utilized in this study are the same as those used in the simulation. The power electronic switches' gate signals are made using the DSP TMS32F28335 toolkit. Figure 8 displays the thirteen-level inverter output phase voltage working at different modulation indices between 0.7 and 1.0. This illustration shows that having closed-loop functionality is possible. As the M value rises from 1.0 to 0.7, there are fewer voltage levels in the phase voltage waveform. When the modulation index is set to unity, Figure 9 displays the waveform of the load current. Figure 10 uses M=1.0 and displays the harmonic spectra for the load voltage and load current.

Table 3: Switching logic of proposed SSTLI Topology

Parameter	[8]	[10]	[14]	[15]	[18]	[16]	[17]	SSTLI
N_{com}	14	18	20	19	33	19	34	11
N_{cf}	5	6	6	5	6	5	5	4
Capacitor voltage Balancing	modulation	sensors	self	self	self	self	self	self
Boost factor	no	no	yes	yes	yes	yes	yes	yes
Voltage stress (*Vdc)	3	5	9	6.5	10.6	6.5	4.83	6

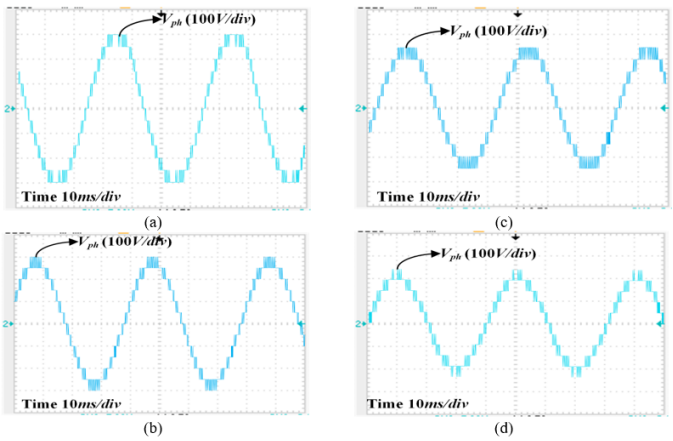


Figure 8: Experimental results of output voltage waveforms for various values of M.

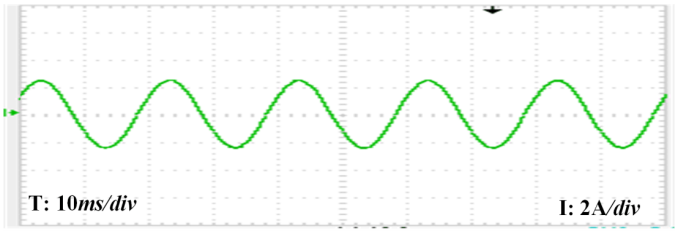


Figure 9: Experimental load current waveform at unity modulation index for RL load.

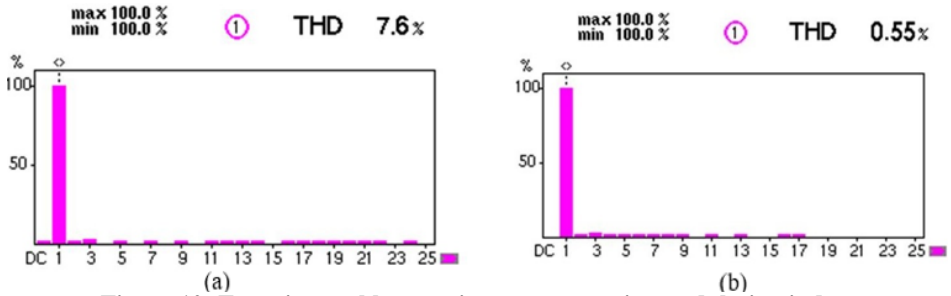


Figure 10: Experimental harmonic spectra at unity modulation index.

6 Conclusion

This work proposed a unique single-source thirteen-level inverter (SSTLI) for the application of PV sources. This topology requires fewer components (ten switches) to obtain thirteen levels and a simpler control scheme is considered for analyzing the operation of SSTLI. The SSTLI has supporting factors which include voltage balance, fewer power switches, voltage gain value, and cost-effectiveness. The sinusoidal PWM technique has been implemented for the verification of the proposed SSTLI by considering RL load. Experiment findings in a real-time simulation system using DSP are also shown to validate the presented SSTLII. This type of single-source DC-AC topology is more feasible for solar renewable energy source applications for its integration into the grid.

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Authors' Contributions

The authors confirm their contribution to the paper as follows: study conception and design: BHK, KJ; data collection: HJ, BJ; analysis and interpretation of results: BHK, AVGAM, DPK; draft manuscript preparation: BHK. All authors reviewed the results and approved the final version of the manuscript.

Competing Interests

The authors declare that they have no competing interests.

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