El Cezeri
Journal of Science and Engineering
ISSN: 2148-3736

Research Article

Investigation of PWM Methods for a 9 Level Boost Inverter Using CD-type Carriers

Sindhuja R[1a], Padma S[2b], Suresh K[3c] Parimalasundar E[4d] and Busireddy Hemanth Kumar[4e]
[1] Electrical and Electronics Engineering Department, SRM Institute of Science and Technology,Ramapuram, Chennai, India
[2] Electrical and Electronics Engineering Department, Faculty of Engineering & Technology, Annamalai University, Chidambaram, India
[3] Electrical and Electronics Engineering Department, Christ University, Banglore, India
[4] Electrical and Electronics Engineering Department, Mohan Babu University (Erst while Sree Vidyanikethan Engineering College, Tirupati, India

sindhuja.gct@gmail.com

DOI : 10.31202/ecjse.1302861
Received: 26.05.2024 Accepted: 15.01.2024
How to cite this article:
Sindhuja R, Padma S, Suresh K, Parimalasundar E, Busireddy Hemanth Kumar, " Investigation of PWM Methods for a 9 Level Boost Inverter Using CD-type Carriers", El-Cezeri Journal of Science and Engineering, Vol: 11, Iss:1, (2024), pp.(30-36).
ORCID: [a]0000-0002-7644-9272; [b] 0000-0003-3550-1756. [c] 0000-0003-3824-1304; [d] 0000-0001-6124-2685, [e] 0000-0001-6282-5102.

Abstract : The article introduces an innovative boost inverter topology that utilizes two switching capacitors and a single Direct Current (DC) source to generate a nine-level output voltage waveform. This design eliminates the need for sensors or additional electronics since the capacitor voltages automatically balance themselves. Unlike traditional inverters, an input DC boost converter isn't necessary, as the output voltage is often twice the input voltage, particularly when the inverter is powered by a natural source. Furthermore, novel modulation techniques proposed for CD-type carrier waves exhibit enhanced efficiency, higher RMS voltage, and reduced harmonic distortion (THD). The effectiveness of the suggested carriers has been verified through investigations employing phase disposition (PD), alternate phase opposition disposition (APOD), and phase opposition disposition (POD). Each technique described under 9LBI has been assessed using a MATLAB/Simulink configuration. The operational and dynamic performance of the proposed architecture has been modeled using MATLAB/Simulink.

Keywords : MLI, PWM, Efficiency, Inverter, THD

1 Introduction

The expansion of renewable energy sources (RES), such as photovoltaic (PV) and wind power, has experienced remarkable growth, particularly over the past decade. This surge is driven by a concerted effort to diminish reliance on fossil fuels and mitigate carbon emissions. In this context, multilevel voltage source inverters (MVSI) have emerged as highly promising and competitive alternatives to traditional power converters. MVSI has demonstrated its efficacy in various industrial applications, including drive systems; uninterruptible power supplies (UPS), active power filters, and other scenarios where stringent performance standards are imperative. Its relevance extends to grid integration for sustainable energy resources. The initial wave of inverters featured cascaded H-bridge converters (CHB), neutral point clamped converters (NPC), and flying capacitor converters (FC), and these were widely adopted across various industries [1]–[4].

These topologies have garnered significant attention and are frequently employed in commercial applications. However, the growing number of output levels poses a notable challenge, particularly with the increased component count demanded by neutral point clamped converters (NPC) and flying capacitor converters (FC). Similarly, cascaded H-bridge converters (CHB) encounter limitations arising from the elevated number of levels, requiring a more extensive array of distinct DC voltage sources. This, in turn, has repercussions on their applicability and restricts their range of applications [5]–[7]. This class of MLI topologies relies on multiple isolated DC voltage sources and is divided into asymmetrical and symmetrical designs. In symmetrical configurations, the magnitude of the DC voltage generators remains constant. On the other hand, in asymmetrical designs, the varying magnitude of DC voltage generators results in a higher number of levels and fewer switches, as well as a reduced quantity of DC voltage sources. However, both types of topologies face limitations in their applications due to the increased requirement for diverse DC voltage sources [8], [9].

To minimize the requirement for numerous sources of DC voltage, there has been an advocacy for switched capacitor (SC) unit designs. Various configurations of the SC unit have been implemented, leading to different output voltage values. One suggested capacitor-based architecture in this context is the Packed E-cell (PEC) topology, as detailed in [10]. The design incorporates two capacitors, two DC voltage sources, resulting in a 9-level voltage output waveform. However, it's essential to note that the design does not enhance the input voltage. In references [11] and [12], which are analogous to [10], 9-level

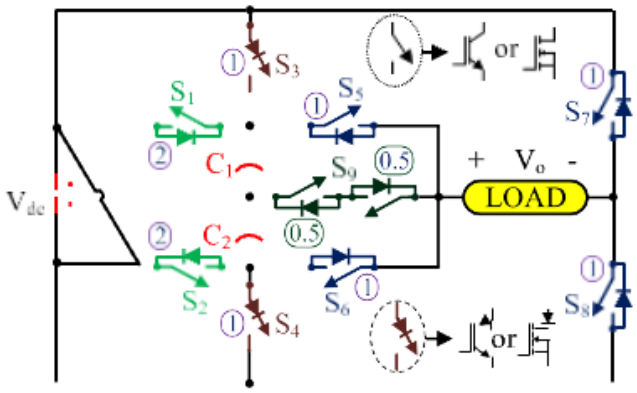

Figure 1: Topology of 9L-MLI.

Multilevel Inverter (MLI) architectures were presented, employing two capacitors and two DC voltage sources. In [13], the authors proposed two new designs featuring two sources of DC voltage and two capacitors. Each of these designs achieves 9 voltage levels across the load. Notably, an H-bridge is employed in both designs to alter polarity, requiring switches with a higher operating voltage. However, these architectures face a limitation in terms of boosting power.

Similarly, in [14], a K-type system with 13 levels of output is presented, utilizing two capacitors and two sources of DC voltage. It's worth noting that the ratings of the two capacitors may vary. The next three levels in this system also involve the discharge of both capacitors, leading to an unstable response in the capacitor voltage and uneven voltage levels across the load [15]–[17]. Carrier-based Pulse Width Modulation (PWM) is widely utilized due to its simple architecture. Commonly, carrier waves are represented by saw-tooth patterns or triangles. Modulation techniques utilizing saw-tooth and triangular carriers are prevalent among various approaches. This research presents a new carrier shape known as the CD-type carrier for PWM techniques, evaluating its effectiveness in comparison to other carrier PWMs, particularly triangular ones. The term "CD-type" is derived from the waveforms resembling the charging and discharging voltage of a capacitor [18], [19].

The primary motivation behind creating the distinctive CD-type carrier waves was to explore the impact of different carrier wave shapes on the overall PWM technique. In previous work, Al-Haddad et al. [3] introduced half-parabolic carrier patterns to leverage the redundant state for capacitor voltage adjustment, incorporating active capacitor voltage balancing into the half-parabola carrier. Another study [8] showcased an entire parabolic carrier, illustrating its positive influence on the overall quality of output waveforms. The innovative carrier signals of CD type introduced in this paper draw inspiration from these prior advancements [20]- [21]. The CD-type carrier combines the characteristics of two previously proposed carriers mentioned above. This modulation method achieves a robust root mean square (rms) voltage while minimizing harmonic content, deviating from conventional PWM techniques. This enhancement contributes to an overall improvement in the quality of generated waveforms. The proposed MLI's key characteristics are:

i. Only one DC source is employed.
ii. The capacitors achieve self-voltage balancing.
iii. Double the input voltage makes up the output voltage.
iv. Switch stress from low voltage.
v. Voltages of capacitor are unaffected by modulation index and load power factor.

2 Investigation of 9LBI Topology

2.1 Description of Voltage Levels

The configuration of the proposed single-phase 9LBI topology, along with the voltage stress over each switch (V_{DC}) depending on the supplied source of DC voltage, is illustrated in Figure **??** The assembly of the suggested topology comprises ten switches, and the choice between IGBTs or MOSFETs for these switches depends on factors such as the converter's operating frequency, voltage, and power rating. The DC supply voltage undergoes a halving process through two capacitors, C1 and C2. A systematic and sequential toggling ON/OFF of the switches maintains 50 percent of the voltage supply for the capacitor voltages (VDC/2). This proposed arrangement generates 9 levels across the load, with a voltage boosting factor twice that. The switching table for the suggested design is provided in Table 1, and Figure 2 depicts the various modes of operation.

The suggested topology creates nine levels across the load. This section specifically details the five levels during the positive half cycles, including the blocking voltages of non-conducting switches.

State 1: During the zero voltage state, connecting capacitors C1 and C2 in a crosswise manner to the source of DC voltage enables them to charge to their maximum voltage. This is accomplished by activating switches S3 and S4. In this state, the load terminals are shorted, and if an inductive load is present, a current path is established by turning ON switches S5 and S7.

Table 1: Switching Sequence for various switches

S1	S2	S3	S4	S5	S6	S7	S8	S9	V_{out}
0	1	0	0	1	0	0	1	0	2 V_{DC}
0	1	0	0	0	0	0	1	1	1.5 V_{DC}
0	0	1	1	1	0	0	1	0	V_{DC}
0	0	1	1	0	0	0	1	1	0.5 V_{DC}
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	0	-0.5 V_{DC}
0	0	1	1	0	1	1	0	0	- V_{DC}
1	0	0	0	0	0	1	0	1	-1.5 V_{DC}
1	0	0	0	0	1	1	0	0	-2 V_{DC}

State 2: In the VDC/2 potential state, achieved by turning ON S8 and S9 and turning OFF S5 and S7, the applied potential equal to VDC/2 emerges across the load. During this step, capacitor voltages VC1 and VC2 are maintained at VDC/2. In this process, a voltage equal to VDC/2 is subtracted from the DC voltage source VDC, effectively removing the capacitor voltage VC1.

State 3: VDC. Transitioning switch S5 from the off to the on position allows the entire source voltage to pass through the load in this voltage condition. Meanwhile, the capacitor voltages are maintained at VDC/2. Both capacitors store energy up to this voltage level during this phase.

State 4: 3VDC/2. In this voltage state, switches S3 and S4 are turned off, enabling the utilization of energy stored in capacitor C2 to establish the third voltage state. By turning ON switch S2, the voltage VC2 is added to the DC voltage source VDC. The potential is maintained at VDC/2, and the condition of capacitor C1 remains unchanged.

State 5: 2VDC. In this voltage state, the energy stored in both capacitors is released, and the voltages of the two capacitors contribute to the DC voltage source. The result of this increase in the DC voltage source is a potential of 2VDC across the load.

To facilitate the boost feature, a cross connection is established between switches S1 and S2, involving capacitors and the DC voltage source. This cross-connection is essential to limit the potential to 2VDC. To ensure that switches S3 and S4 do not conduct during boost mode operation, they are connected in series with diodes. Switches S3 through S8 must block the supply voltage VDC, and the bidirectional switch S9 must block fifty percent of the applied voltage.

2.2 Modulation Techniques

The research introduces several modulation techniques to control the operation of the Multilevel Inverter (MLI) circuit. This section focuses on Pulse Width Modulation (PWM) using CD-type carriers. Within the category of level-shifted modulation techniques, the proposed modulation strategy is discussed, known as Level-Shifted PWM (LS-PWM). Traditionally, there are three types of level-shifted modulation techniques:

i. Alternate Phase Opposition Disposition (APOD),
ii. Phase Opposition Disposition (POD), and
iii. Phase Disposition (PD).

The planned carriers fall into each of these three categories. To mitigate sideband overtones present in standard modulation schemes, the frequency of the carrier wave must be significantly higher than the frequency of the modulating wave. This section details the development of modified CD-type carriers as a carrier signal. CD-type carrier waves, essentially parabolic in nature, are generated through various combinations.

The modulation of pulse width (PWM) approaches significantly impacts the ripple, average, and peak quantities of the junction temperature of a device. Increased power dissipation, additional switching, or imbalanced losses due to uneven gate pulses can contribute to thermal stress in devices. Elevated thermal stress can expedite the deterioration of power devices, potentially leading to permanent damage to the inverter. A recent development for single-phase Multilevel Inverters (MLI) is dual pole clamped PWM using a two-loss balancing approach.

The process of generating the CD-type wave involves leveraging both sinusoidal and pulse functions, as visually explained in Figure 3. Block-C is responsible for creating the first half of the CD wave, mimicking the capacitors' voltage waveform during the charging phase. This is achieved by summing the product of the pulse function and the modulus of a sinusoidal function. Moving to Block-D, this section generates a portion of the CD wave that mirrors the shape of the capacitors' voltage waveform during the discharging mode.

To delve into more detail, the following formulas were employed in these blocks to produce the final carrier wave of CD type, as illustrated in the accompanying Figure 3. The intricacies of these formulas capture the essence of the waveform generation process and the interplay between sinusoidal and pulse components.

The creation of sinusoidal functions involves using the pulse and carrier wave of CD type. By taking the component of the sine wave up to 90 degrees, the signal x(t) has been generated. The function y(t) is produced by time-shifting the pulse and scaling the shifted pulse component by a sinusoidal function. Consequently, 1 is added to y(t).

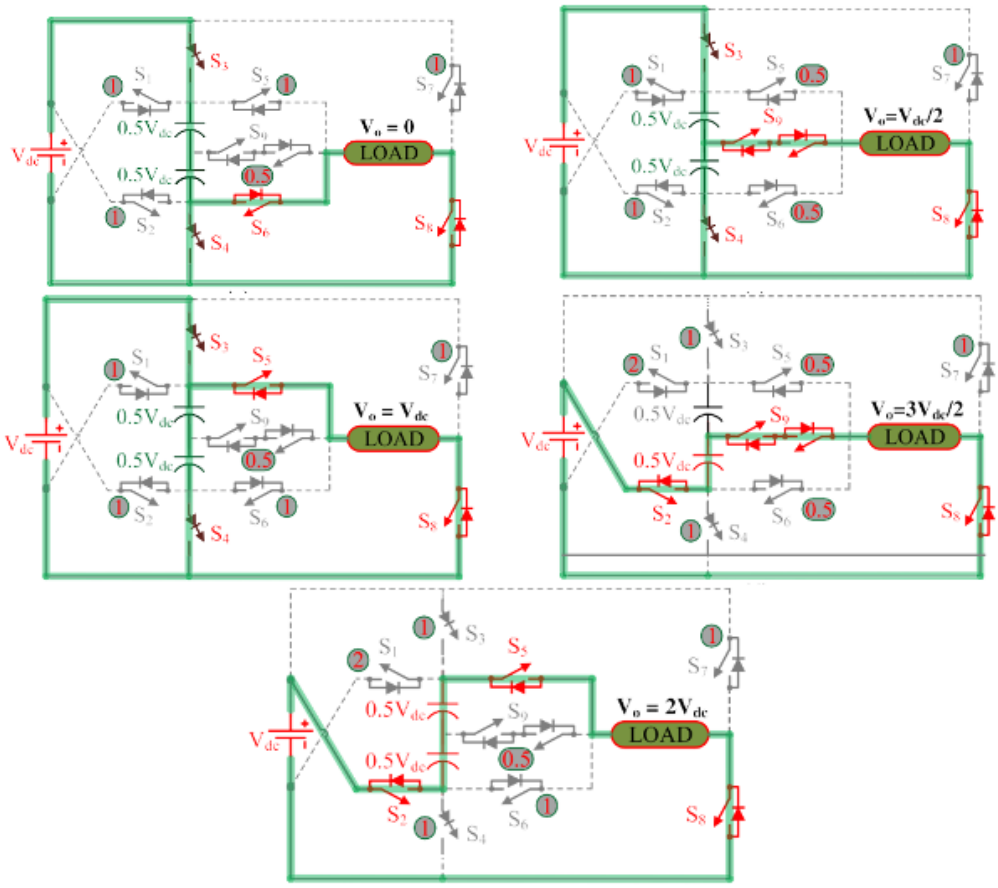

Figure 2: Modes of Operation for various levels of output

$$x(t) = |\sin(t)|\, u(t) - |\sin(t)|\, u(t - \frac{\pi}{2}) \tag{1}$$

$$y(t) = [-|\sin(t)|\, [u(t) - u(t - \frac{\pi}{2})]] \tag{2}$$

$$z(t) = 1 + y(t - \frac{\pi}{2}) \tag{3}$$

The discharge wave has a frequency that is twice as high as the targeted carrier frequency due to factors (1), (2), and (3). To reduce the frequency, another pulse function with a frequency double that of the sinusoidal function is employed.

$$a(t) = [z(t)][u(t) - u(t - \frac{\pi}{2})] \tag{4}$$

Equation (4) is the carrier wave of CD type that generates eight carriers with vertical shifts. After generating one carrier wave, eight carrier signals are produced, each needed to generate nine levels with identical shapes but with a level shift of 0.5. These carriers, labeled L1 to L8, are CD-type carriers with an operating frequency equivalent to the standard sinusoidal signal's natural frequency. By comparing Vref with the carriers L1 to L8, the firing signal for each carrier is determined, and the corresponding pulses are 2VDC, 1.5VDC, VDC, VDC, 0.5VDC, 0, -0.5VDC, -VDC, -1.5VDC, and -2VDC.

Figure 4 illustrates the CD-type carriers alongside the sinusoidal wave, serving as a reference signal with a natural frequency of 50 Hz. In all four cases, the magnitude of each level-shifted carrier is 0.5. The carrier wave itself has a frequency of 4000 Hz, generating a total of eight vertically shifted carrier waves with a magnitude of 0.5.

3 Outcomes of Simulation and Discussion

The utilization of MATLAB/Simulink tools facilitated the thorough modeling of the proposed 9-level structure, as visually represented in Figure 5. The detailed simulation outcomes, capturing various waveforms pertinent to this proposed structure, are presented in Figure 6. To provide a specific illustration, when subjecting the system to an AC voltage output with a peak level

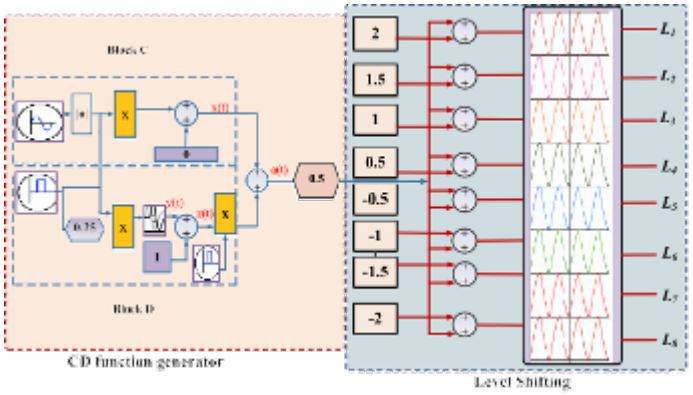

Figure 3: Generation of CD type carrier waves

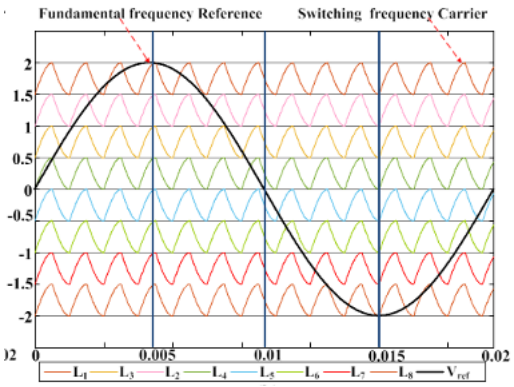

Figure 4: Generated PWM pulse pattern.

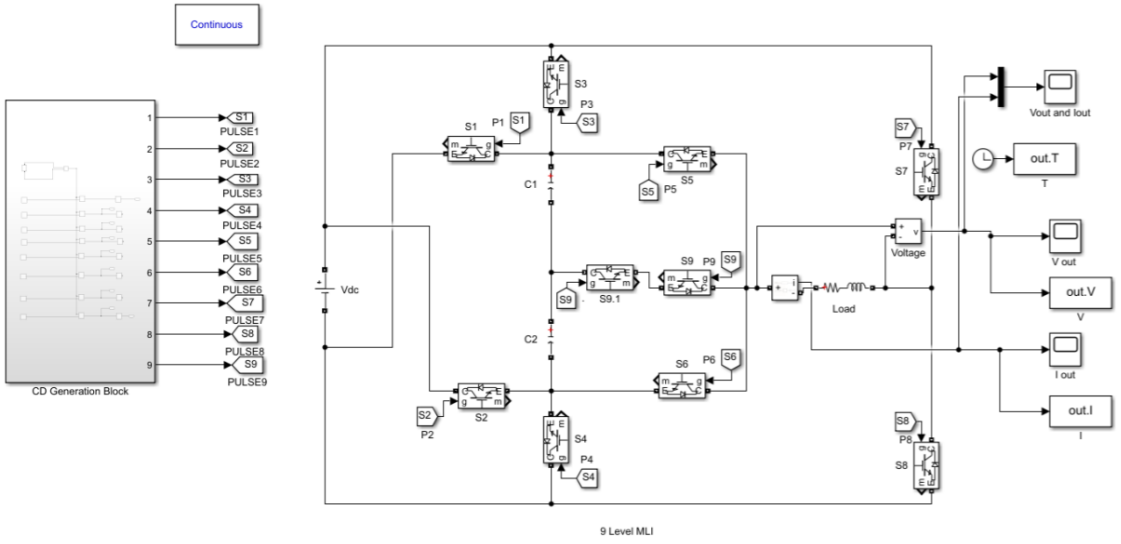

Figure 5: MATLAB Simulation File.

of $200V$ applied to a series-connected RL load (defined by $Z = 50mH + 20$), the resultant output current attains a peak level of $7.5A$. Figure 7 further elucidates the dynamic interplay of current and voltage output waveforms, specifically highlighting the response when substituting an RL load with $Z = 50mH + 50$ for a purely resistive load characterized by $Z = 50$.

The balanced nature of both capacitor voltages remains unaffected by changes in load type, affirming that the load type exerts no influence on capacitor voltage balancing. A voltage range of 50V is observed across both capacitors, with minimum and maximum values measured at 45V and 51V, respectively. Furthermore, Figure **??** provides insight into the Fast Fourier Transform (FFT) of the voltage output, revealing a Total Harmonic Distortion (THD) of 9.41% after the removal of all lower-order harmonics. This underscores the effectiveness of the system in maintaining a balanced capacitor voltage and relatively low harmonic distortion in the output voltage.

The performance metrics of the proposed architecture are depicted in Fig. 8, showcasing the changes in capacitor ripple voltage and Total Harmonic Distortion (THD). It is observed that as the power output increases, the ripple voltage of the capacitor also rises. This increase in ripple voltage has a discernible impact on the voltage output waveform, leading to a slight degradation in THD. To elaborate, with no load, the THD is measured at 9.2%, and as the power output reaches 2 kW, it experiences a modest increase to 9.7%. These metrics provide valuable insights into the behavior of the system under varying power output conditions.

The effectiveness of the proposed architecture has been further assessed by introducing a significant change in load and a modulation index (MI). Figure 9 illustrates a dynamic modification of the modulation index, transitioning from 1.0 to 0.6 and then from 0.6 to 0.4. This alteration results in a reduction in the number of levels, first to 7 levels with a modulation index around 0.6 and subsequently to 5 levels with a modulation index of 0.4. Notably, despite these changes, both capacitor voltages remain balanced. This analysis provides valuable insights into the robustness and adaptability of the proposed architecture under varying load and modulation conditions

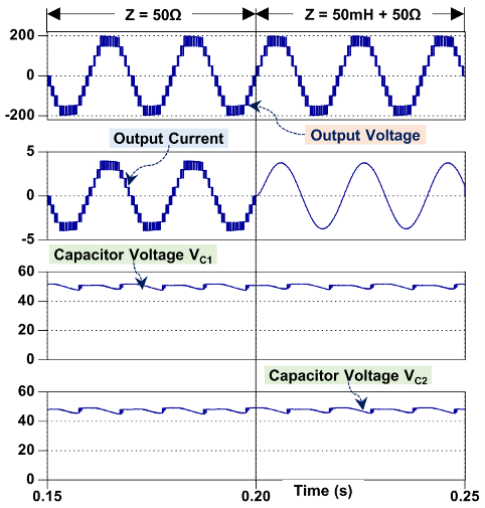

Figure 6: Output Voltage & Current waveform across Load and Capacitor voltage.

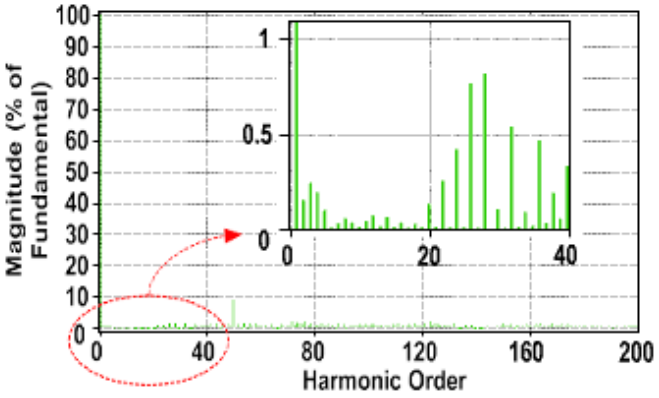

Figure 7: FFT Spectrum of Output Voltage Waveform.

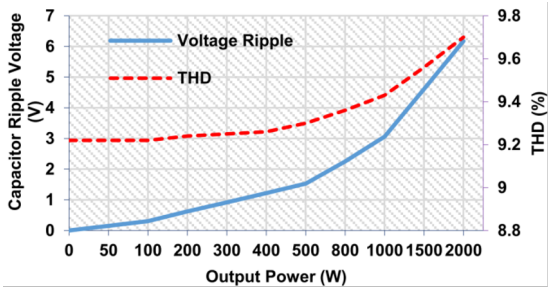

Figure 8: Variation of THD and Capacitor Ripple voltage with respect to Output Power.

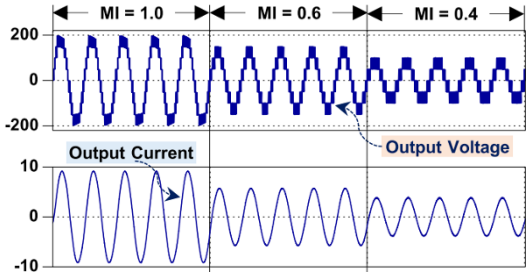

Figure 9: Output Voltage and Current Waveform for change in MI.

4 Conclusions

The comprehensive comparison study emphasizes the potential of the proposed topology, showcasing its ability to achieve the same number of voltage levels with fewer components. This reduction in components translates to a lower cost for the topology, which utilizes a single DC voltage source to attain nine levels. The efficiency of this approach is underscored by the cost-effectiveness it brings to the table. The introduced CD Type PWM method plays a pivotal role in enhancing waveform quality and substantially reducing harmonics. Of particular note is the distinctiveness of the proposed PWM approach, standing out for its minimal component requirement, cost-effectiveness, and heightened effectiveness. These features position it as particularly suitable for applications in low and medium voltage scenarios. The viability of the suggested topology is not only theoretically sound but also confirmed through numerous observed outcomes under various loading conditions. The abundance of simulation results serves to further validate the improved converter performance achieved by the proposed technique.

Acknowledgment

This work was supported by Sree Vidyanikethan Educational Trust (SVET), Tirupati, Andhra Pradesh, India.

Competing Interests

The authors declare that they have no competing interests.

Authors Contributions

The authors confirm contribution to the paper as follows: study conception and design: SR, PS; data collection: SR, SK; analysis and interpretation of results: PE, BH; draft manuscript preparation: SR. All authors reviewed the results and approved the final version of the manuscript.

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