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Research Article

Design of low power DTMOS based FCS and its notch filter application for ECG signals#

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Notch Filter
Powerline Interference
Electrocardiograph

Abstract: In this study, p-MOSFETs in floating current source circuit are converted to dynamic threshold voltage MOSFET structure and a second order notch filter application is carried out by using the DTMOS based FCS circuit. The proposed model is simulated in LTSPICE simulator by using Taiwan Semiconductor Manufacturing Company 0,18µm CMOS technology. DTMOS structure allows the operation of the circuit at lower power about 4,95nW. Operating frequency of notch filter consisting of the DTMOS-FCS circuit is set up to suppress the undesirable effects of power-line interference on the electrocardiograph signals.

1. Introduction

Electrocardiograph (ECG) signals are exposed to distortion by several noise sources such as electric power system and recording electrodes [1, 2]. And power-line interference (PLI) (centered at 50/60 Hz) is a major problem during the recording of the ECG signals. Therefore, suppression of the PLI components from the ECG signals is required. This suppression can be executed via different types of notch filters [2, 3].

On the other hand, advances in technology lead to increase the demand for low power consumption and lower dimensional devices. Low power applications are provided at lower dimensional devices. By this way, decreasing channel length gives rise to the leakage current problems. In order to minimize leakage currents, threshold voltage cannot be held below a certain limit in regular MOSFETs [4, 5]. As a result, dynamic threshold voltage MOSFET (DTMOS) structure offers an opportunity for ultra low voltage applications [6, 7].
Floating Current Source structure has been firstly proposed as output stage of current-mode feedback amplifier (CFA) [8]. Some benefits of this structure are as follows; succession of output currents for any input, unaffected by transistor matching, low total harmonic distortion [8]. All of these benefits show that FCS isn't only an output stage for CFA but also takes place in various studies such as non-feedback differential amplifier, full-wave rectifier, negative second generation current conveyor, and filter operation [9-12].

In this study, p-MOSFETs in FCS circuit are converted to DTMOS. In addition, a second order notch filter is constructed using the DTMOS-FCS circuit, and the proposed filter circuit can be used to suppress the PLI components from the ECG signals.

2. DTMOS Structure

Regular MOSFETs are converted to DTMOS by connecting the bulk and gate in standard CMOS manufacturing process [6, 7]. DTMOS structure and its circuit symbol are shown in Figure 1. As mentioned in previous section, DTMOS structure allows ultra low power applications. This is achieved by applying forward bias to body-source junction in order to reduce threshold voltage (V_{TH}) of DTMOS (Equation-1) [6, 7]. By reduction of threshold voltage, inversion charge (Q_N) is increased

(Equation-2). So, larger inversion charge leads to a higher current drive in DTMOS in comparison to the regular MOSFETs [6, 7].

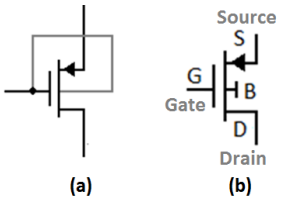

Figure 1. *(a) The structure of DTMOS and (b) its circuit symbol [5].*

$$V_{TH} = 2\Phi_B + V_{FB} + \gamma\sqrt{2\Phi_B - V_{BS}} \quad (1)$$

where γ is the body effect parameter. V_{FB} and V_{BS} represent the flat band voltage and bulk to source voltage, respectively. Φ_B is inversion layer potential.

$$dQ_n = C_{OX}\left(dV_G - \frac{dV_{TH}}{dV_G}dV_G\right) \quad (2)$$

where C_{OX} is the oxide capacitance and V_G is the gate voltage.

3. DTMOS based FCS Circuit

FCS circuit possesses two input and two output stages as shown in Figure 2. And the circuit includes two PMOS and two NMOS devices. The most important feature of this structure is to following of the output currents each other with a phase angle difference of 180 degrees [8]. By using Kirchoff Current Law, it can be seen that output currents follow each other:

$$I_{B1} - I_{B2} - (I_{OutN} + I_{OutP}) = 0 \quad (3)$$
$$I_{B1} = I_{B2} = I \quad (4)$$
$$I_{OutN} = -I_{OutP} \quad (5)$$

where I_{B1} and I_{B2} represent bias currents.

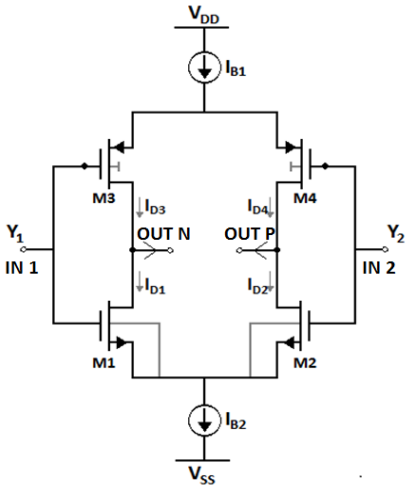

Figure 2. *The circuit of DTMOS based FCS.*

4. Second Order Notch Filter

In order to suppress the PLI components from the ECG signals, the notch filter [13] seen in Figure 3 is utilized. The notch filter is constructed using DTMOS based FCS circuit. Transfer function (H) and quality factor (Q) equations of the notch filter are as follows [13]:

$$H_{bandstop}(s) = \frac{s^2C_1C_2 + g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}} \quad (6)$$

$$Q = \frac{\sqrt{C_2g_{m1}}}{\sqrt{C_1g_{m2}}} \quad (7)$$

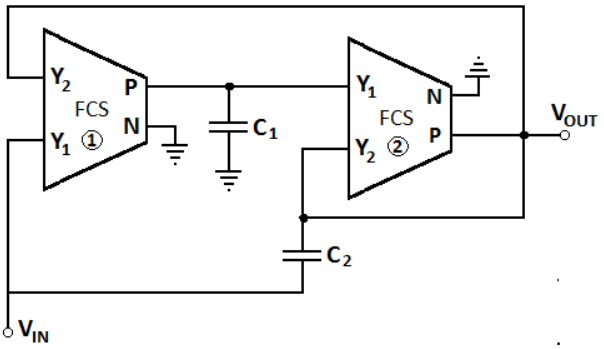

Figure 3. *DTMOS-FCS based second order notch filter [13].*

5. Second Order Notch Filter

The proposed model is simulated in LTSPICE simulator by using TSMC 0,18µm CMOS technology. Voltage sources, bias currents, and input voltage are chosen as given in Table 1 and aspect ratios of the transistors are given in Table 2.

Table 1. *DTMOS-FCS Circuit Parameters.*

Parameters	Values
Voltage Sources	V_{DD} = -V_{SS} = 0,15V
Bias Currents	I_{B1} = I_{B2} = 16,5nA
Input Voltage (AC)	V_{IN} = 0,03V_{AC} (1 kHz)

Table 2. *Aspect Ratios of MOSFETs.*

MOSFETs	Aspect Ratios (W/L)
M1 – M2	300µm/2µm
M3 – M4	5µm/2µm

Simulation results of the proposed model are shown in Figure 4 - 7. DC analysis and AC analysis of DTMOS-FCS circuit can be seen in Figure 4 and Figure 5. Output currents follow each other with phase angle difference of 180° as expected from the characteristic equation. For AC analysis, power consumption is calculated as 4,95nW. In addition, transconductance is observed as 231,289nΩ^{-1} (Figure 6) and it can be said from Figure 6 that the filter circuit can be used for approximately 20kHz bandwidth.

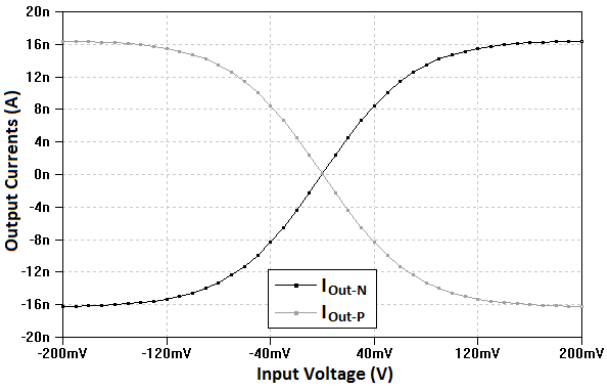

Figure 4. *The DC transfer characteristics of DTMOS-FCS circuit.*

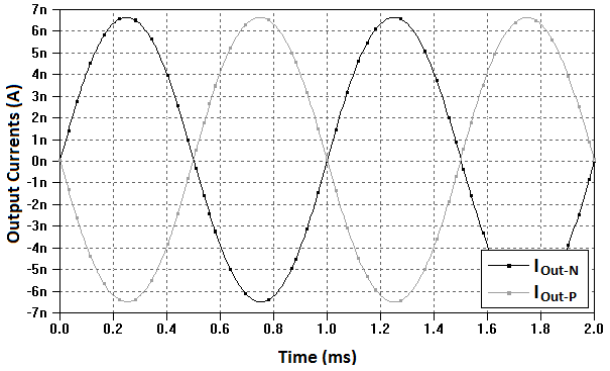

Figure 5. *The output currents of DTMOS-FCS circuit.*

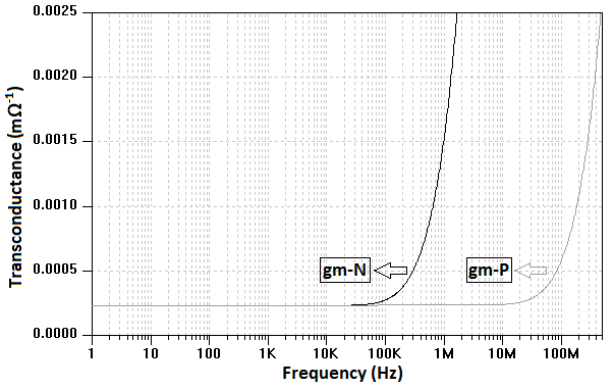

Figure 6. *The transconductance of DTMOS-FCS circuit.*

5.1. Notch Filter Application of DTMOS-FCS Circuit

The proposed notch filter is operated by using simulator and the frequency response of the filter is given in Figure 7. Capacitor values of the proposed filter are adjusted to reach the interference frequency. Capacitor values are chosen as; C_1 = 210pF and C_2 = 2100pF. By means of Equation 7, Q parameter of notch-filter is calculated as 3. Total harmonic distortion is obtained about 0,12%. Operating frequency of the filter is about 55Hz that is located at frequency range of PLI. Thus, it can be said that this structure can be used to suppress PLI components.

Moreover, it can be inferred from Figure 7 that DTMOS structure also allows to operate at lower frequencies. In the FCS circuit, that doesn't include DTMOS, it will be required higher value capacitances to reach the interference frequency.

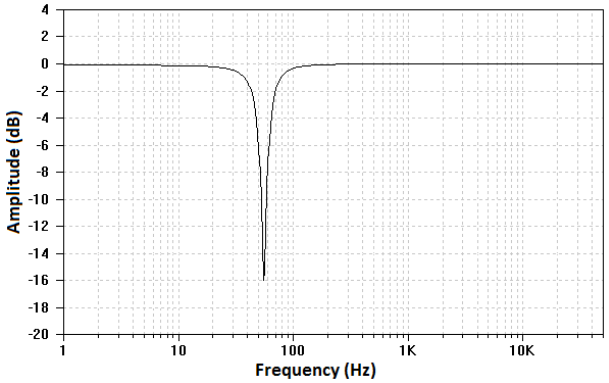

Figure 7. *The response of DTMOS-FCS notch filter.*

Conclusions

In the conclusion, DTMOS based FCS circuit has low power consumption as 4,95nW and its second order notch filter application is suitable to suppress the power line interference which is a major problem for the ECG signals. It can be said that DTMOS based FCS structure is favourable in terms of lower power consumption and dimension considerations in integrated circuits.

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