MOS-ONLY AUTOMATION TECHNIQUE WITH AN EXEMPLARY MOS-ONLY BP/LP AGILE FILTER DESIGN

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Abstract: *In this work, a systematic of the automation in the result of the re-obtained small signal parameters based on SPICE and CADENCE-SPECTRE is presented for MOS-Only circuits. Accuracy of the re-obtained parameters was improved by re-formulating in the basis of SPICE and CADENCE-SPECTRE. Moreover, piece-wise polynomial regressive models are presented for* g_{ds} , g_m *and* I_{ds} *. Also, performance of the models is compared with conventional expressions. Success of the given MOS-Only design automation based on re-obtained small signal parameters is verified with an exemplary new agile filter.*

Keywords: *MOS-Only, polynomial, SPICE, CADENCE-SPECTRE*

1. Introduction

MOS-Only circuit design has been gaining big importance due to the fact that it doesn't necessitate large chip area. The most important requirement of the MOS-Only design is to understand physical properties and operating mechanisms of the basic components in electronics. Furthermore, in Very Large Scale Integrated (VLSI) circuit design, a great deals of circuits have been sized by hand-calculations and iteratively chain of computations. In this point of view, there is a wide gap for design automation proposals, which incorporates knowledge and experience of designer and re-formulation of the conventional equations in this area. As a result, different algorithms or methods are arisen from this urgent demand and rapidly growing of VLSI technology. In the literature, analog design automation is an active research area, so that a couple of studies, which are convex optimization based [1]-[3] and utilized from genetic algorithm [4] were developed. Especially, convex optimization based methods bring much more efficient computations than others due to the fact that they present globally optimum solution and robust technique for a wide range of applications. However, this requires cost functions and basic equations to be posynomial and/or monomial format [5]-[9]. Therefore, it reduces computational accuracy. On the other hand, convex optimization based algorithms generally include a chain of computations, which bring long computational time. It can be said that this aspect is another significant drawback of these methods.

Gain and speed of the circuit were included in main design parameters in [10]-[12] by using convex optimization. Furthermore, these studies bring new design equations, which are independent of technological parameters. Although they present much more powerful solutions than others with regard to Monte-Carlo simulations, these spend much more computational time and effort than other primitive methods. So, they are inefficient proposals for small and compact circuits such as MOS-Only schemes. In this point of view, we are unaware of any design automation method for MOS-only circuits except for [13]. As a result, this work is improved version of [13] with regulated design equations. Also, this paper is significantly extended version of [14] presented in ELECO-2016 with a large number of simulations such as Monte-Carlo and Total Harmonic Distortions (THD) of the circuits. In addition to that, design constraints of the exemplary circuit in [14] are changed and their performances are proved with those simulations.

2. Proposed Automation Method

When Figure.1 is considered, conventional analog circuit design lacks of efficient formulations of C_{gs} and C_{gd} , which only incorporate simulation results and effect of the design parameters in the saturation region. Conventional approach of these capacitances is as follows:

$$C_{gs} \approx \frac{2}{3} C_{ox} WL \qquad C_{gd} \approx 0 \tag{1}$$

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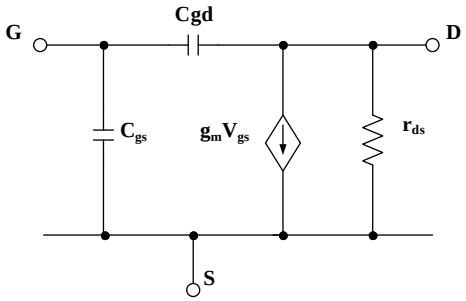


Figure 1. MOSFET small signal equivalent circuit ($V_{BS}=0$)

However, this approach does not include V_{DS} and V_{GS} effects on these parameters. In this view, C_{gs} and C_{gd} are modelled by using SPICE and CADENCE-SPECTRE simulations with approximately 350 and 400 points respectively. Moreover, C_{ds} and other bulk capacitances are not taken into account in this work due to the fact that they are 50-100 times smaller than C_{gs} and C_{gd} in high frequency applications. In this respect, polynomial regression and linear interpolation techniques are applied to the simulation based data in order to model C_{gs} and C_{gd} as shown in Figure.2 and Figure.3. They can be evaluated as follows:

$$C_{gs} \approx 0.66*W(k_1+k_2L+k_3V_{GS}+k_4V_{GS}L+k_5{V_{GS}}^2) \quad (2)$$

$$C_{gs} \approx 0.66*W(m_1+m_2L+m_3V_{DS}+m_4V_{DS}L+m_5{V_{DS}}^2) \quad (3)$$

$$C_{gd} \approx 0.312*W(n_1+n_2L+n_3V_{DS}+n_4LV_{DS}+n_5{V_{DS}}^2+n_6L{V_{DS}}^2 + n_7{V_{DS}}^3+n_8L{V_{DS}}^3+n_7{V_{DS}}^4) \quad (4)$$

$$L \in [0.18,1.2],\ W \in [2,600] \text{ in } \mu\text{m}$$

In here, (3) is used for constant V_{GS} cases. These cases occur in the design automation cycle when designer wants to keep V_{GS} constant while V_{DS} voltages of the transistors change. It affects automation flow but keeps computational simplicity. Moreover, 'k', 'm' and 'n' are regression constants with different units and they have different values for pmos and nmos devices.

Other disadvantage of the conventional design approach comes from g_m and g_{ds} calculation as shown in (5) and (6). They explicitly lack of fundamental design parameters' effects and also brings strongly dependence on technological parameters' information, which are not known exactly.

$$g_m \approx \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)I_D} \quad (5)$$

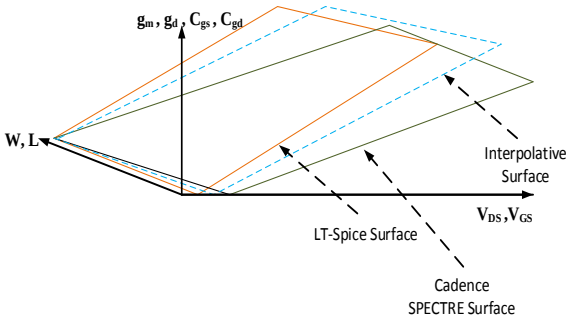


Figure 2. Relaxation of the simulation based data, which is obtained from polynomial fitting to the SPICE and CADENCE-SPECTRE [13].

$$g_d \approx \lambda I_D \quad (6)$$

In this regard, (5) and (6) are re-formulated based on SPICE simulations by considering V_{DS} and V_{GS} effects as they can be observed in (7) and (8):

$$g_m \approx W\left(\begin{array}{l}\left(\sum_{i=0}^{n=2}\sum_{j=0}^{m=2}p_{k,i,j}L^i{V_{GS}}^j\right)+\left(\sum_{i=0}^{n=1}p_{k,3i,3-3i}L^{3i}{V_{GS}}^{3-3i}\right)\\ +\left(\sum_{i=0}^{n=1}p_{k,4i,4-4i}L^{4i}{V_{GS}}^{4-4i}\right)+\left(\sum_{i=0}^{n=1}p_{k,2i+1,3-2i}L^{2i+1}{V_{GS}}^{3-2i}\right)\end{array}\right) \quad (7)$$

$$a = \text{linspace}(0.1,1.8,5)\ ,\ a(\text{k}) < \text{V}_{\text{DS}}(\text{k}) \le a(\text{k+1})$$

$$L \in [0.18,1.2],\ W \in [2,600]\ \mu m\ \text{k} \in [1,4]$$

In these calculations, V_{DS} effect is taken into consideration by splitting rail to rail V_{DS} voltage to the 4 regions. It can be shown that this type of piece-wise model improves computational accuracy as observed in [8]. Furthermore, g_{ds} can be re-obtained in the same way as follows:

$$g_{ds} \approx W(c_{i1}+c_{i2}V_{DS}+c_{i3}V_{GS}+c_{i4}{V_{DS}}^2+c_{i5}V_{GS}V_{DS}+ c_{i6}{\text{V}_{\text{DS}}}^3+c_{i7}{\text{V}_{\text{DS}}}^2\text{V}_{\text{GS}}+c_{i8}{\text{V}_{\text{DS}}}^4+c_{i9}{\text{V}_{\text{DS}}}^3\text{V}_{\text{GS}}) \quad (8)$$

$$b = \text{linspace}(0.18,1.2,11)\ ,\ b(\text{i}) < L(\text{i}) \le b(\text{i+1})$$

$$L \in [0.18,1.2],\ W \in [2,600]\ \mu m\ i \in [1,10]$$

In here, simulation based data between 400-500 samples are used to re-formulate g_m and g_{ds} to construct new equations directly dependent on design parameters as shown in Figure.4. Under these approaches, calculated values and simulation results are compared by taking into account [8] and [9] for 300 samples in Table.1. In the table, conventional approach, which is used in hand-calculations contains (1), (5) and (6) equations.

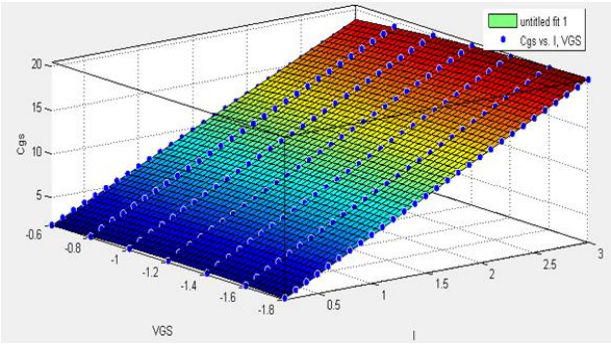


Figure 3. C_{gs} variaton vesus L (channel length) and V_{GS}. (Dots are linear interpolation of the SPICE and CADENCE results, whereas colored scheme is polynomial fitted surface. In here, device is pmos, C_{gs} in fF and W=2μm) [13].

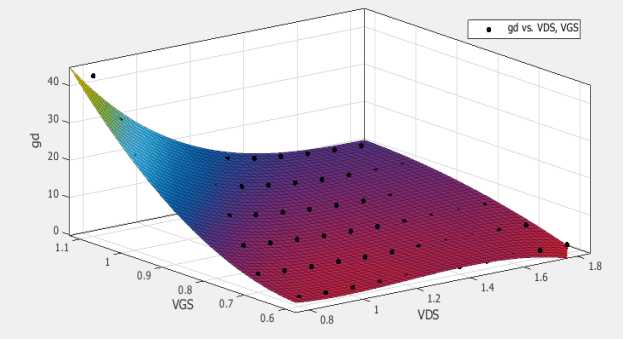


Figure 4. g_{ds} variaton vesus V_{DS} and V_{GS}. (Dots are linear interpolation of the SPICE and CADENCE results, whereas colored scheme is polynomial fitted surface. In here, device is nmos, g_{ds} in μm, L=0.3 μm W=2μm) [13].

As for Figure.5 and MOS-Only automation flow, it starts to design the circuit with random generation of the NETLIST. NETLIST describes connections of the devices in which designer is interested. The generated NETLIST is given to the input of DC and AC analyzer. DC characteristics of the circuit define conditions and equations such as saturation conditions, branch currents and node voltages. AC analyses are realized by extracting transfer function, center frequency, quality factor and different additional parameters of the circuit. Resulting circuit is sent out to the next block. It is sized by automation flow with aforementioned polynomial regressive small signal parameters. If that dimensioned circuit outperforms the constraints (Q, f_0, A_v , Z_{in}, Z_{out} *etc.*), it goes into the next step to construct its bias circuitry. Unless, final performance metrics of the circuit pass the cost function and constraints' test, dimensioning will be repeated.

3. Simulation Results

MOS-Only design automation flow is realized in MATLAB using Intel i5, 2.4GHz PC. Automation parameters are constructed with BSIM3v3 and BSIM4 models based on 0.18μm TSMC CMOS technology. In this respect, an exemplary agile filter structure, which is illustrated in Figure.6 is produced by using aforementioned automation cycle. Meanwhile, synthesis time of this kind of circuit in the end of automation is typically measured as a couple of minutes after netlist generation containing specific functionality.

Agile filter methodology is given in Figure.7. This structure is proposed in [15] and investigated in detail. In the literature, a great deals of agile filter structures are presented based on [15]. [16]-[20] present different agile schemes based on VDTA and CDTA or different topologies. In this work, a novel MOS-Only agile filter is proposed as exemplary structure for our automation algorithm. This circuit differs from others in many regards such as it can be safely tuned up to 500 MHz and it consists of only MOSFET devices without any external components. Furthermore, 'M_ext' is used as MOS-capacitor and connecting different sized MOS-capacitors with any switching system can safely change quality factor of the

Table 1. Mean Error Comparison in Small Signal Parameters' Calculation

Small Signal Parameters (Unit)	Mean Error in Conven-tional Approa-ch(%)	Mean Error in This Work (%)	Mean Error in [8] (%)	Mean Error in [9] (%)
$g_m(\mu S)$	33	3	3.5	1.2
C_{gs}(fF)	46	2.1	-	-
C_{gd}(fF)	-	1.3	-	-
$g_d(\mu S)$	40.6	3.15	24.5	10.1

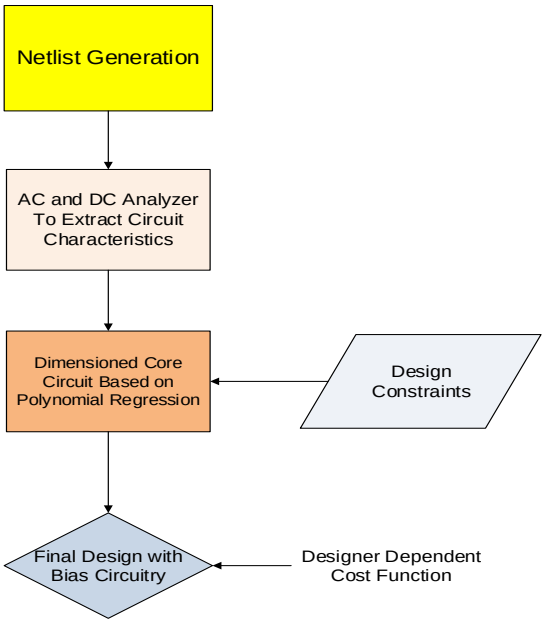


Figure 5. Proposed design automation flow for MOS-Only circuit

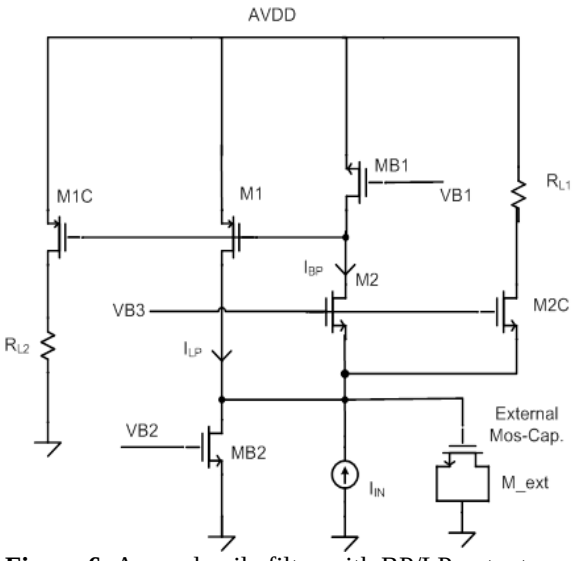


Figure 6. A novel agile filter with BP/LP outputs as an examplary circuit produced by proposed MOS-Only design automation flow

filter. In the end, to diversify our automation synthesis outputs, different designs from [14] are presented in this work and tabulated in Table 2. and 3. In addition to BP/LP outputs of the filter, channel length of the M2 can be changed in order to realize agility as illustrated in Figure.7.

$$\frac{I_{BP}}{I_{IN}} = -\frac{C_{gs1}g_{m2}s}{g_{m2}g_{m1}+C_{gs1}g_{m2}s+C_{gs1}C_{gs2}s^2} \quad (9)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{g_{m1}g_{m2}}{g_{m2}g_{m1}+C_{gs1}g_{m2}s+C_{gs1}C_{gs2}s^2} \quad (10)$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \ , \ Q = \sqrt{\frac{C_{gs2}g_{m1}}{C_{gs1}g_{m2}}} \quad (11)$$

Above equations enumerated between (9)-(11) are extracted from AC equivalent circuit in Figure 8. Overall bandpass function is given in (12) by considering all of parasitics of the core devices (M1 and M2) in Figure 6. Proposed MOS-Only circuit design flow is realized by considering all of these parasitics.

$$\frac{I_{BP}}{I_{IN}} = -\left(\frac{C_{gd1}C_{gd2}r_{ds1}r_{ds2}s^2 - (C_{gs1}r_{ds1} + C_{gd1}g_{m2}r_{ds1}r_{ds2} + C_{gs1}g_{m2}r_{ds1}r_{ds2})s}{c+bs+as^2} \right) \quad (12)$$

$$a = r_{ds1}r_{ds2}(C_{gd1}C_{gd2}+C_{gd1}C_{gs2}+C_{gd1}C_{gs1} + C_{gd2}C_{gs2}+C_{gs1}C_{gs2}) \quad (13)$$

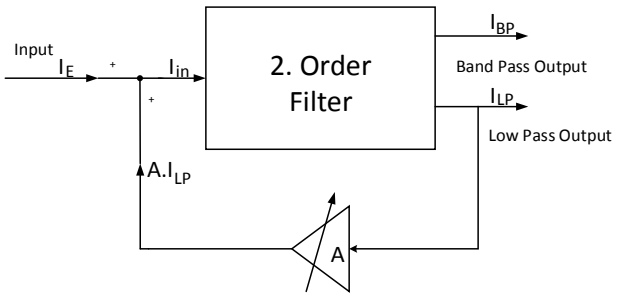


Figure 7. A second order current mode agile filter whose center frequency can be controlled by lowpass to input feedback [15]

$$b = C_{gd1}r_{ds2}+C_{gd2}r_{ds1}+C_{gd2}r_{ds2}+C_{gs1}r_{ds1} + C_{gs1}r_{ds2}+C_{gs2}r_{ds1}+C_{gd1}g_{m1}r_{ds1}r_{ds2} + C_{gd2}g_{m2}r_{ds1}r_{ds2}+C_{gs1}g_{m1}r_{ds1}r_{ds2} \quad (14)$$

$$c = 1+g_{m1}r_{ds1}+g_{m1}g_{m2}r_{ds1}r_{ds2} \quad (15)$$

Table.2 and Table.3 tabulates performance of the proposed design flow in comparison with CADENCE-SPECTRE and SPICE simulations. Small difference between simulators and proposed method comes from ignorable parasitcs of the bias circuit. Meanwhile, bias circuit of the designed filter at the output of design automation flow is dimensioned by obtaining bias currents. Bias currents are re-formulated by using aforementioned polynomial regressive context in order to catch high accuracy. In conventional formulation of the square law in I_{ds} brings high calculation error in comparison with simulations over 40%. Owing to the fact, I_{ds} is re-obtained based on design parameters as follows:

$$I_{DS} \approx \frac{W}{L}(d_{i1}+d_{i2}V_{GS}+d_{i3}V_{GS}{}^2+d_{i4}V_{GS}{}^3+d_{i5}\mathrm{V_{GS}}{}^4) \quad (16)$$

$$a = \mathrm{linspace}(0.1,1.8,5)\ ,\ a(\mathrm{k}) < \mathrm{V_{DS}}(\mathrm{k}) \le a(\mathrm{k+1})$$

$$L \in [0.18,1.2],\ W \in [2,600]\ \mu m\ \mathrm{k} \in [1,4]$$

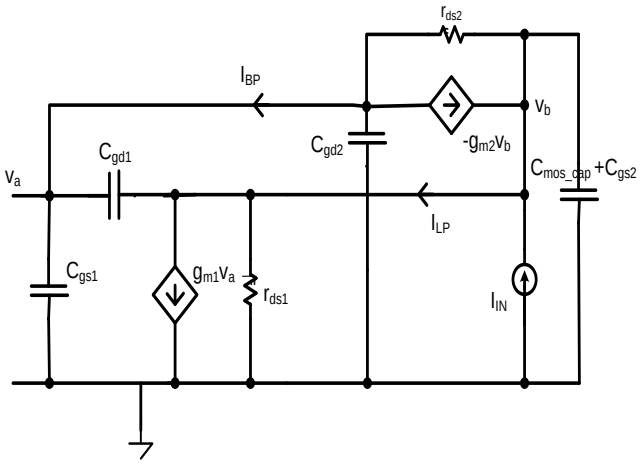


Figure 8. AC equivalent circuit of the core structure in Figure.7

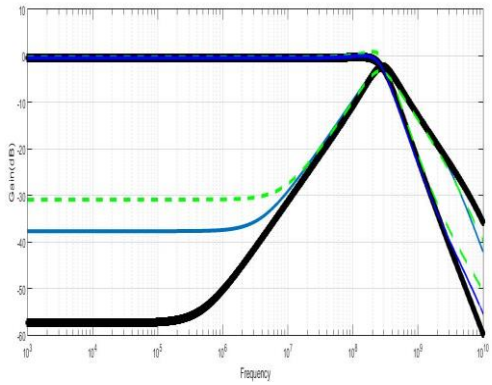
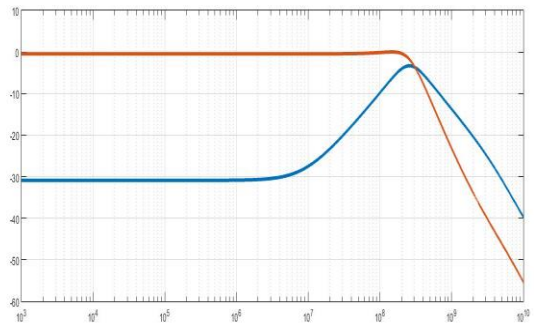


Figure 9. Proposed agile filter's frequency responses (dashed green—CADENCE, blue and thin—SPICE, black and thick—automation result)

In Figure.9, automation result is compared with SPICE and CADENCE results. In frequency domain, it can be seen that LP and BP results are in a good agreement. Moreover, Figure.10 shows frequency responses of the design 1 and 2 whereas filters have good agility as shown in c of Figure.10. To prove performances of the design 1 and 2 THD and Monte-Carlo simulations are given as well.

Table 1. Comparison Between Proposed MOS-Only Design Automation Algorithm and Simulations

Device Specs (DESIGN 1)	LT-Spice	Cadence-SPECTRE	This Work
f_0 > 200MHz	256MHz	257MHz	288MHz
Q > 0.8	0,83	0,8	0.9
Power < 500µW	460µW	450µW	485µW
Area < 400 µm^2	-	145µm^2	336µm^2
Transistor Dimensions	M1 W=35µ, L=0.18µ M2 W=6µ, L=0.72µ MB1 W=2µ, L=0.18µ MB2 W=18µ, L=0.18µ M1C W=35µ, L=0.18µ M2C W=48µ, L=0.72µ M_ext W=100µ, L=1.2µ VB1=1.15V, VB2=0.58V, VB3=0.8V		



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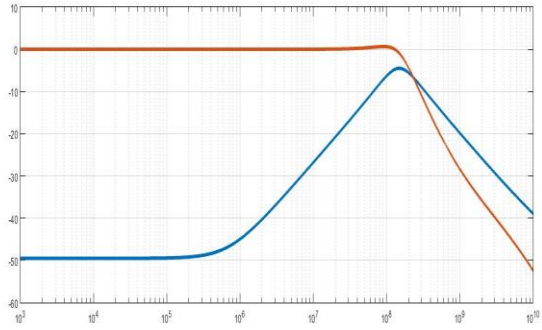

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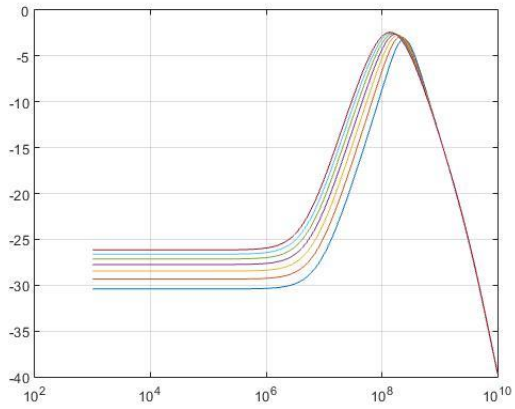


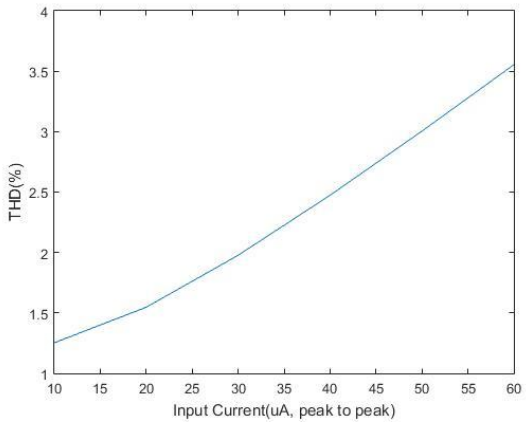
c)

Figure 10. Proposed examplary agile filter's frequency response (blue one-BP, red one LP) a) Design 1, b) Design 2, c) Agility of the filter by changing M2's channel length

Figure.11 depicts THD performance of the examplary designs. THD result is very acceptable up to 60 µA peak to peak input current bound for the proposed circuits.

Table 2. Comparison Between Proposed MOS-Only Design Automation Algorithm and Simulations

Device Specs (DESIGN 2)	LT-Spice	Cadence-SPECTRE	This Work
f_0 > 100MHz	145MHz	125MHz	152MHz
Q > 0.8	0.9	0.9	0.95
Power < 400µW	255µW	268µW	235µW
Area < 200 µm^2	-	165 µm^2	201 µm^2
Transistor Dimensions	M1 W=21µ, L=0.18µ M2 W=2µ, L=1.5µ MB1 W=2µ, L=1µ MB2 W=13.5µ, L=0.18µ M1C W=21µ, L=0.18µ M2C W=20µ, L=1.5µ M_ext W=35µ, L=1.2µ VB1=1.15V, VB2=0.58V, VB3=0.8V		



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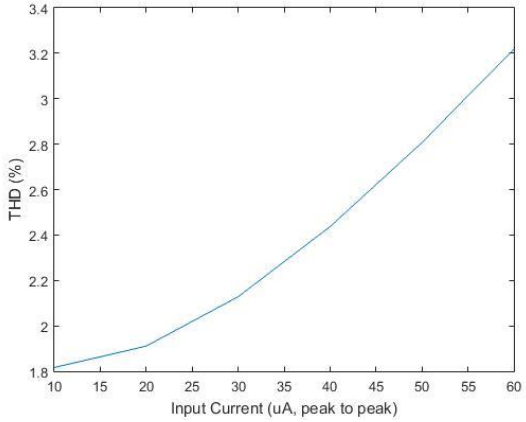
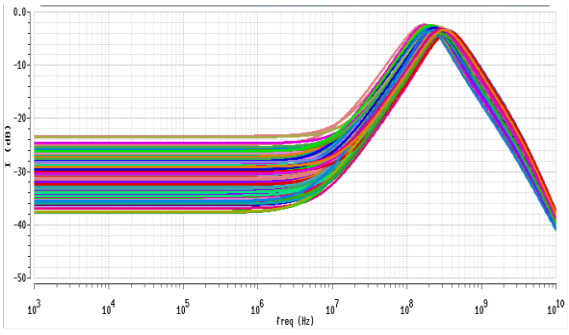


b)

Figure 11. THD result of the examplary designs: a) Design 1, b) Design 2.

In addition to the THD, Monte-Carlo simulations are given to test robustness of the exemplary designs against variability. In this respect, for 100 random samples are used to simulate process and mismatch variations for design 1 and 2. In the first part of the Figure.12, BP response variation can be observed. Although attenuation variate against Monte-Carlo points, it is confined in band of 10dB approximately. In addition, second part promises consistency of the design 1 due to the fact that center frequency of the filter changes up to 10%. Furthermore, Figure 13 shows the Monte-Carlo performance the other design. Its center frequency changes within 10% as well.



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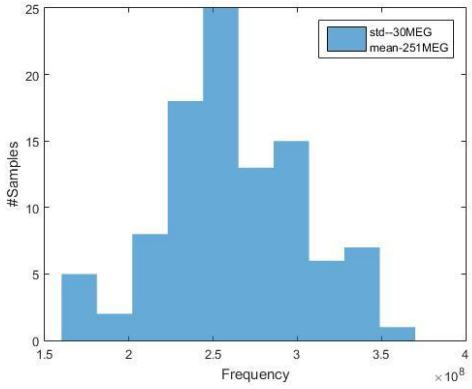
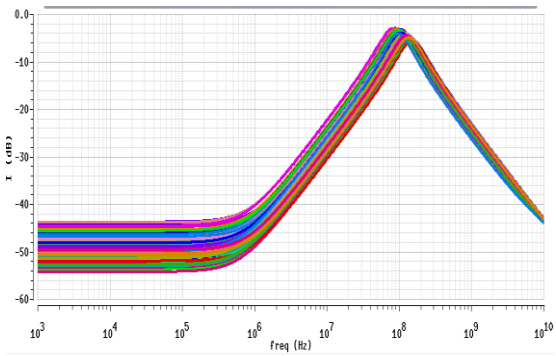


b)

Figure 12. Monte-Carlo simulation of the design 1: a) Frequency response of the BP output, b) Center frequency variation.

4. Conclusions

Proposed MOS-Only automation flow can be used to design novel structures, which contain small chip area and have promising performance metrics as shown in this paper. Moreover, this methodology produces not only filter structures but also a wide range of different circuits such as oscillators, phase shifters, amplifiers and so on. In the end, by adding new small signal parameters into the automation flow, accuracy of the automation will be increased.



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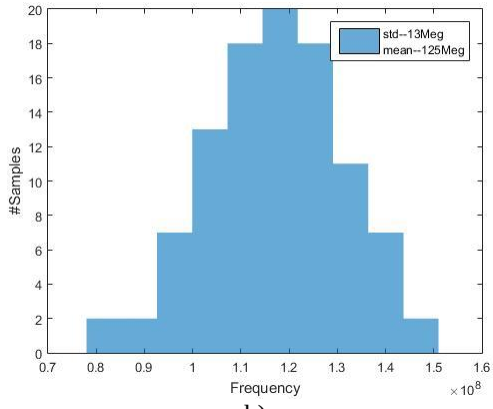

b)

Figure 13. Monte-Carlo simulation of the design 2: a) Frequency response of the BP output, b) Center frequency variation.

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