AN ENHANCED CURRENT-CONVEYOR BASED INSTRUMENTATION AMPLIFIER WITH HIGH CMRR

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Abstract: *In this work, a current-mode instrumentation amplifier with common-mode current cancellation is realized using enhanced CCII topology. Detailed CMRR analysis is performed and parameters for maximizing the CMRR are defined. The proposed structure is simulated using SPICE and realized on a prototyping board. According to the simulation and measurement results the proposed circuit shows superior CMRR performance compared to other well-known current-mode instrument amplifier topologies.*
Keywords: *Current-mode instrumentation amplifier, CMRR, current conveyors.*

1. Introduction

Instrumentation amplifier is one of the most frequently used design blocks in analogue signal processing which is used for differential signal amplification [1,2]. Voltage-mode instrumentation amplifiers are more popular compared to current-mode implementations; especially three op-amp instrumentation amplifier is the most frequently realized structure. The challenge in three op-amp instrumentation amplifier is matching ratio requirement for the resistor network. If the resistors are not accurately matched, high CMRR cannot be achieved. On the other hand current mode instrumentation amplifiers have special properties such as achieving gain independent of bandwidth [3]. Moreover, resistor matching is not an issue for many of the current-mode implementations. Besides the advantages of current-mode circuits, dc stability of the voltage-mode circuits are superior to current-mode ones [4].

In this work, a current-mode instrumentation amplifier (CMIA) based on differential current subtraction is implemented using enhanced current conveyors. The proposed structure is the enhanced implementation of the circuit proposed by Su and Lidgey [5]. In the proposed scheme, the implementation requires matched resistor pair; however, it is shown that high CMRR can be achieved by 1 % matching ratio of the resistors. Moreover, the number of resistors to be matched is not as high as the three op-amp implementations. In [2] it is mentioned that the CMRR of the current differencing instrumentation amplifier circuit is limited by the mismatch of the CCII outputs. However, by using advanced CCIIs such as commercial AD844, the implementation is not affected by impedance mismatch. Moreover, if the frequency is not high, the impedance mismatch is not an issue at all.

CCII+ based current-mode implementations are simulated and it is shown that the proposed approach is superior in CMRR and precision. The proposed circuit performance is measured using commercial AD844 current-mode devices and LF353 op-amps. The test results agree with simulations.

2. CMIA Structures

There are various current-mode implementations of instrumentation amplifiers in the literature [2-11]. Especially CCII+ based implementations are attractive for discrete component implementation. The first current-mode instrumentation amplifier (CMIA) proposed by Wilson [3] is shown in Figure 1. In CCII based implementations, low impedance terminal X has a limited R_x resistance, which limits the gain precision. The simplified model of CCII+ is depicted in Figure 2. The differential gain formula of the instrumentation amplifier shown in Figure 1 is:

$$A_d(s) = \frac{R_L}{(R_G + 2R_X)} \frac{1}{(1 + sC_L R_L)} \tag{1}$$

where R_x is the equivalent input resistance at the X terminal, R_G is the gain resistor, R_L is the load resistor and C_L is the effective output capacitance of the Z node of CCII+ [3].

In [6], an enhanced model of basic instrumentation amplifier is introduced, so that Rx resistance effect in the X terminal is avoided. Later on, the implementation is named as operational conveyor in [4]. Here, the effect of R_x resistance is eliminated by using an op-amp feedback. In

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general, CMRR of CMIAs is inversely proportional to the gain resistance R_G. In (1), there exists $(2R_x + R_G)$ in the denominator of the gain formula of the basic CCII based instrumentation amplifier of Wilson [3].

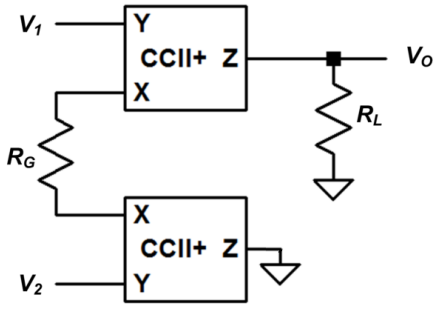


Figure 1. CCII+ based CMIA [3].

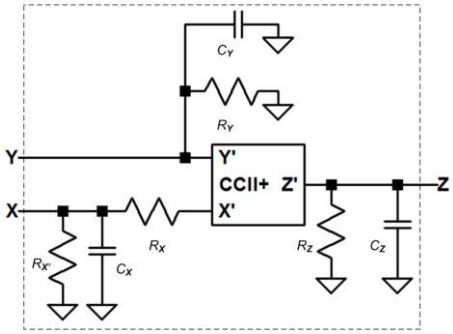


Figure 2. Simplified model of the CCII+.

To minimize the effect of R_x ,which is an internal resistance of the CCII, R_G is increased. Whenever R_G is increased, then CMRR decreases. Using the operational conveyor explained in [6] R_x effect is avoided, so that small values of R_G can be selected. The circuit of Figure 1 can be implemented by replacing the CCII+ elements with the enhanced CCII+ [6] as shown in Figure 3(a). In this configuration, the differential gain of the circuit becomes:

$$A_d(s) = \frac{R_L}{R_G}\frac{1}{(1+\frac{s\tau}{1+K\beta})} \tag{2}$$

where $\beta = R_G / (2R_x + R_G)$, τ and K are the time constant and the open loop gain of the op-amp, respectively. As shown in (2), the bandwidth is not severely affected by the modified implementation.

By implementing operational conveyors, precision of the instrumentation amplifier is increased. The cost of the implementation is increased by two op-amps. In later work Gift et.al name the enhanced current-conveyor as operational conveyor [4] which is shown in Figure 3(b).

In (Gift 2007) [4] an improved model of the Azhari and Fazlalipoor's implementation [7] is suggested which is shown in Figure 4. Here, the gain is doubled compared to Wilson CMIA [3], and CMRR is

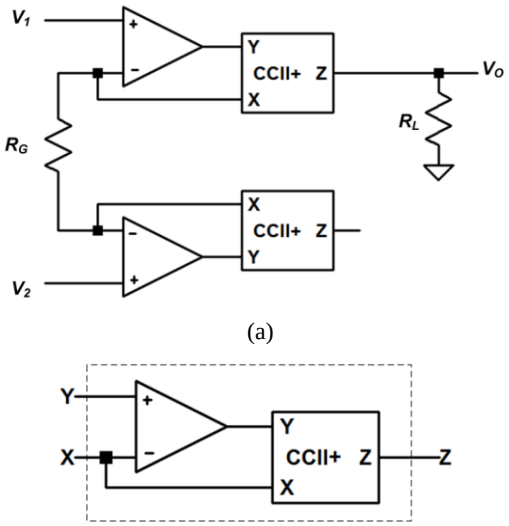


Figure 3. (a) Enhanced CMIA [6]; (b) enhanced current conveyor, i.e. the operational conveyor.

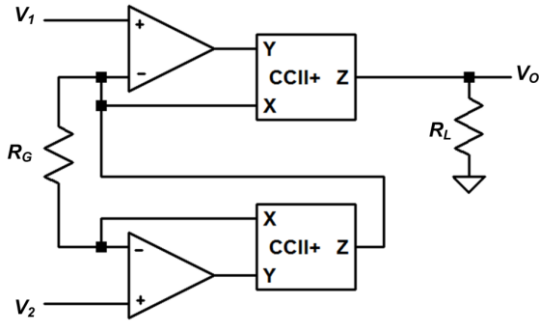


Figure 4. Improved implementation of Azhari's work [4].

improved. Here, the gain formula for low frequencies is:

$$A_d = \frac{V_o}{(V_2 - V_1)} = \frac{2R_L}{R_G} \tag{3}$$

3. Enhanced Current Differencing Instrumentation Amplifier

In this work, a differential current subtraction scheme is employed to further improve the CMRR of the enhanced instrumentation amplifier. The proposed circuit scheme is depicted in Figure 5. For simplicity, current transfer errors of the current conveyors are neglected for the differential gain calculations. The C_Z capacitances are the parasitic impedances of Z terminals of the CCIIs. Other parasitic impedances are neglected since other node impedances dominate over the parasitic impedances. In the input stage, V_1 and V_2 differential signals are applied to the inputs of the operational conveyors. Id current flows in the directions shown in Figure 5. The op-amp at the output stage is used for current subtraction and current to voltage conversion. For the positive terminal of the output stage op-amp:

$$I_d = \frac{V_1 - V_2}{R_G} \tag{4}$$

Here, the input stage parasitic impedances are neglected since R_G is much smaller than the parasitics. For the positive terminal of the output op-amp,

$$V_p = -I_d (R_1 \parallel \frac{1}{sC_Z}) \tag{5}$$

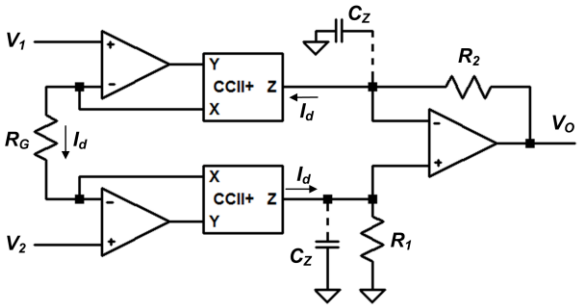


Figure 5. Proposed instrumentation amplifier

For the negative terminal of the output stage op-amp,

$$I_d = V_n . sC_Z + \frac{V_n - V_0}{R_2} \tag{6}$$

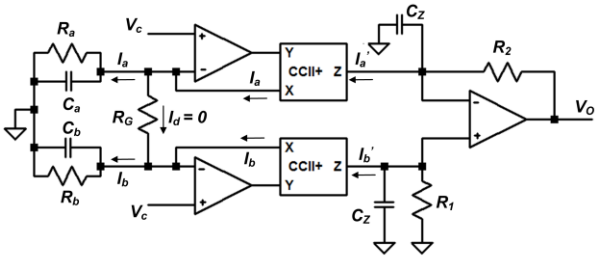


Figure 6. Common-mode input signal analysis

For the op-amps in linear operation $V_p = V_n$.
By replacing V_p inside V_n,

$$\frac{V_o}{R_2} = -I_d \left[1 + (R_1 \parallel \frac{1}{sC_Z}) sC_Z + \frac{(R_1 \parallel \frac{1}{sC_Z})}{R_2} \right] \tag{7}$$

$$V_o = \frac{(V_2 - V_1)}{R_G} R_2 \left[1 + (R_1 \parallel \frac{1}{sC_Z}) sC_Z + \frac{(R_1 \parallel \frac{1}{sC_Z})}{R_2} \right] \tag{8}$$

$$A_d = \frac{V_o}{(V_2 - V_1)} = \frac{R_2}{R_G} \left[1 + \frac{R_1}{R_1 + 1/sC_Z} + \frac{R_1}{R_2} . \frac{1}{1 + sC_Z R_1} \right] \tag{9}$$

By selecting $R_1 = R_2$, the differential gain is equal to:

$$A_d = \frac{V_o}{(V_2 - V_1)} = \frac{2R_1}{R_G} \tag{10}$$

If the input stage operational amplifier non-idealities are included, similar to (2) differential gain A_d is equal to:

$$A_d(s) = \frac{2R_1}{R_G} \frac{1}{(1 + \frac{s\tau}{1 + K\beta})} \tag{11}$$

where $\beta = R_G / (2R_x + R_G)$, τ and K are the time constant and the open loop gain of the op-amp, respectively. Input stage pole dominates over the output if same op-amps are used in the circuit, since the current differencing op-amp does not suffer from gain-bandwidth product limitations.

4. CMRR Analysis

The CMRR for the circuit of Figure 5 is affected by the mismatches of the impedances from X nodes to ground node. For the common-mode gain analysis, the circuit is redrawn in Figure 6. Here, C_a and R_a represents the first CCII's X node input parasitic impedances as $Z_a = R_a \| 1/sC_a$ [4]. Similarly, C_b, R_b and Z_b represent the second CCII's X node input parasitic impedances. In [4], Z_a and Z_b defined as equivalent, however, in the proposed topology, the mismatch of the two impedances have crucial node in CMRR calculations. The parasitic impedances Z_a and Z_b are the impedances from X nodes to ground; it is a summation of the impedances of X nodes of the input impedances of op-amps and CCII+ circuit together with layout and/or printed circuit board (PCB) parasitics. The resistive component of the input impedances from the X node to ground is usually in the order of mega-ohms. The I_a and I_a' are the input common-mode current at X node, and the copied current at Z node, respectively, for the first operational conveyor. Similarly, the I_b and I_b' are the input common-mode current at X node, and the copied current at Z node, respectively, for the second operational conveyor. Regardingly,

$$I_a = \frac{V_c}{Z_a} \tag{12}$$

$$I_a^{'} = (1 - \varepsilon_{Ca}) I_a = \gamma_{Ca} I_a \tag{13}$$

$$I_b^{'} = (1 - \varepsilon_{Cb}) I_b = \gamma_{Cb} I_b \tag{14}$$

where ε_{Ca} and ε_{Cb} are current transfer errors od X node to Z node for the first and second CCIIs, respectively. In the case that R_a and R_b together with C_a and C_b are close to each other, I_a' can be approximated as:

$$I_b = (1 - \varepsilon_X) I_a = \gamma_X I_a \tag{15}$$

Here, the phase angles of the currents are disregarded for easy calculations, however, γ_X can also be represented as a phasor. For the common mode analysis, the current mismatch between $I_b^{'}$ and $I_a^{'}$ is more significant, i.e., ε_X dominates over ε_{Ca} and ε_{Cb}. Since then, current transfer errors of ε_{Ca} and ε_{Cb} can be neglected, then,

$$I_a^{'} \approx I_a \tag{16}$$

$$I_b^{'} \approx I_b \tag{17}$$

$$I_b^{'} \approx (1-\varepsilon_X) I_a \approx \gamma_X I_a \tag{18}$$

The reason for the assumptions is that, matching ratios of the parasitic input impedance is more difficult than matching the current conveyors. The V_p voltage of the output op-amp is calculated as:

$$I_a^{'}(R_1 \parallel \frac{1}{sC_Z}) = V_p \tag{19}$$

The current equation for the V_n node is:

$$I_b^{'} = \frac{V_n}{\frac{1}{sC_Z}} + \frac{V_n - V_o}{R_2} \tag{20}$$

By replacing $I_a = V_c / Z_a$,$V_n = V_p$, $I_a^{'} \approx I_a$ and $I_b^{'} \approx \gamma_X I_a$,

$$\frac{V_o}{R_2} = -\frac{V_C}{Z_A}\gamma_X + \frac{V_C}{Z_A} + (R_1 \parallel \frac{1}{sC_Z})\left[\frac{1}{\frac{1}{sC_Z}} + \frac{1}{R_2}\right] \tag{21}$$

$$\frac{V_o}{R_2} = \frac{V_c}{Z_A}\left[-\gamma_X + (R_1 \parallel \frac{1}{sC_Z})\left[sC_Z + \frac{1}{R_2}\right]\right] \tag{22}$$

$$A_{CM} = \frac{V_o}{V_c} = \frac{R_2}{Z_A}\left[-\gamma_X + (R_1 \parallel \frac{1}{sC_Z})\left[sC_Z + \frac{1}{R_2}\right]\right] \tag{23}$$

C_Z can be neglected for simplicity, which holds for low to medium frequencies. Then, the simplified common mode gain can be estimated as:

$$A_{CM} \cong \frac{R_2}{Z_A}\left[-\gamma_X + \frac{R_1}{R_2}\right] \tag{24}$$

$$\gamma_R = \frac{R_1}{R_2} = \frac{R_2(1-\varepsilon_R)}{R_2} \tag{25}$$

$$\gamma_R = (1-\varepsilon_R) \tag{26}$$

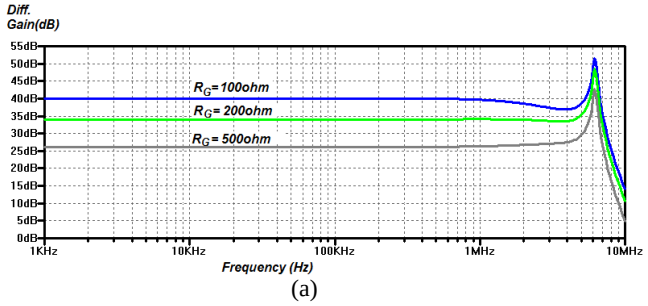
$$A_{CM} \cong \frac{R_2}{Z_A}(-\gamma_X + \gamma_R) \tag{27}$$

The CMRR can be estimated as:

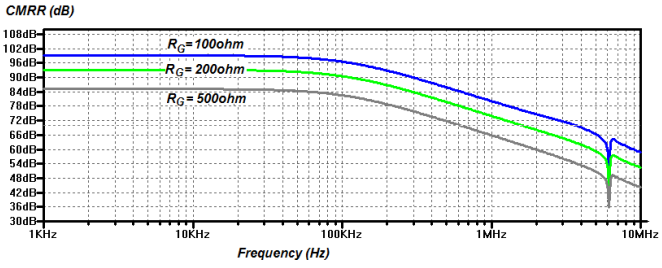
$$CMRR = \frac{|A_d|}{|A_{CM}|} \cong \frac{2Z_A}{R_G|-\gamma_X + \gamma_R|} \cong \frac{2Z_A}{R_G}\frac{1}{|-\varepsilon_X + \varepsilon_R|} \tag{28}$$

where Z_A represents the parasitic impedances from X node of the conveyor to ground, ε_X represents common-mode current mismatch related to the parasitic impedance mismatch of the X ports of the two operational conveyors (i.e. mismatch related to Z_a and Z_b in Figure 6), ε_R represents mismatch between R_1 and R_2 resistances of the proposed circuit, and R_G is the gain resistance. As the equation implies, to increase the CMRR:

- R_G resistance should be small,
- Input parasitic impedances should be as high as possible,
- R_1 and R_2 resistances should be matched,
- Input parasitic impedances should be matched (with the symmetry at X nodes of the current conveyors).



(a)



(b)

Figure 7. (a) Differential gain of the proposed structure; (b) CMRR of the proposed structure.

5. Simulations and Measurement Results

The proposed structure is simulated in SPICE and then tested on a prototyping board. First, the proposed instrumentation amplifier gain is simulated using various gain resistances. For the CCII+ and op-amp implementations, AD844 and LF353 are used, respectively. For the simulations, R_1 and R_2 resistances are selected as 5kΩ. Gain resistance R_G is selected as 100 Ω, 200 Ω and 500 Ω. The simulation results are shown in Figure 7 (a).

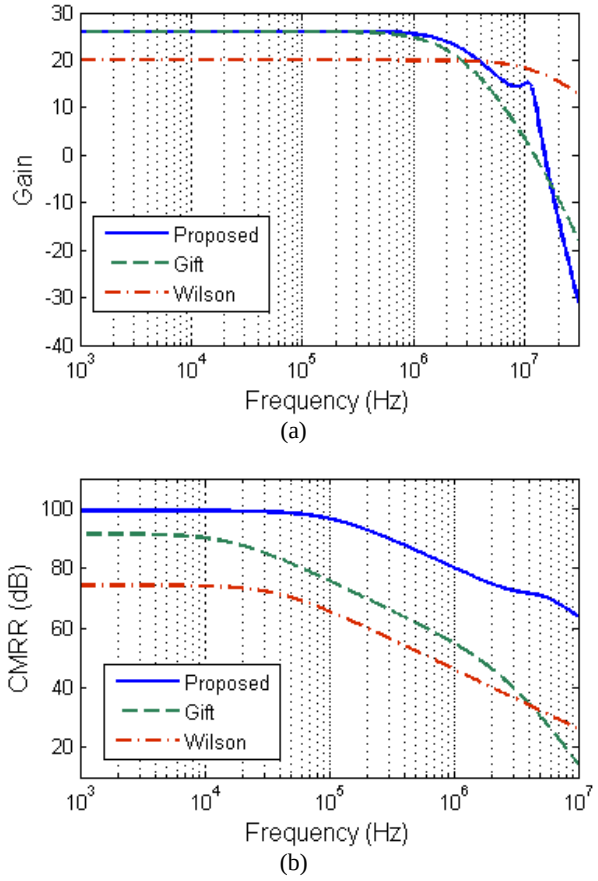


Figure 8. Simulation results: (a) Gain comparisons between Wilson 1989 [3], Gift [4] and the proposed CMIA; (b) CMRR results.

For the CMRR measurements, R_1 and R_2 resistances are selected as 5kΩ with ±1% tolerance. Moreover, external input parasitic impedances R_a and R_b are selected (by assumption) as 1 MΩ; C_a and C_b are selected as 2pF. The parasitics are given externally to show the mismatch effect. There are external impedances in circuits such as PCB resistances, wiring capacitances etc. Moreover, in this way, input impedance mismatches are also represented. Here, all of the parasitic impedances are simulated using ±5% tolerances. The worst case CMRR measurements according to the provided conditions by using various gain resistances are shown in Figure 7(b). Moreover, Monte-Carlo analyses are also applied to the circuit.

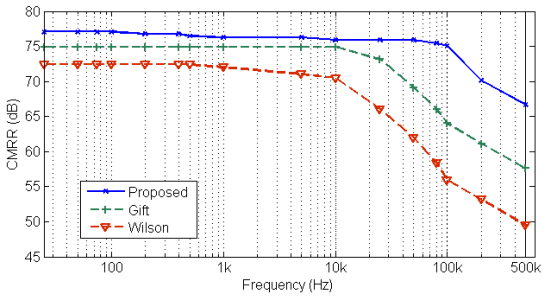


Figure 9. CMRR measurements of Wilson [3], Gift [4] and the proposed circuit

Worst-case simulation results of the Monte-Carlo analyses agree with the provided test results shown in Figure 7(b).

Instrumentation amplifiers of Wilson [3] and Gift [4] implementations are also simulated and realized for comparison. R_1 = R_2 = 1k Ω, R_G = 200 Ω are selected for the simulations. R_L is selected as 1k Ω for the circuit in (Gift 2007) [4], and 2 kΩ for the implementation in (Wilson 1989) [3], since the non-feedback gain formulation in [3] is halved. As shown in Figure 8(a), Wilson implementation gain is deteriorated because of the serial X node resistance of the CCII, where other structures are not affected by the X resistance since enhanced current conveyor topology (operational conveyor) is used. The proposed structure and Gift structure gain is degraded at 2MHz where the circuit 3-dB points are affected by op-amp bandwidth limitations. However, larger bandwidth op-amps can be used to resolve the limitation. For all of the simulations, external R_a, R_b, C_a and C_b parasitic impedances are included with the same values provided in the previous simulations. The CMRR simulation results of each of the topologies are shown in Figure 8(b). The proposed structure has the highest CMRR compared to others.

The proposed structure and the others are also realized on a prototyping board and CMRR measurements are made under the same test conditions. The CMRR results are shown in Figure 9. Although the measured CMRR results are much lower than the simulations depending on measurement conditions, the proposed structure has higher CMRR records compared to the CMIAs proposed by Wilson [3] and Gift [4]. To compare the proposed work with other CMIA implementations, Table 1 is provided.

Table 1. CMRR comparison with previous work

	CMRR	f_T
Wilson [3]	72	20 kHz
Gift [4]	75	30 kHz
Azhari [7]	95	10 kHz
Ghallab [9]	76	100 kHz
Khan [10]	72	100 kHz
Proposed	77	100 kHz

In Table 1, only Azhari et.al. [7] has higher CMRR, however, the bandwidth of the CMIA is much lower. Ghallab et.al. [9] proposes a high CMRR instrumentation amplifier. On the other hand, it is built using discrete transistors, difficult to build in discrete circuitry. In the

Table, only proposed work and Gift [4] has precise gain calculation dependent on discrete resistor values. To make a fair comparison, only CMIAs with discrete component implementations is included in Table 1. In the literature there are also monolithic implementations of instrumentation amplifiers [12-14]. In general, monolithic implementations provide higher CMRR due to better matching conditions, such as Prior et.al. [12] has 120 dB CMRR with 105 kHz bandwidth. However, in discrete implementations CMRR values are lower,as shown in Table 1.

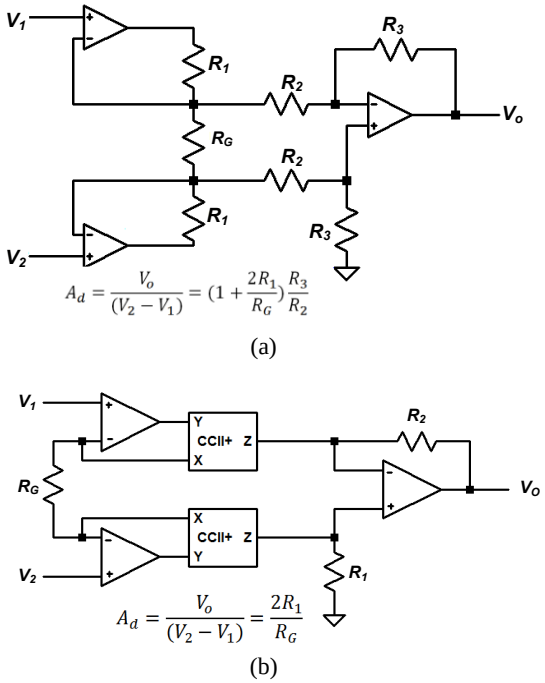


Figure 10. Instrumentation amplifiers: (a) Voltage-mode 3-opamp instrumentation amplifier; (b) Proposed CMIA.

6. Comparison with Voltage Mode Amplifier

It is important to show the CMRR advantage of the current-mode approach compared to the well-known 3-opamp instrumentation amplifier. Figure 10(a) and Figure 10(b) shows the 3-opamp configuration and the proposed current-mode implementation, respectively.

The CMRR measurements of the both implementations are made through Monte-Carlo simulations with %1 tolerances of the gain resistors. According to the Monte-Carlo simulations, the achievable CMRR value is 77 dB for the voltage-mode implementation whereas CMRR is 110 dB for the current-mode implementation. The simulation results are also shown in Fig. 11. For the simulations, LF353 wideband op-amps are used for voltage-mode amplifiers whereas AD844 is used for the current-conveyor implementations. The simulation results clearly show the advantage of the current-mode instrumentation advantage since the resistor mismatch dependency is much lower than the voltage-mode approach.

7. Conclusion

In this work, current-mode instrumentation amplifier proposed by Su and Lidgey [5] is improved using the operational conveyor [4, 6]. The proposed structure is simulated and implemented using AD844 current conveyors and LF353 wideband operational amplifiers. According to the measurements and simulations the proposed instrumentation amplifier is superior in CMRR compared to the previous current conveyor based implementations. Furthermore, the gain of the instrumentation amplifier can be precisely adjusted using external resistors. CMRR calculation is given and rules for increasing CMRR are defined in detail. Since gain is not dependent on internal resistances of the current conveyors in the proposed structure, gain resistance R_G can be selected smaller which provides higher CMRR.

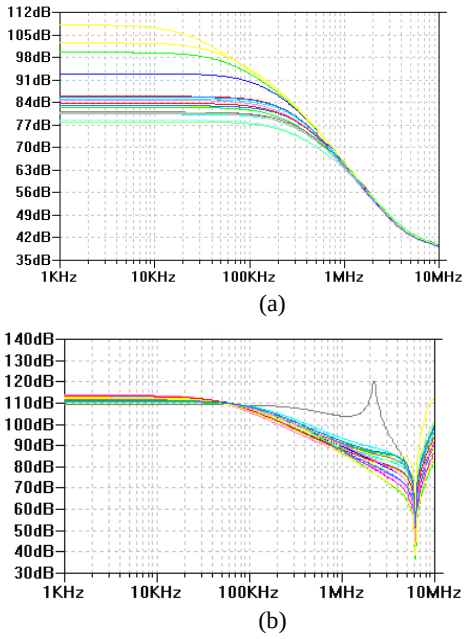


Figure 11. Monte-Carlo CMRR simulations of: (a) 3-opamp instrumentation amplifier; (b) Proposed CMIA

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