Design and Optimization of a High Power Density and Efficiency Boost PFC

B. Fincan, M. Yilmaz, A. Goynusen, and K. Erenay

***Abstract*—Nowadays electrical appliances have been becoming more and more popular every day in our life, and the systems that have more power density and that use energy efficiently and that improve the quality of the energy are required more. Especially with the decisions and regulation changes of the United States and the European Union in recent years, it has become compulsory to replace low efficiency electric motor drive systems with high efficiency permanent magnet electric motors and drivers, and as a result permanent magnet motors that have high efficient field orientation control algorithms technologies have begun to be chosen. Low cost uncontrolled rectifiers that have high power factor have become a necessity with the need for DC bus. In such systems with inherently nonlinear characteristics, the need for Power Factor Correction (PFC) circuit has been increasing, and Boost PFC (BPFC) which increase the input voltage are widely preferred for low/medium power applications. Therefore, distortion harmonics and high frequency noises are reduced according to standards such as CSRIP Class B – TS EN 61000-3-2 and also output voltage remains constant, becoming more than peak amount of the input grid voltage. In that study, it is designed that BPFC that has 1,150W output power level by increasing system's power density and efficiency. The system cost is reduced by decreasing the requirement of EMI filters and heatsink size, since using SiC (Silicon Carbide) diode and optimizing the system contribute increasing efficiency and power density. The most efficient Boost PFC design is realized at the lowest cost by performing detailed design, loss and cost analysis for each component used. The Boost PFC with full system efficiency of 95.5% at full load is obtained by model validation done by comparing the simulation results with the experimental results obtained by hardware implementation.**

Index Terms—**Active filter, harmonic, efficiency, power density, power factor correction, SiC diode.**

I. Introduction

ENVIRONMENTAL problems are emerging day by day with increasing energy demand and therefore the importance of more efficient use of energy is increasing. Without considering the effects on the economy and the environment, the use of all kinds of energy and systems distorts the ecological balance and causes global warming. In this context, energy resources in the country's economy should be evaluated with sustainable development approach, and efficient production and saving of energy should be taken into consideration. For this reason, it has come to the agenda to replace the inefficient drive systems with more efficient systems with the regulations and restrictions introduced.

Permanent magnet synchronous motors are the most efficient motors and have high power densities, which require voltage-fed driver. This type of conventional voltage-fed drive systems, which have disadvantages such as high cost, a large number of semiconductor switch elements, and complex control algorithms, require DC bus voltage, except for the matrix converters and they also produce harmonics and noise.

Electrical systems that transmit high frequency components (harmonics and noises) to the grid can cause electronic devices that do not have enough immunity to electromagnetic interference (EMI) to be adversely affected or distorted. For this reason, the expected noise level from a device conforming to electromagnetic compatibility (EMC) standards is that does not transmit noise to the grid, and that it is resistant to external noise, and that the elements inside the device do not interfere or distort each other. For these reasons, energy quality and efficiency are very critical in electric energy systems and precautions must be taken [1].

Passive filters consisting of elements such as inductance, capacity and resistance can be used to suppress reactive components at higher frequency values. The reactive power suppressing capacitive compensation systems in the fundamental frequency components are the most commonly used passive filter systems. These filters are not able to act on reactive components outside of the previously targeted frequencies and carry the risk of resonance with the capacitive or inductive components in the grid and the capacitive or inductive load that the system feeds. In this case, the overcurrent generated at the resonance frequency can damage the system [2]. With the BPFC used as an active filter, the phase difference between the current that grid feeds and the grid voltage, the reactive power and grid harmonics are reduced to zero and the power factor converges to one. In power electronic circuits, the power factor (PF) cannot be measured only by the phase difference between current and voltage ($cos\varphi$). Because the expression of $cos\varphi$ is only a measure of the fundamental frequency components. In fact, as can be seen in Equation (1), the power factor is the ratio between average value of the product of the input current and input voltage and the effective value of the product of the

B. FINCAN, is with Department of Electrical Engineering, Istanbul Technical University, Istanbul, Turkey, (e-mail: fincan@itu.edu.tr).

M. YILMAZ, is with Department of Electrical Engineering, Istanbul Technical University, Istanbul, Turkey, (e-mail: myilmaz@itu.edu.tr).

A. GOYNUSEN, is a senior engineer at Pavotek R&D, Istanbul, Turkey, (e-mail: alper.goynusen@pavotek.com.tr).

K. ERENAY, is a manager at Pavotek R&D, Istanbul, Turkey, (e-mail: kerem.erenay@pavotek.com.tr).

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input current and input voltage. In other words, the PF calculation is calculated by concept of Total Harmonic Distortion (THD), which is seen in Equation (2), where high frequency currents are also considered.

$$PF = \frac{\frac{1}{T_s}\int_0^{Ts} v_{in}(t)\cdot i_{in}(t)dt}{\sqrt{\frac{1}{T_s}\int_0^{Ts}\left(v_{in}(t)\cdot i_{in}(t)\right)^2 dt}} = \cos\varphi \cdot \frac{1}{\sqrt{1+THD^2}} \quad (1)$$

$$THD = \frac{\sum_{n=2}^{n=\infty} I_n^{\,2}}{I_1} \quad (2)$$

BPFC can keep the output voltage constant even when the input voltage increases or decreases. In this way, even if the voltage drops, the motor input voltage does not change and the motor operation is not affected. Since the output voltage is higher than the peak value of the input voltage, there is also a minimum value for the output voltage. For a single-phase system in Turkey, this value cannot be less than 381 V because the effective value of the mains voltage in Turkey can rise to 265V. The average value of the output voltage can be selected as at least 385V since it is necessary to work somewhat away from the limit value. The BPFC elements have a maximum voltage level due to their internal resistance. If the output voltage is close the input voltage in the BPFC, the converter can work more efficiently [3]. The input current of the medium power motors (1 - 3 kW) operating with 400V input voltage is low, so copper losses are reduced and these motors can operate at wider speed and torque range depending on the input voltage. Therefore, the fact that the BPFC with 400V output voltage is able to run with very high efficiency, which provides a great advantage in electric motor applications. For higher power systems, bridgeless PFC or interleaved PFC circuits should be used [4].

For the design of a high-efficient and power-intensive BPFC, detailed loss analysis must be performed by selecting the appropriate elements [5]. Each element is sized according to current and voltages and the selection of elements has been made with detailed designs in which losses and cost are taken into consideration. While SiC diode and system optimization result in increase in total efficiency and power density, and EMI filter and heatsink requirement are reduced and total system cost is reduced. The simulation results are compared with the hardware implementation results, and a BPFC with 1,150W output power is realized by increasing the power density and efficiency at low cost.

II. BPFC

There are three modes in the BPFC depending on the inductance current continuity: 1. Continuous conduction mode (CCM), 2. Discontinuous conduction mode, 3. Critical conduction mode. In the context of this work, CCM with less switching losses has inductance current which closer to the sinusoidal than other modes, and therefore has smaller EMI filters [6]. Figure 1 shows the BPFC and the control block diagram for this circuit. From the point of view of cost and loss analysis, it can be said that five main system components should be concentrated. These are uncontrolled bridge rectifier, inductance, output capacitor, MOSFET and diode. In the scope of the study, electronic card design and hardware system have been implemented by analyzing every system element, designing and making the necessary calculations accordingly.

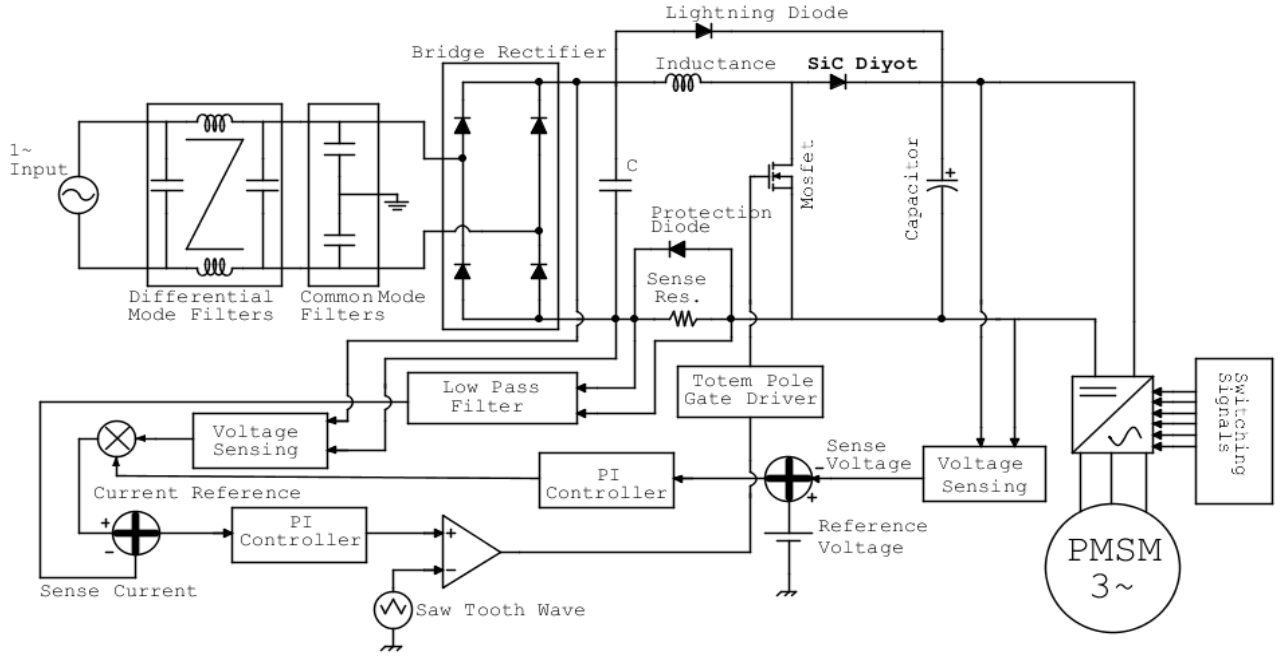

Fig.1. BPFC and its control block diagram

A. BPFC Controller Design

The output dc bara voltage will be oscillated in a certain range as the average value is 390V, V_o, and the voltage divider is used in the circuit so that it reduces the output DC bus voltage to 2.5V. The oscillations on the output voltage may lead to system instability. For this reason, as shown in Figure 2, the system stability is increased by connecting a parallel 470pF capacitor (C_{o1}) to resistance. In order to keep the output voltage constant, compensation is done by using PI controller. The difference between the reference output voltage and the measured output voltage is compensated by the PI controller, which gives the current amplitude reference value.

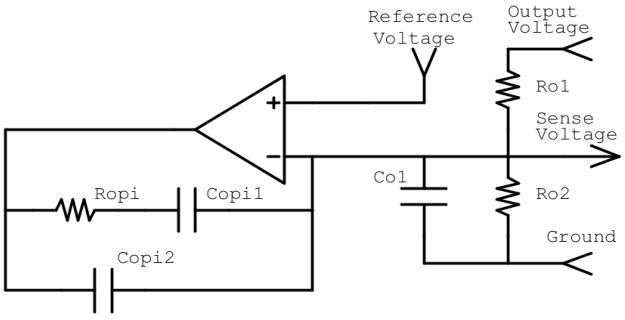

Fig.2. Output voltage sense circuit and PI controller

The FAN6982 IC is used in the study and the variables given by the IC for the PI controller account are given below. In Equation (3), K_{max} is the ratio between the maximum allowed output power and the nominal output power, which is 1.3 for this study. The output current (I_o) is 2.95A and the output capacitance (C_o) is selected as 420µF as will be discussed in the next sections. The cut-off frequencies of PI controller are 20Hz and 50Hz. G_{MV} is an error amplifier, which is constant and $70 \cdot 10^6$. According to, Equation (4), (5) and (6), C_{op1}, R_{op1} and C_{op2} are calculated 47nF, 170 kΩ and 18nF, respectively.

$$K_{\max} = P_{o,\max} / P_o \tag{3}$$

$$C_{op1} = \frac{G_{MV} \cdot I_o \cdot K_{\max}}{5 \cdot C_o \cdot (2 \cdot \pi \cdot f_{VC})^2} \cdot \frac{2.5}{V_o} \tag{4}$$

$$R_{op1} = \frac{1}{2 \cdot \pi \cdot f_{VC} \cdot C_{op1}} \tag{5}$$

$$C_{op2} = \frac{1}{2 \cdot \pi \cdot f_{VP} \cdot R_{op1}} \tag{6}$$

A sense resistance whose value does not change importantly with temperature (<100 ppm, temperature coefficient) should be chosen to read the inductance current. The sense resistance is one of the most critical points in the reliability of the system and the power rating of it should be chosen appropriately. With Equation (7), the effective value of the current passing through the inductance for the lowest input voltage of 185V is calculated as 6.5A, and for the 66mΩ sense resistance, 2.77W power loss will be according to Equation (8). η is efficiency of system.

$$I_{L,rms} = \frac{P_o}{V_{in(\min)} \cdot \eta} \tag{7}$$

$$P_{loss,sense} = I_{L,rms}{}^2 \cdot R_{sense} \tag{8}$$

As shown in Figure 3, diodes connected in reverse parallel to the sense resistance are added to protect it from overcurrent (lightning, etc.). Because the voltage drop across this diode is greater than the voltage drops across the sense resistor, the diode will not switch on - (up to 1,150W output power, P_o) during normal operation. Due to the sense current that has a noise, it is necessary to use a low-pass filter to suppress these noises. This filter is extremely critical, as the time constant of the filter increases, the system stability increases but the capacitive increases and *cosφ* goes away from 1.

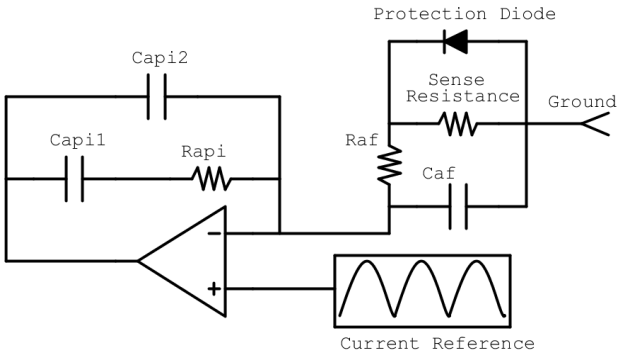

Fig.3. Current sense filter

The output voltage error is compensated by the PI controller as described in the previous section and the reference current value waveform is obtained by multiplying the input voltage shape by the current amplitude value given by PI controller. The difference between the sense current and the reference current is compensated again by the PI controller and the obtained signal is compared with the sawtooth wave to obtain the pulse width modulation signal to be applied to the MOSFET. f_{IC} is cut-off frequency of the PI controller, which should be selected times less than the switching frequency, so it is 6600Hz and, f_{IP} 60kHz in this study. G_{MI} is error amplifier, whose value is $88 \cdot 10^{-6}$. According to Equation (9), (10), (11) and (12), R_{api}, C_{api1} and C_{api2} seen in Figure 3 are selected 220Ω, 330nF and 12nF, respectively.

$$\left| \frac{\hat{V}_{CS}}{\hat{V}_{IEA}} \right|_{@\, f = f_{ic}} = \frac{R_{ölçme} \cdot V_o}{V_{RAMP} \cdot 2 \cdot \pi \cdot f_{ic} \cdot L} \tag{9}$$

$$R_{api} = \frac{1}{G_{MI} \cdot \left| \frac{\hat{V}_{CS}}{\hat{V}_{IEA}} \right|_{@\, f = f_{ic}}} \tag{10}$$

$$C_{api1} = \frac{1}{R_{api} \cdot 2 \cdot \pi \cdot \frac{f_{IC}}{3}} \tag{11}$$

$$C_{api2} = \frac{1}{R_{api} \cdot 2 \cdot \pi \cdot f_{IP}} \quad (12)$$

B. BPFC Inductance Calculation and Design

Because the dimensions such as size, loss and price are the determining factors for the inductance design, a core material selection must be made first. The use of ferrite cores is not preferred due to the fact that the fringing flux occurring in the air-gap is due to the noise propagation to other elements. In addition, the ferrite material core will lose its inductance function when it reaches the critical magnetic field density. For this reason, instead of a ferrite material, a powder core material is used. Since the saturation point of the powder core is higher than the saturation point of the ferrite core, smaller volume and mass inductances can be made by the powder core and emitted noise is lowered when the powder core is used. With a toroidal core, the inductance with high inductance value can be designed in unit volume. As the load increases, the air spaces in the powder core nest get irregularly saturated and inductances with the powder core do not have a constant magnetic permeability. As the saturation air particles increase, the magnetic reactivity and hence the inductance are reduced [7]. Because of these properties, Magnetics Company's "KoolMu" powder core is chosen and used in design. If the current on the inductance is chosen to have a fluctuation of 50%, the inductance value of Equation (13) will be set to 300µH. At the input voltage of 185V, the peak value of the inductance current will be 13.75A and the current ripple will be 5.5A.

The inductance design using Magnetics-KoolMu 77439 coded powder core is achieved with this inductance to obtain an inductance of 135nH in one turn wire wound, with an inductance value of 486H with 60 turns. This is valid when no current flows through the inductance value and the inductance value will decrease with loading. Using the company's "Magnetics Curve Calculation Tool", an inductance value of 296µH is obtained with 60 turns full load KoolMu 77439, which gives the value determined from Equation 13 [8], T is period of switching.

$$L = \frac{1}{\%Dalgalılık_{I_L}} \cdot \frac{V_{in(\min)}^{\ 2}}{P_o} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{in(\min)}}{V_o}\right) \cdot T \quad (13)$$

$$H_{\max} = \frac{I_{L,\max} \cdot N}{l_e} \cdot \frac{4 \cdot \pi}{1000} \quad (14)$$

$$H_{\min} = \frac{I_{L,\min} \cdot N}{l_e} \cdot \frac{4 \cdot \pi}{1000} \quad (15)$$

The maximum value of the magnetic field strength, H_{max}, is calculated to be 96.53 Oersted according to Equation (14), minimum value of the magnetic field strength, H_{min}, is calculated to be 57,91 Oersted according to Equation (15). B_{max} 4,800 Gauss corresponding to H_{max} and B_{min} 3,300 Gauss corresponding to H_{min} are designated as "normal magnetization curves" in the magnetics catalog [6]. The flux and frequency-dependent core loss given by the manufacturer Magnetics is given in Equation (16) and is calculated to be 5.433W, f is frequency of switching and V_{core} is volume of the core.

$$P_{loss,core} = \frac{\left(B_{\max} - B_{\min}\right)^2}{4} \cdot f^{1.46} \cdot V_{core} \quad (16)$$

Depending on the current density of the windings, 1.5 mm diameter wire copper coil is used and a cross section area of 1.76 mm^2 is provided and the total length of copper wire used is approximately 6.23 meters. The conductor wire resistance is calculated as Equation (17) based on the specific resistance of the length and the copper at 100°C, and is determined as 71mΩ. Coil losses are calculated using the effective value of the coil current according to Equation (18), ρ is resistivity of copper. The effective value of the coil current for the input voltage of 185V will be 6.5A, resulting in a loss of 3W. In total, a power loss of 8.432 watts was determined.

$$R_{copper} = \frac{\rho \cdot l_{copper}}{A_{copper}} \quad (17)$$

$$P_{copper} = I_{L,RMS}^{\ 2} \cdot R_{copper} \quad (18)$$

C. MOSFET Selection and Losses Analysis

In the case of BPFC, the body diode parallel to the MOSFET never switches on, so it is only necessary to focus on the MOSFET. The current value of the MOSFET should be selected according to the lowest value of the input voltage, considering the highest junction temperature. The low value of C_{oss} and the transmission resistance of the MOSFET to be selected and the fast switching is very important in terms of efficiency.

The effective value of the current passing through the MOSFET can be calculated using Equation (19) and the maximum current value of the MOSFET is 13.75A. This current value must be met by the MOSFET even at a temperature of 100°C. The effective value of the MOSFET current according to Equation (19) is calculated as 4.08A. Conduction loss can be calculated by Equation (20), considering the relation of the conduction resistance with temperature. The equations (21), (22) and (23) are used for the turn-off losses in the case of equations (24) and (25). The parameters seen in Equation (20), (21), (22), (24) and (25) can be found from used MOSFET datasheet.

$$I_{MOS,RMS} = \frac{P_o}{V_{in,RMS}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{in,RMS}}{3 \cdot \pi \cdot V_o}} \quad (19)$$

$$P_{S,cond} = I_{MOS,RMS}^{\ 2} \cdot R_{on(100°)} \quad (20)$$

$$t_{on} = C_{iss} \cdot R_g \cdot \ln\left(\frac{V_g - V_{th}}{V_g - V_{pl}}\right) + C_{rss} \cdot R_g \cdot \left(\frac{V_o - V_{pl}}{V_g - V_{pl}}\right) \quad (21)$$

$$C_{rss} = \frac{Q_{gd}}{V_o} \quad (22)$$

$$P_{s,on} = 0.5 \cdot I_{L,ort} \cdot V_o \cdot t_{on} \cdot f \quad (23)$$

$$t_{off} = C_{rss} \cdot R_g \cdot \frac{V_o - V_{pl}}{V_{pl}} + C_{iss} \cdot R_g \cdot \ln\left(\frac{V_{pl}}{V_{th}}\right) \quad (24)$$

$$P_{s,off} = 0.5 \cdot I_{L,ort} \cdot V_o \cdot t_{off} \cdot f \quad (25)$$

Calculation of turn-off switching losses by conventional methods is given in Equation (25). In addition, C_{oss} behaves like a non-linear capacitive snubber, so the turn-off switching losses will be lower than the calculated value. Equations (26) where MOSFET is not in conduction, equation (27) gate losses are calculated. The sum of the losses calculated in Equation (23), (25), (26) and (27) is calculated as seen in Equation (28), and the total losses are obtained.

$$P_{S,OFF} = E_{OSS} \cdot f \quad (26)$$

$$P_{S,Gate} = V_g \cdot Q_g \cdot f \quad (27)$$

$$P_{S,Total} = P_{S,cond} + P_{S,ON} + P_{S,OFF} + P_{S,Gate} \quad (28)$$

D. Diode Selection

The diode is one of the most critical elements as the diodes in BPFCs produce high values of reverse current (I_{rrm}) as they go (depending on the slope of the current during turn-on time). Since the reverse current I_{rrm} passes through the MOSFET at the time of turn-on (t_{on}) of the MOSFET, it causes both the loss of switching and the problems of electromagnetic interference (EMI). Diode reverse recovery times (t_{on}, t_a, t_b), I_{rrm} and MOSFET current are shown in Fig. 4. As can be seen, the I_{rrm} current increases the MOSFET current. Using the totem pole structure, the MOSFET's t_{on} duration can be increased, so that the EMI generated by the reverse current I_{rrm} is reduced, but the switching losses are also increased in the same way [9].

The maximum value of the inverse recovery current is obtained by the Equation (29) and the decreasing curve of the diode current is obtained by the Equation (30). The duration of change from the zero current to – I_{rrm} by the Equation (31) is calculated again. The values of Q_{rr} and t_{rr} are obtained from the manufacturer's diode information book and $I_{d,\,peak}$ is equal to the peak value of the inductance current, of course. As the Q_{rr} value increases, the turn-on switching loss of the MOSFET appears to increase significantly.

$$I_{rrm} = \frac{2 \cdot Q_{rr}}{t_{on}} \quad (29)$$

$$\frac{dI_f}{dt} = \frac{I_{d,peak}}{t_{on}} \quad (30)$$

$$t_a = \frac{I_{rrm}}{\frac{dI_f}{dt}} \quad (31)$$

$$t_b = t_{rr} - t_a \quad (32)$$

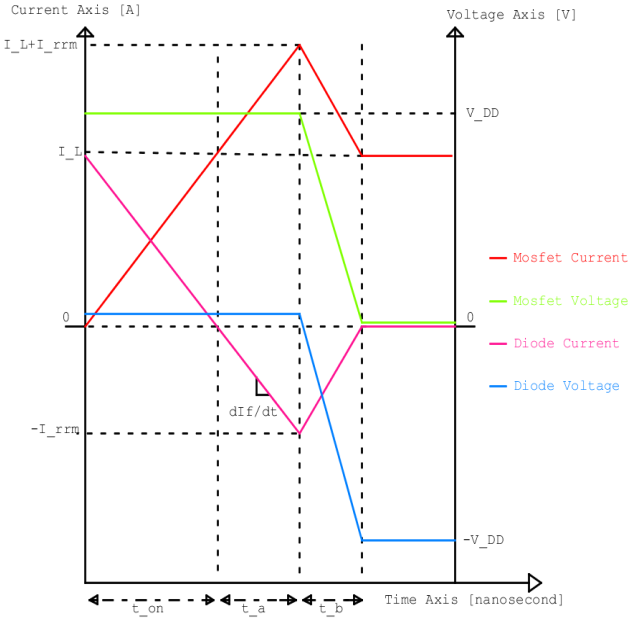

Figure 4: Diode inverse recovery current, MOSFET current and invertals durations

The average value of the diode current according to the BPFC structure is equal to the average of the load current. The average of the diode current with Equation (33), the diode conduction losses with Equation (34), the switching losses with Equation (35) and the diode total losses with Equation (36) are obtained. V_f is voltage drop of used diode, it can be found from used diode datasheet.

It has been observed both theoretically and experimentally that the problems mentioned above are not able to be solved by the use of conventional silicon diodes in the system. For this reason, Silicon Carbide (SiC) diodes with very low reverse recovery times and currents are preferred in the BPFC. The recovery charge of SiC diodes is small enough not to be compared with the reverse recovery charge of silicon diodes. SiC diodes have other reasons to be used. For instance, these diodes fall in reasonable prices in recent years, their reliability is high, their switching behavior is independent of temperature and they can withstand high temperature values. These superior features make it possible to increase the switching frequency and reduce the EMI level significantly while achieving a circuit with increased efficiency, reduced size and increased power density.

In Table I, loss analysis is performed for 5 different MOSFET elements and in Table II, loss analysis is performed for 6 diode elements, 2 silicon diodes and 4 SiC diodes. Assuming that R_{on} and R_{off} resistances are 15Ω and 30Ω, respectively, the turn-on time for the MOSFET and the turn-off time are calculated using Equation (21) and Equation (24). I_{rrm} with Equation (29), diode switching losses using I_{rrm} with Equation (35) and diode conduction losses with Equation (34)

are calculated for each diode element in Table II. After the loss - price optimization is made; it is decided to use ST STC606 SiC diode. It is predicted that this diode will produce 0.37A I_{rrm} when going to turn-off. This current value is added to the MOSFET turn-on current as shown in Table I and as shown in Figure 4, and the total loss is calculated by using Equation (28) for each MOSFET element. After the loss - price optimization, Fairchild decided to use the FCH125N60E MOSFET element. According to the analysis result, it is estimated that the MOSFET element has 21.12W loss during operation and the junction temperature is 59°C. The SiC diode is expected to operate at 7.66W loss.

It is thought that two paradigms should be emphasized. The first is that the resistance values of R_{on} and R_{off} are actually determined after the tests made after the Test Setup is established. In the determination of R_{on} and R_{off} gate resistances, the role of the equations given for MOSFET loss analysis is only in the stage of initial value assignment. The most accurate gate resistance values can only be found by empirical methods because the MOSFET element is a nonlinear element since it has the parasitic capacitances, inductances and resistances of the structure which changes with the operating frequency, the gate voltage, the noise level at the gate voltage, the junction temperature, the Drain - Source Voltage and the quality of the printed electronic board drawn. For this reason, there is still no exact model in the literature that compares the turn-off and turn-on characteristics of the MOSFET. The second paradigm is related to the diode reverse recovery current model. Before a real reverse current I_{rrm} is recovered and settled zero, it fluctuates around the zero point with decreasing amplitude in the MHz range. This oscillation affects both EMI and increases losses. For this reason, there is no doubt that the reverse recovery current model is also an incomplete model.

It should be preferable to use the TO220 package as much as possible because the parasitic inductance of the TO220 package is less than the parasitic inductance of the TO247 package. On the other hand, the heat dissipation performance of the TO247 package is higher than that of the TO220 package. For this reason, the TO224 package is chosen because the MOSFET losses are greater than 10W and the diode losses are smaller than 10W.

TABLE I
MOSFET LOSSES ANALYSIS (R_{on}=15Ω and R_{off}=30Ω)

MOSFET	t_{on} [ns]	t_{off} [ns]	Ps,con [W]	Ps,on [W]	Ps,off [W]	P_g [W]	P_{total} [W]	I_{rrm} [A]	ΔT
INFINEON 1	74.931	29.31	1.53	11.40	4.32	0.07	17.32	0.37	7.79
INFINEON 2	34.155	13.06	1.76	5.19	1.93	0.03	8.91	0.37	12.09
INFINEON 3	166.310	22.83	2.07	25.29	3.37	0.10	30.83	0.37	17.57
FAIRCHILD 1	107.019	21.29	1.61	16.28	3.14	0.10	21.12	0.37	9.50
FAIRCHILD 2	115.328	32.40	1.60	17.54	4.78	0.10	24.03	0.37	10.81

TABLE II
DIODE LOSSES ANALYSIS

	Diode	Q_{rr} (nQ) (130A/nS)	P_{con} [W]	t_{rr} [ns]	dIf/dt [A/ns]	I_{rrm} [A]	t_a [ns]	t_b [ns]	P_{switch} [W]	P_{total} [W]
Silicium Diodes	INFINEON	120.00	6.38	65.0	129	3.24	17.45	47.55	1.57	7.95
	FAIRCHILD	62.00	9.86	17.0	129	2.16	9.02	7.98	0.81	10.67
SiC Diodes	WOLFSPEED	15.00	4.93	8.00	129	0.28	2.18	5.82	0.20	5.13
	INFINEON	10.00	5.80	5.00	129	0.19	1.45	3.55	0.13	5.93
	ROHM	9.00	4.50	12.0	129	0.17	1.31	10.69	0.12	4.61
	ST	20.00	7.40	23.0	129	0.37	2.91	20.09	0.26	7.66

E. BPFC Capacitor Selection

In the BPFC, the value of the C_o capacitor is determined by the amount of oscillation of the output voltage. The average of the output voltage is 390V, and according to Equation (37), a voltage swing of about 24V with a capacity of 420µF will occur. In spite of ΔV_o = 6%, it is decided to use 420µF capacitor considering cost and volume optimization. The serial parasitic resistance value for DC link capacitor according to Equation (38) is obtained as 1.136 Ω. The ambient temperature of this capacitor is 85°C, the loss factor (DF) value is 0.15, the maximum effective value of the current to pass is 1.55 A and the tolerance is 20%. f_{grid} is frequency of grid.

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{grid} \cdot \Delta V_o \cdot V_o} \quad (37)$$

$$ESR = \frac{DF}{2 \cdot \pi \cdot f_{grid} \cdot C_o} \quad (38)$$

The riskiest component of the life cycle of BPFCs is the DC bus capacitor, which determines the circuit life. For this

reason, the lifetime of the capacitor must be calculated appropriately and the selection must be made accordingly. In practice, the system will be placed in the basement so that the BPFC will work in a water booster. In summer the basement can have an ambient temperature of 50°C (T_0). The information booklet of the capacitor to be used is provided with a working guarantee of 85 hours (T_{max}) ambient temperature of 3000 hours ($LIFETIME_0$). When calculated according to Equation. (39), this capacitor has been determined to have a life of 33,000 hours (approximately 7.5 years) [10].

$$LIFETIME = LIFETIME_0 \cdot 2^{\frac{T_{\max} - T_0}{10}} \quad (39)$$

The effective current of the capacitor is obtained by using Equation (40), and the effective value of the current to pass through the capacitor when the input voltage is 185V is determined as 3.8A. According to Equation (41), the amount of power loss in the capacitor is calculated.

$$I_{C_{O,RMS}} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot P_o^{\,2}}{3 \cdot \pi \cdot V_{in(\min)} \cdot V_o} - \frac{P_o^{\,2}}{V_o^{\,2}}} \quad (40)$$

$$P_{C_o} = I_{C_{O,RMS}}^{\,2} \cdot ESR \quad (41)$$

It is important to choose a capacitor that will guarantee the effective value of the current to pass through the capacitor, otherwise the life of the capacitor will decrease rapidly. According to the datasheet of the selected capacitor, 1.55 A is guaranteed for a frequency of 120Hz and an ambient temperature of 85°C. Because the application system will operate at approximately 50°C, this capacitor can withstand currents greater than 1.55A in the datasheet. When the information from the manufacturer is multiplied by the temperature coefficient of 2.42 at 1.55A, this capacity is calculated to be at most 3.75A at 50°C ambient temperature.

The capacitor current is obtained at the full load and the lowest input voltage value in the PSIM simulation program, then this capacitor current is separated to components in accordance with frequency by using Fourier Transform. These current components regard to frequency are given in Table III. The capacitor current components are multiplied by frequency coefficients received from manufacturer, these frequency coefficients are given in Table III. After the multiplications, the products are summed, and the result shown in Table III is calculated as 3.418A. Since the value of 3.418A is lower than the previously calculated value of 3.75A, it is estimated that this capacitor is within safe limits.

TABLE III
FREQUENCY AND CAPACITOR CURRENT RIPPLE RELATION

Frequency	Current [A]	Frequency Coefficients	Frequency coefficient times current [A]
100 Hz	1.944	1.041	2.023
10 kHz	1.698	0.709	1.205
50 kHz and over	0.272	0.699	0.19
TOTAL			3.418

F. Bridge Rectifier Selection

In BPFC, one-phase line voltage is rectified by full-wave (bridge) uncontrolled rectifier. Two diodes always conduct during period. For this reason, the power loss is as much as the products of the voltage drop across the two diodes and the average current. The average current of the bridge rectifier with Equation (42) and power loss with Equation (43) are calculated. Although the amount of loss in the bridge rectifier and the number of semiconductors can be decreased by using bridgeless power factor correcting circuit, but this circuit structure causes EMI to increase. In higher power applications, the bridgeless-interleaved power factor correction circuits can be used to increase the efficiency, they also reduce the magnitude of the input current harmonics and the capacitor voltage fluctuation, but this type of circuitry results in a complex build with the increase the number of components [11].

$$I_{average} = \frac{2}{\pi} \cdot \frac{\sqrt{2} \cdot P_o}{V_{in,\min}} \quad (42)$$

$$P_{bridge} = 2 \cdot I_{average} \cdot V_{drop} \quad (43)$$

G. MOSFET Gate Driver Design

The maximum gate current value that the FAN6982 IC used in the operation can provide is 500mA. This is not a value that is large enough to allow the gate current of the MOSFET to turn-on and turn-off at the desired speeds. Therefore, the maximum turn-on and turn-off currents are increased by installing the Totem Pole structure shown in Fig. 5. As the maximum current of NPN and PNP BJTs is 1,500mA, the maximum transmission and cutting current is increased to 1500mA.

In Figure 5, the R_{g1} resistance limits and protects the PWM source, the R_{g2} resistance provides high impedance between base and collector, and the R_{g5} termination resistance limits oscillations in the gate circuit of totem pole. Following the experiments, the R_{g3} (R_{on}) resistance that determines the t_{on} time is set to 15Ω, and the R_{g4} (R_{off}) resistance that sets the t_{off} time is set to 30Ω.

H. Design of Printed Circuit Board and Hardware Implementation

PCB design is done using Altium Designer drawing program. First of all, all the elements are added to the drawing program with their actual dimensions. This avoids unnecessary gaps between elements, avoiding extra PCB lead

inductance and copper resistances as much as possible. Double-layer PCB drawing is done; the necessary jumpers are passed from the second surface. With the use of a mask and an inner casing, the lifetime of the circuit is increased and the soldering problem that can occur during the building is minimized.

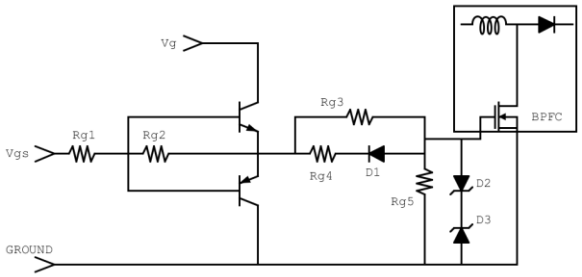

Figure 5: Totem pole gate circuit

One of the factors to be considered in the design and drawing of the PCB is the determination of cycles with high current change (di/dt) and points with high voltage change (dv/dt). The high di/dt current loop is as shown in Figure 6 (a). The parasitic inductances in this cycle are the ones that induce parasitic voltage. For this reason, a capacitor of 100 nF should be added to suppress high frequency components parallel to the output capacitance. Thus, the MOSFET, SiC diode and 100nF capacitances can be designed as close to each other as possible and the parasitic inductance value is reduced as much as possible. The high dv/dt area is shown in Figure 6 (b), where the parasitic capacitances in this region cause noise currents to be generated. PCB design should be made to prevent these areas from forming capacities with ground, earth or other elements. Another factor to note is that the FAN6982 IC's ground used and BPFC's ground must be separated from each other and connected to each other only at one point. In this way, the IC which produces the switching signal will be affected at least from the ground's voltage collapse or voltage rise. In addition, remarkable effects have also been observed when the ground point and the heatsink are connected each other in the design [12].

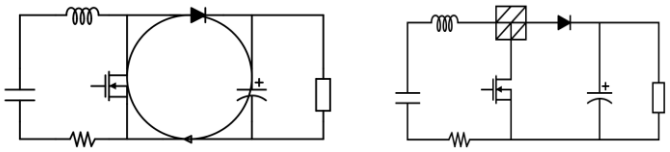

Figure 6: (a) High di/dt loop (b) High dv/dt node

III. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

The PCB electronic circuit designed with Altium Designer program has been printed. The figure of the experimental setup which is realized by hardware is shown in Figure 7. Measurements are performed using Tektronix 2024 as oscilloscope and Fluke 80i as current probe. Figure 8 shows the inductance current and input voltage waveforms when the input voltage is 185V. As can be seen, the effective value of the inductance current is 6.5A as expected. The peak value exceeds the value of 13A and the inductance fluctuation is around 45%, which agrees with the values obtained by analytical calculations. Figure 9 shows the input voltage and input current waveforms when the input voltage is 164V. As can be seen, there is no phase difference between the input current and the input voltage and the noises on the input current is suppressed. The effective value of the input current is about 7.4A and the input power is about 1.213kW. Figure 10 shows the output voltage and output current obtained experimentally. The output voltage fluctuation is around 22V and the calculated value is very close. Similar to the output voltage, the output current has also ripple at 100Hz. The output voltage average is 400V and the output current average is 2.88A, and the output power in this case is 1.152kW.

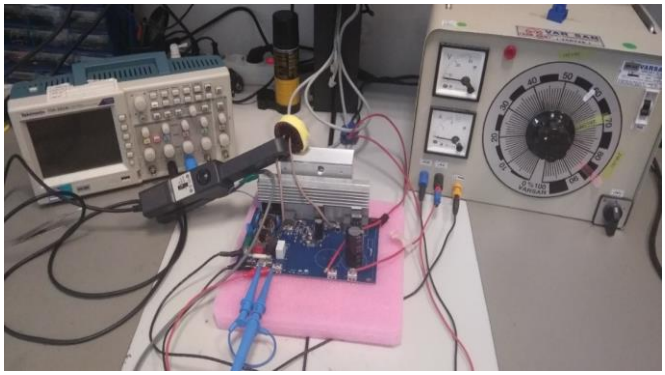

Figure 7: Experimental setup

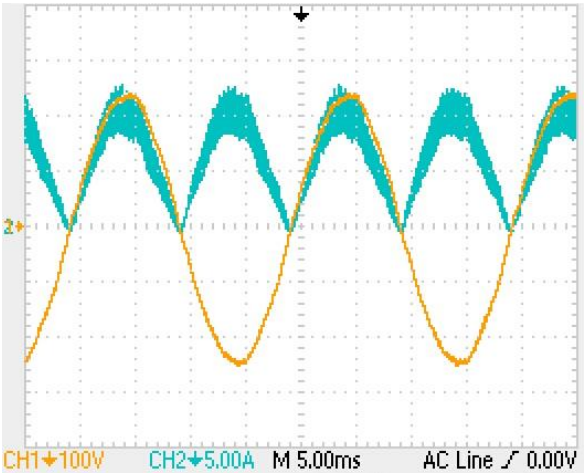

Figure 8: 185V-1,150W – Input voltage (Yellow Line) - inductance current waveforms (Green Line)

Experimental results and simulation results obtained in LTSpice are compared and similarities are observed. Using the LTSpice program, the non-ideal behavior of the switching elements is observed in obtaining the simulation results. In Figure 11, the relationship between input voltage variation and efficiency is measured and compared both in simulation environment and in experimental results. When the results are examined, it is seen that the efficiency is released at 95.5% levels. As the input voltage increases, the required input current value decreases and the efficiency increases at marginal amount.

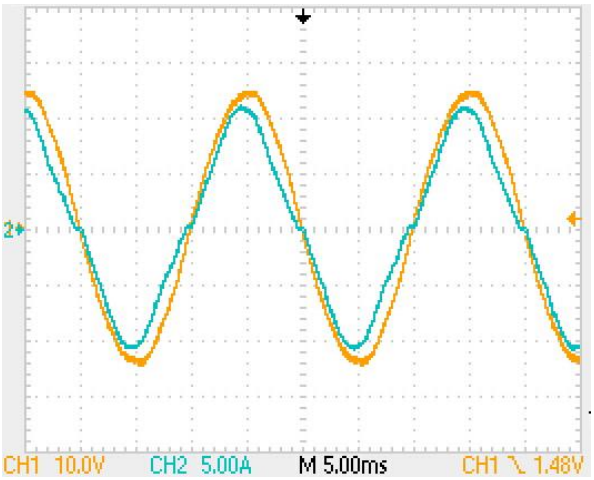

Figure 9: 164V-1,150W – Input voltage (Yellow Line) - input current waveforms (Green Line)

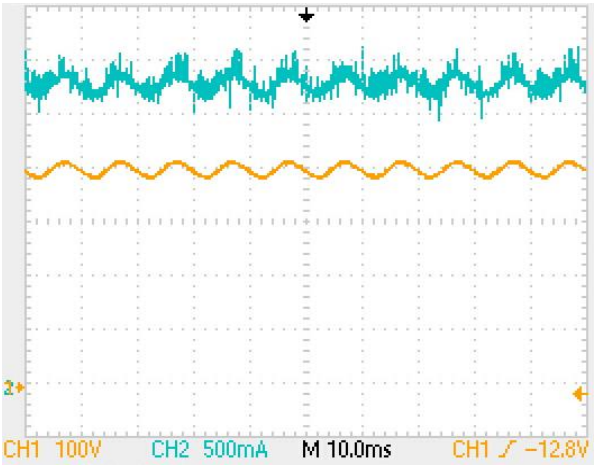

Figure 10: Output voltage (Yellow Line) - current waveforms (Green Line)

The difference of 1.7% between the simulation results and the experimental results can be explained by the lack of the switching loss models in the LTSpice and the modeling of the inductance iron losses with a constant parasitic resistance in the LTSpice program. In Figure 12, the relationship between loading rate and efficiency obtained both experimentally and in LTSpice environment. Even at low load levels, the efficiency is not lower than the 93% level. Thus, it is shown that there is no significant change in efficiency even at low power requirements.

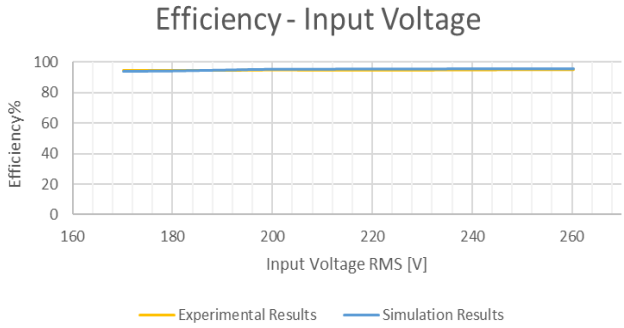

Figure 11: Simulation and experimental efficiency results according to input voltage RMS value

In Figure 13, the total loss analysis is given when the input voltage is 230V. According to this analysis, it is seen that MOSFET is the most lost element with power loss of 21.3W. Then, 9.22W bridge rectifier, 6.05W inductance, 7.6W SiC diode and 10,22W loss capacitor are listed as other important loss components. The total loss amount is around 56W.

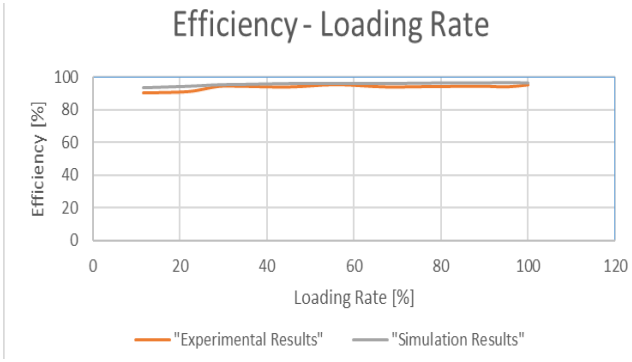

Figure 12: Simulation and experimental efficiency results according to loading rate

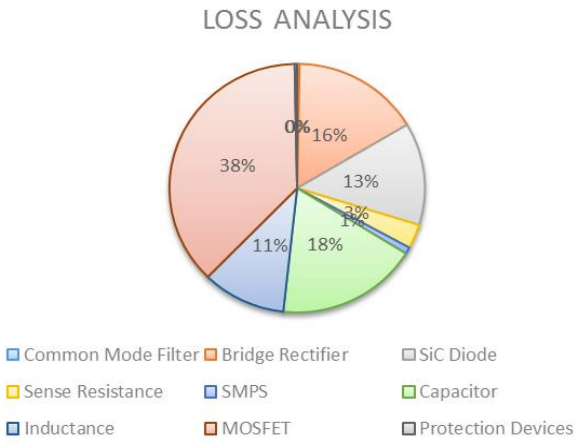

Figure 13: Components losses analysis

IV. CONCLUSION

Cost and efficiency optimization with BPFC has been carried out to design an active filter with increased power density. A detailed loss analysis is performed for each element and the SiC diode reverse recovery current is included in the loss analysis. By using the SiC diode, the reverse recovery current is limited and the efficiency increase is ensured. The analytical equations are given for the maximum current flowing through the elements and the maximum amount of voltage and verified with the model created in the PSIM simulation environment. In order to do losses analysis in the most accurate way, the LTSpice model is constructed. The Fourier analysis of the capacitor current is found in the PSIM environment. The printed circuit board is performed with the Altium Designer program and the experimental results obtained by hardware implementation are compared with the simulation results and verified by checking their compatibility with each other. According to simulation and experiments, it is observed that the system operates between 95% and 95.5%

efficiency. The following recommendations can be applied so that the system to operate at higher total efficiency can be obtained. In the later stages of the design work will be carried out and analyzed.

- BPFC can be changed with the topology that are able to do soft switching during turn-on time so as to eliminate $P_{s,on}$ losses that are 16W in this study [13].
- A MOSFET that has lower conduction resistance can be selected so as to reduce $P_{s,on}$ losses that is 1.61W in this study and also this MOSFET can be parallelled even if less conduction losses are desired.
- A new capacitor that has more capacitance can be replaced with the used 420V, 420μF capacitor that has 10.22W losses, thus voltage ripple and ESR can be decreased. Moreover, this capacitor can be parallelled in order to have less capacitor losses, but this also reduces the power density of system.
- To get rid of the bridge rectifier losses which are 9.22W, bridgeless PFC topology can be used, but this leads to increase in the EMI level and thus volume of EMI filters.

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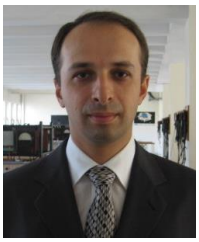
BIOGRAPHIES

BEKİR FINCAN received the B.S. degree from the Electrical Engineering Department, Istanbul Technical University (ITU), Istanbul, Turkey, in 2012, and the M.S. degrees from the same department in 2015. He is now PhD student at the same University.
He is currently a research assistant at the Istanbul Technical University. His research interests power electronics, especially DC/DC converters.



MURAT YILMAZ received the B.S. degree from the Electrical Engineering Department, Istanbul Technical University (ITU), Istanbul, Turkey, in 1995, and the M.S. and Ph.D. degrees from the same university, in 1999 and 2005, respectively.
He is currently an Assistant Professor at the Istanbul Technical University. His research interests power electronics and electrical machines design, control, optimization, and reliability modeling in motor drives and electric drive vehicles including electric, hybrid, and plug-in hybrid electric vehicles.

ALPER GOYNUSEN received the B.S. degree from the Electrical Engineering Department, Yildiz Technical University (YTU), Istanbul, Turkey and the M.S. degree from Electrical Machines and Power Electronics Engineering program from the same department and university in 2011 respectively.
He is currently a senior design engineer in Pavotek Electronics Design Company, and formerly worked in Arcelik and AVL as a design engineer.
His research interests are power electronics and motor drive circuits, analog electronics, soft switching and resonant circuits, analog and digital control theories.

HAYRI KEREM ERENAY received B.S. degree from Electrical Engineering and Electronics, Bosphorus University (BU), Istanbul, Turkey, 1995 and M.S. degree from Bosphorus University Electrical Enginering and Electronics n 1998.
Worked from 1995 – 2013 in Arçelik R&D, power electronics team, motor control and motor based sensing and identification.
From 2014 until now, he is business line manager in power systems group in Pavotek Electronics Design Company, working on motor control and power supply systems.