GU J Sci 30(3): 281-287 (2017)

Gazi University

Journal of Science

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Electrical conduction mechanisms in plasma-enhanced chemical vapor deposited SiO_2 dielectric films

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Article Info

Received: 13/03/2017
Accepted: 24/07/2017

Keywords

PECVD,
SiO2,
Frenkel-Poole emission,
Dielectric

Abstract

In this study, SiO_2 films with thicknesses 50 nm were grown on *n*-GaAs substrate by plasma enhanced chemical vapor deposition technique. To investigate the electrical transport mechanisms, Au/SiO_2/*n*-GaAs (MOS) type capacitor structures were fabricated and measured current density-voltage (*J-V*) characteristics at room temperature. As a function of the applied gate voltage, Schottky emission, Frenkel-Poole emission, and trap-assisted tunneling were found as dominant current transport mechanisms under depletion mode. The obtained trap levels were attributed to defects related with the Ga vacancies formed at the SiO_2/GaAs interface.

PACS: 73.30.+y: 73.40.Qv: 73.40.Ns

1. INTRODUCTION

Silicon dioxide (SiO_2) is a dielectric material and it has played an important role in the development and evolution of microelectronics industry due to its large band gap (~ 9 eV), high melting temperature, and high resistivity [1-8]. Also SiO_2 has been used as an interfacial layer between high-k dielectric materials and substrates [9-14]. On the other hand, gallium arsenide (GaAs) material is one of the III-V semiconductor compounds and due to its superior electron transport properties compared to silicon, much attention has been focused on GaAs based oxide structures such as SiO_2/GaAs. In order to achieve good electronic devices, high-electrically quality SiO2 dielectric films should be achieved, which is very closely related to deposition techniques [15-20].

In the present work, SiO_2 dielectric films were deposited on GaAs by plasma enhanced chemical vapor deposition technique (PECVD). Chemical vapor deposition (CVD) is a multifaceted procedure which is currently used for deposition of metals, composites of nonmetallic materials such as carbon, silicon, carbides, nitrides, oxides, and intermetallics. In the CVD technique, a precursor gas (source gas) flows into a chamber, over the heated substrates to be coated, and deposition of thin films on the surface occurs due to the chemical reaction in vapor phase. On the other hand, PECVD is a hybrid technique which uses electrical energy for producing a plasma, and the produced plasma activates the reaction by transferring the energy of its species to the precursors and induces free radical formation. This technique is one of the low-temperature deposition methods and the advantage of this technique is to deposit silicon oxide with a high deposition rate and at low temperature, that is compatible with a large range of microelectronic-optoelectronic applications [21,22]. Au/SiO_2/n-GaAs MOS capacitor devices were fabricated and current conduction mechanisms causes the leakage current in the devices were investigated at room temperature. Leakage current causes the instability and loss of power in the electronic circuits. The knowledge of the conduction process in the dielectric films and the discovery of the mechanisms that lead to the leakage current are vital important. For this reason, current-voltage (I-V) measurements of the Au/SiO_2/n-GaAs MOS capacitors were performed to extract basic electrical parameters and leakage current conduction mechanisms. In our previous study [23], the leakage current mechanisms in thin (3 nm) SiO_2 films were

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analyzed and Frenkel-Poole emission, ohmic conduction, and space-charge limited conduction mechanisms were found. But in this study, thick SiO_2 (50 nm) films were deposited and found different electrical transport mechanisms.

2. EXPERIMENTAL METHOD

The GaAs substrates were n-type, with (100)-orientated wafers and having a thickness of about 350 µm. The wafers were dipped into ammonium peroxide for a few seconds to remove native oxide layer on the wafer surface. Au/Ge/Ni alloy was evaporated on the back side of the cleaned GaAs substrate and annealed at 430 oC for 40 seconds to perform ohmic contacts. Insulator layer (SiO_2) with a thickness of approximately 50 nm was deposited on the upper surface of the GaAs by using plasma enhanced chemical vapor deposition (PECVD) technique. In PECVD system SiH4 gas and O2 gas were used for Si and oxygen sources, respectively. After deposition the dielectric films, the gold film (thickness ~ 100 nm) was subsequently deposited, using an thermal evaporation source onto the surface of the SiO_2 through holes (1 mm diameter) in the metal mask and current density-voltage (J-V) and capacitance-voltage (C-V) measurements were performed to investigate electrical transport mechanisms.

3. RESULTS AND DISCUSSION

The J-V characteristics of the Au/SiO_2/n-GaAs MOS capacitor devices are given in Fig. 1. As can be seen in fig. 1, current density depends on the applied gate voltage and increases with increasing gate voltage. In ideal case, SiO_2 dielectric films are nearly insulator in which no appreciable leakage current must occur [24]. But, due to insulators are typical dielectric materials, depending on the magnitude of the applied gate voltage, electrical conduction occurs in the dielectric films. In general, these conduction mechanisms were divided into two categories; electrode-limited (conduction occurs due to the electrode/dielectric interface) and bulk-limited (conduction occurs via dielectric defects) conduction mechanisms [24, 25]. In this study, several electrical conduction models were tested to explain the measured J-V curves.

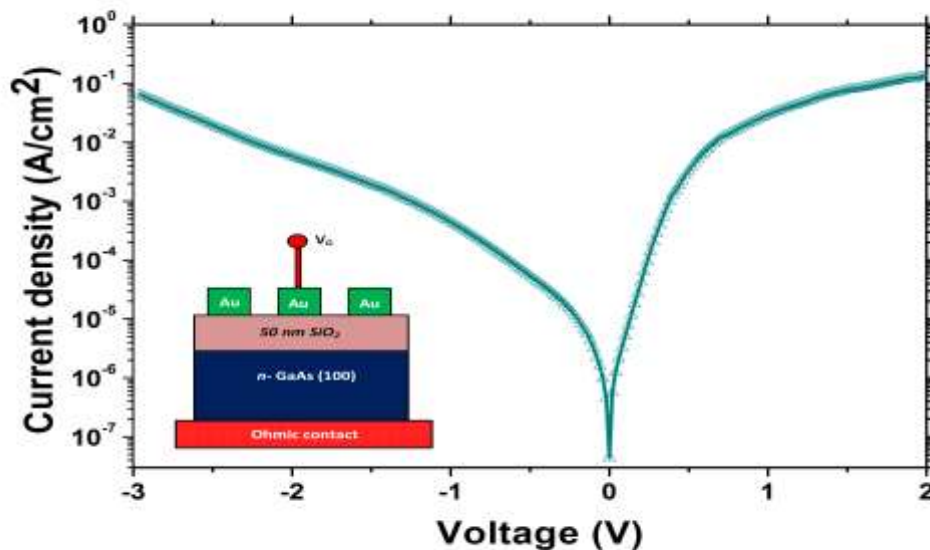

Figure 1 . *J–V characteristics of the Au/SiO₂/n-GaAs capacitor devices*

Under depletion mode, at low electric fields, the Schottky emission (SE) mechanism is described as

$$J \propto A^{*}T^{2}exp\left[\frac{-q\left(\phi_B-\sqrt{qE/4\pi\varepsilon_r\varepsilon_o}\right)}{k_BT}\right] \quad (1)$$

where J, E, A*, ϕB, εr, q, and k are the current density, the electric field, the effective Richardson constant, the barrier height, the dielectric constant of the dielectric films, the electronic charge, and Boltzmann constant, respectively. We point out that having a straight line on the ln (J) versus E1/2 plot does not guarantee SE based conduction. Therefore, it is important to ensure that the obtained dynamic dielectric

constant from the slope of the ln (J) versus E1/2 plot is comparable with static and optical dielectric constants.

Using Eq. (1), εr can be calculated from the ln J vs. E1/2 plot (Fig. 2) if SE applies. From the ln J vs. E1/2 graph, ϕB and εr were calculated as 0.63 eV and 3.36, respectively. This dielectric constant value coincides with the static dielectric constant 3.38, which was obtained from the high frequency (at 1 MHz) Capacitance-Voltage (C-V) measurements as shown in fig.3. The dielectric constant (εr) can be calculated on the basis of the formula as C=εrεoA/d, where, ; C is the capacitance of the films in strong accumulation, A; area of the capacitor (0,00785 cm2), d; thickness of SiO_2 film (50 nm), and εo; permittivity of free space. Thus, we can safely say that the current conduction mechanism in Au/SiO2/n-GaAs capacitor at low electric fields is due to Schottky emission mechnanism. Schottky emission is an electrode-limited conduction mechanism and if the electrons can obtain enough energy provided by thermal activation, the electrons in the metal will overcome the energy barrier at the metal/dielectric interface to go to the dielectric [24].

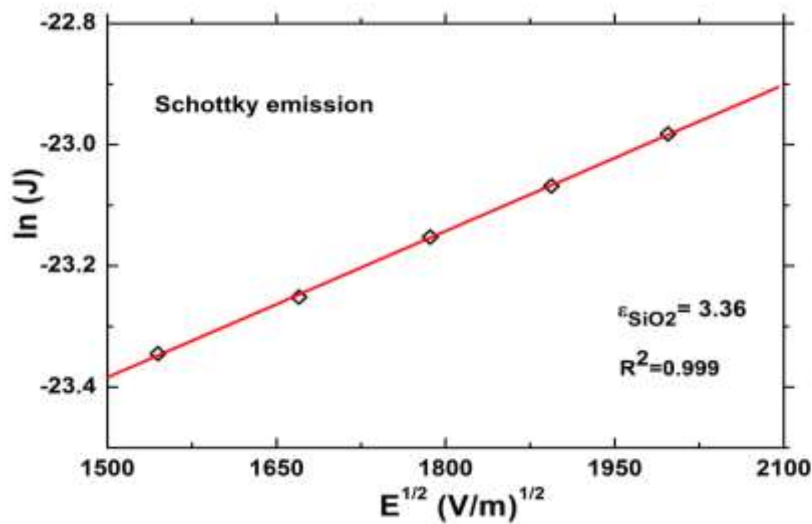

Figure 2. *Schottky emission model fitted for the Au/SiO_2/n-GaAs capacitor devices.*

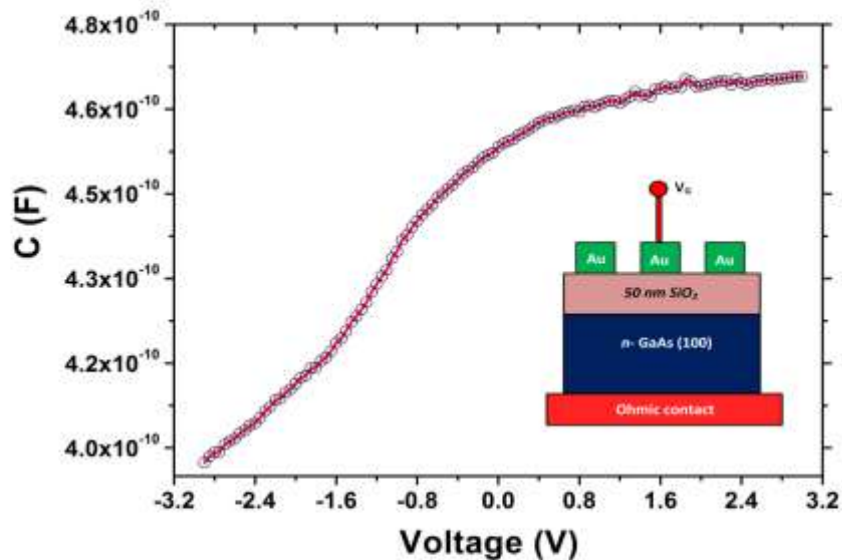

Figure 3. *High frequency (1 MHz) C-V measurements of Au/SiO_2/n-GaAs capacitor devices.*

At medium electric fields, Frenkel-Poole emission (FP) which is a field assisted thermal de-trapping of a carrier from the bulk dielectric material into conduction band can cause the leakage current. Therefore, it is a bulk-limited conduction process. In this mechanism, FP emission can be given as

$$J \propto E exp\left[\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_o})}{k_B T}\right] \tag{2}$$

where ϕ_t is the electrical active trap level within the band gap of the SiO_2. Ln *J*/*E* vs. $E^{1/2}$ plot is given in fig. 4, and according to Eq. (2), the slope of fig. 4 provides an estimate of the dielectric constant of SiO_2 dielectric film. As can be seen in fig. 4, the plot is very well fitted ($R^2 = 0.999$) with the FP mechanism, and ϕ_t and ε_r were calculated to be 0.45 eV and 3.92, respectively.

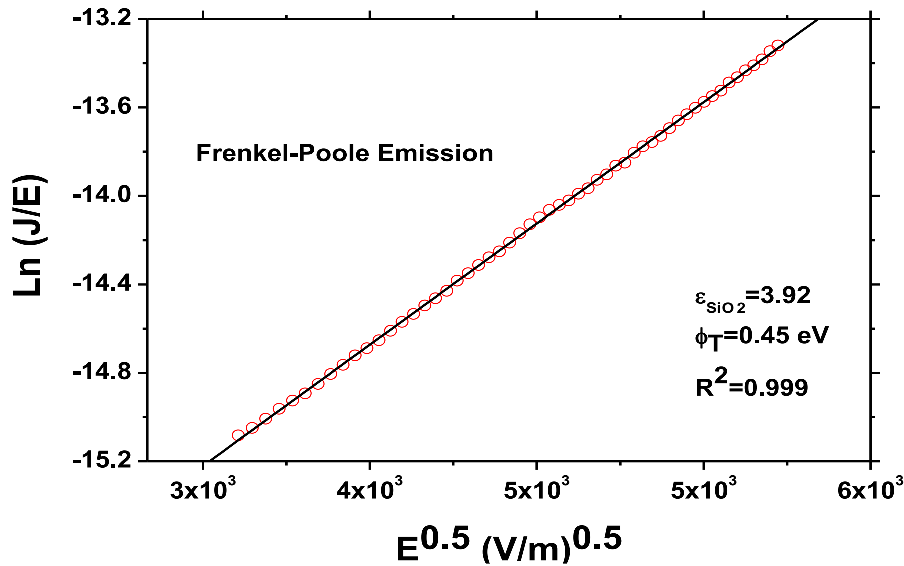

Figure 4. *Frenkel-Poole plot of the Au/SiO₂/n-GaAs capacitor structures*

The calculated dielectric constant value was in good agreement with the static dielectric constants (3.38) and it can be said that the current conduction at medium electric field is due to FP-emission mechanism. The obtained energy level of the electrically active defect states was found as 0.45 eV and this value is coincides with the value reported by Deenapanray [26] and Burkner [27]. They have explained these trap levels with 0.45 eV as excess gallium vacancies (V_{Ga}) defects generated at the SiO_2 /GaAs interface by the migration of gallium atoms into the SiO_2 dielectric films. Therefore, the obtained traps levels at medium electric fields were attributed to Ga atoms in the SiO_2 dielectric films and they cause FP-emission from the dielectric layer into the conduction band of semiconductor.

Finally, at higher electric fields, the current density was fitted by the trap assisted tunneling (TAT). The current due to TAT mechanism is given by

$$J_{TAT} \propto exp\left\{\frac{-8\pi\sqrt{2qm_{AlN}}}{3hE}\phi_t^{3/2}\right\} \tag{3}$$

where $\phi_t$is energy level of the electronic defects in the band gap of the dielectric. Using the Eq. (3), ϕ_t was obtained from Fig. 5 as 0.47 eV.

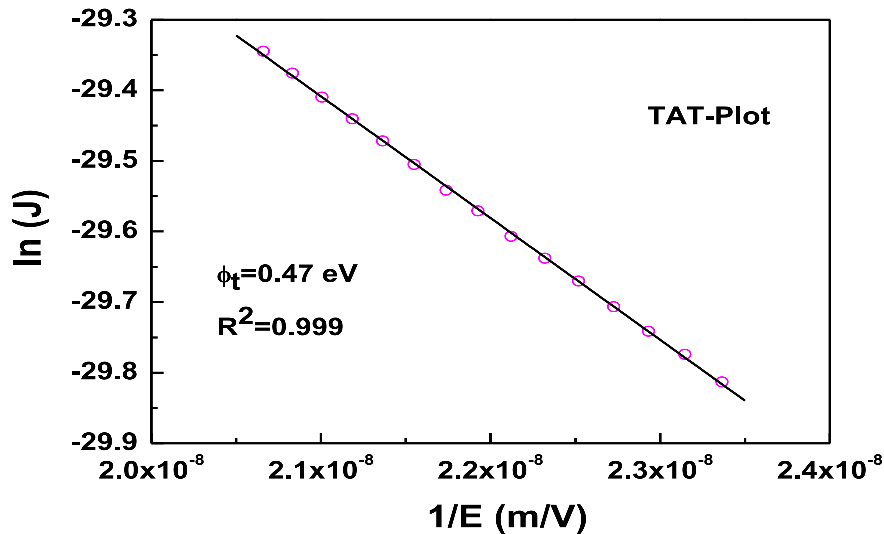

Figure 5. *TAT- plot of the Au/SiO2/n-GaAs capacitor structures.*

The obtained ϕ_t value is very close to 0.45 eV that predicted for V_{Ga} defects generated at the SiO_2 /GaAs interface. In general, the leakage current via tunneling decreases as an exponent function with increasing film thicknesses. But even in a thicker gate dielectric, if the high amount of the traps localized in the dielectric film or at the interface between the dielectric and semiconductor, these traps play an active role in the formation of the leakage current at higher gate electric field. Some studies have been reported related with the current conduction in SiO_2 films. For example, Lim et al. [28] reported that Schottky emission and Frenkel-Poole emission were found as dominant mechanisms in atomic layer deposited SiO2 films at low and high electric field, respectively. In addition, they have stated that the film thickness is one the key parameter which influences on the electrical conduction mechanisms. Ravindra et al. [29] reported that Fowler-Nordheim tunneling was dominant conduction mechanism in SiO_2 films. Perera et al. [30] reported that ohmic conduction, trap-assisted tunneling, and Fowler-Nordheim tunneling was basic conduction mechanisms in nitrided SiO_2 films.

4. CONCLUSION

In this work, SiO_2 dielectric films were deposited on *n*-GaAs substrates by the PECVD technique. Current transport mechanisms of the fabricated Au/SiO_2/*n*-GaAs capacitor structures were investigated over a wide range of applied electric fields under depletion mode. Depending on the applied electric fields, current conduction mechanisms were found as Schottky emission, Frenkel-Poole emission, and trap assisted tunneling. The calculated energy levels of the electronic defects are attributed to the excess vacancies (V_{Ga}) generated at the SiO_2 /GaAs interface by the out-diffusion of Ga atoms into the SiO_2 dielectric films.

ACKNOWLEDGMENTS

The Authors would like to thank Michael Schneiderman at Submicron Research Center at Weizmann Institute of Science for SiO_2 coating by PECVD. This study was supported by the Turkish Prime Ministry state Planning Agency under project no: 2001K120590 and The European Transnational Access Program # RITA-CT-2003-506095 WISSMC.

CONFLICT OF INTEREST

No conflict of interest was declared by the authors

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