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The thickness effect of insulator layer between the semiconductor and metal contact on *C-V* characteristics of Al/Si_3N_4/p-Si device

Al/Si_3N_4/p-Si aygıtının *C-V* characteristikleri üzerine metal ile yarıiletken kontak arasındaki yalıtkan tabakanın kalınlık etkisi

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Abstract

Metal-insulator-semiconductor (MIS) structures have great interest for their good applications in electronic and optoelectronic. Their importance can be attributed that they have storage layer property, capacitance effect and high dielectric constant. For this reason, two samples of Si_3N_4 layers were deposited with plasma-enhanced chemical vapor deposition (PECVD) technique on p-type Si; first is about 5 nm thickness and the other is about 50 nm. The thicknesses of Si_3N_4 were adjusted by an ellipsometer. The thickness effect of Si_3N_4 layers on the Al/Si_3N_4/p type Si contact was studied with the capacitance-voltage (C–V) and conductance–voltage (G-V) characteristics of the contact at the frequency range from 10 kHz to 1 MHz and applied bias voltage from −5 V to +5 V at room temperature. In each contact having different insulator layers, capacitance values decreased and conductance values increased with increasing frequencies. The interface states (N_{ss}), the effect of series resistance (R_s), barrier height (Φ_b) and carrier concentration (N_a) were found from the capacitance-voltage (C–V) and conductance–voltage (G-V) measurements and explained in the details. To determine memristor behavior of the Al/Si_3N_4/p type Si contact, dual C-V and G-V measurements were performed at 500 kHz and the room temperature, and the results were compared for 5 nm and 50 nm thicknesses layers. Consequently, changing of Si3N4 layer thickness influenced properties of the contacts, and these two contacts have memristor behavior and, they can be used and improved as memory devices in the future.

Keywords: Al/Si_3N_4/p- Si, Schottky, Capacitance behavior, MIS, Thickness effect

Öz

Metal-Yalıtkan-Yarıiletken (MIS) yapılar elektronik ve optoelektronikteki iyi uygulamalarından büyük ilgiye sahiptirler. Bu yapıların önemi tabaka depolama özelliği, kapasitans etkisi ve yüksek dileketrik sabitlerine sahip olmalarına dayandırılabilir. Bu yüzden Si_3N_4 tabakalı iki adet numune plazma destekli kimyasal buhar biriktirme (PECVD) yöntemiyle birinin kalınlığı 5 nm diğerinin kalınlığı 50 nm olacak şekilde p-tip Si üzerine büyütüldü. Si_3N_4 tabakasının kalınlığı bir elipsometreyle kontrol edildi. Al/Si_3N_4/p tip Si kontağın üzerine Si_3N_4 tabakasının kalınlık etkisi 10 kHz-1 MHz frekans değerleri için -5 V'tan +5 V voltaj aralığında yapıların kapasitans-voltaj (C–V) ve iletkenlik-voltaj (G–V) karakteristikleri ile oda sıcaklığında araştırıldı. Farklı kalınlığa sahip kontakların her bir durumda kapasitans değerlerinin artan frekansla azaldığı ve iletkenlik değerlerinin arttığı tespit edildi. Ara yüzey durumları (N_{ss}) ve Seri direnç (R_s) etkileri, bariyer yüksekliği (Φ_b) ve taşıyıcı yoğunluğu (N_a) kapasitans-voltaj (C–V) ve iletkenlik-voltaj (G–V) karakteristikleri karakterizasyonlardan elde edildi ve açıklandı. Ayrıca 5 nm ve 50 nm kalınlık değerindeki tabakalar için 500 kHz frekansta çift yönlü C-V ve G-V karakterizasyonlarından elde edildi ve kıyaslandı. Sonuç olarak, Si_3N_4 tabakasının kalınlık değişiminin kontakların özelliklerini etkilediği görüldü ve bu kontakların Memrezistör yapısına sahiptirler ve gelecekte hafıza aygıtları için kullanılabilir ve geliştirilebilirler.

Anahtar kelimeler: Al/Si_3N_4/p- Si, Schottky, Kapasitans özelliği, MIS, Kalınlık etkisi

1 Introduction

Schottky diodes and metal-semiconductor devices have good properties for using in the electronic industry such as low voltage rectifiers, inverters in high frequency, solar cells, polarity protection and freewheeling diodes [1],[2]. Past to present, schottky diodes or contacts have attracted the interest on their conduction mechanism and barrier height and, they have been mostly investigated several times by many researchers [3]-[7].

Properties of metal and semiconductor contacts can be changed by use of interfacial insulator layers [8]. SiO_2, Si_3N_4, SnO_2, TiO_2 and $SrTiO_3$ etc. are used as insulator layers between semiconductor and metal contacts and, these layers causes to deviate from the ideal structure of the contact and provide new properties to them [9].

To better understand the metal and semiconductor contacts, their conduction mechanism and barrier height should be known. There are various parameters to explain their current conduction mechanism and barrier height such as doping concentration of atoms, interface layer, interface states density, series resistance, temperature effect, applied bias voltage and homogeneity and thickness of the insulator layer. If insulator layers are ≤100 Å thicknesses, they could be called a metal–insulator-semiconductor (MIS) structure [10] otherwise, they are called metal-oxide-semiconductor (MOS) structure [11]. One of most important characteristics of insulator layers in the MIS structure are having dielectric property which is resemble a capacitor. If an insulator layer in the MIS is very thin (˜30 Å), electrical parameters of this structure can be determined by current-voltage (*I–V*) and capacitance-voltage (*C-V*) measurements. But the existence of more thickness insulator layer at the interface, (*I–V*) measurements cannot be used.

The aim of this study, to investigate Al/Si_3N_4/p type Si contact according to 5 nm and 50 nm insulator layer thicknesses at room temperature because of understanding changing performance and quality of these devices depending on its thicknesses.

2 Materials and methods

p-type Si wafers which were polished and cleaned for the deposition of the Al/Si_3N_4/p type Si heterojunctions have (100) orientation and 7.3 x 10^{15} cm^{-3} carrier concentration according to manufactures specifications. The wafers were degreased consecutively in acetone and isopropyl alcohol with ultrasonic cleaner for 5 min. The degreased wafers were etched with HF:H_2O (1:10) for 30 second to take out the surface damages and undesirable impurities. Before ohmic contact, the p-type Si wafers were cut into pieces of 1.0 cm length by 1.0 cm breadth. Aluminum was evaporated (thermal) on other sides of the p-type Si for the ohmic contact and the p-Si/Al were annealed at 450 °C for 3 minute in N_2 ambience. The Al contacts have been formed by thermal evaporation method as points with diameter of around 1.0 mm on the front surface of the p-Si wafers. The thickness of metal coating was designated with a quartz screen positioned in close intimacy to the Si.

The insulator layers have been formed PECVD technique on p-type Si nearly 5 nm and 50 nm thicknesses. (The ratio of Si_3N_4 (SiH_4:NH_3, (185:45 sccm)). The schematic diagram of contacts could be seen in Figure 1. The *C–V* and *G–V* measurements of the diodes were performed by using HP 4192 A LF Impedance Analyzer.

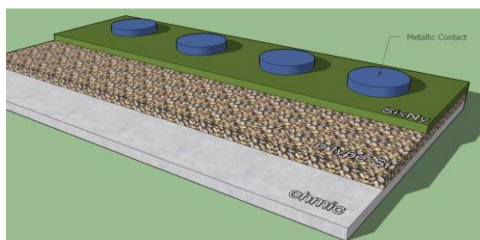

Figure 1: Schematic diagram of Al/Si_3N_4/p-Si device.

3 Results and discussion

The *C–V* characteristics of having 5 and 50 nm thicknesses Al/Si_3N_4/p-Si contacts have been shown in Figure 2(a) and Figure2(b), respectively. It can be said that capacitance properties of two contacts affected bias voltage and frequency alterations. As shown in Figure 2(a) and Figure 2(b), capacitance values have decreased with increasing (10 kHz to 1 MHz) frequencies in the accumulation and depletion regions. These decreasing can be attributed to the interface states and interfacial native Si_3N_4 layers between semiconductor and metal. In the high frequencies, interface states cannot follow ac signals and this causes low capacitance values [12]. The values of capacitances have shown each frequency, changing forward to reverse bias for having 5 nm thicknesses Si_3N_4 layers but in having 50 nm thicknesses Si_3N_4 layer, there is no any capacitance peaks changing applied bias that can be attributed increasing native layer thickness 5 nm to 50 nm [11],[13].

The *G-V* plots of the Al/Si_3N_4/p type Si contacts could be seen in Figure 3 for having different thicknesses Si_3N_4 layers. It has shown that conductance values increased with increasing frequencies for 5 nm and 50 nm native layer thicknesses. This increasing can be ascribed not following ac signal in the high frequencies. In 5 nm thicknesses Si_3N_4 layer could be observed peaks in the depletion region in all frequencies and these peaks have tendency to reverse bias voltage with increasing frequency. However, in 50 nm thicknesses Si_3N_4 layer; there are no seeing peaks at the *G-V* plots. This conclusion attributed also increasing native layer effect [11],[14].

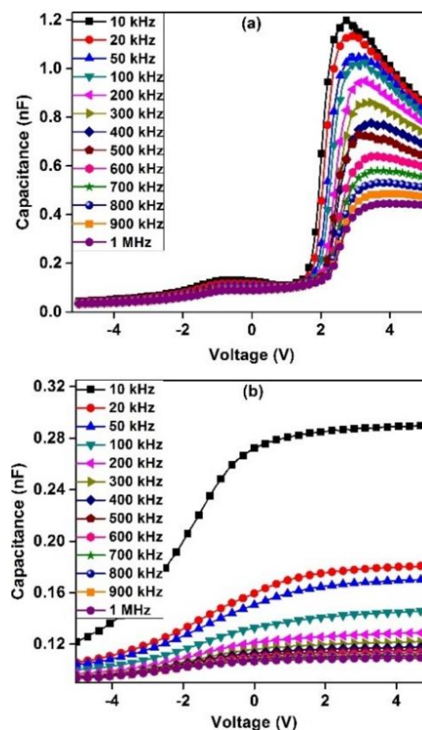

Figure 2: The capacitance-voltage (C–V) characteristic different frequencies for having 5 nm (a) and 50 nm (b) thicknesses Si_3N_4 layers in Al/Si_3N_4/p type Si contacts

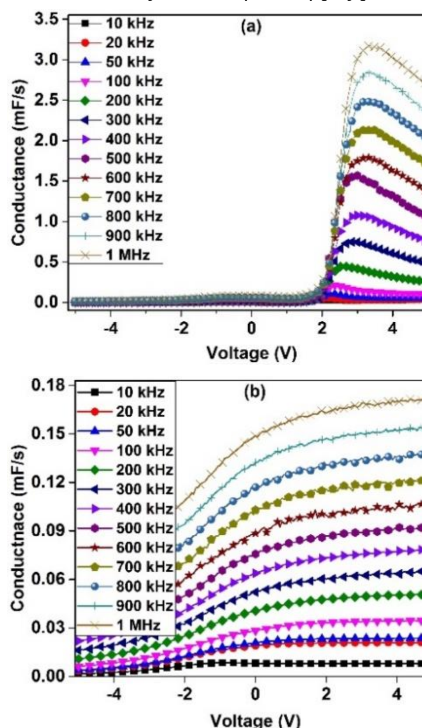

Figure 3: The conductance-voltage(*G–V*) characteristics of having 5 nm (a) and 50 nm (b) Al/ Si_3N_4/p type Si contacts.

R_s versus bias voltage plots have been displayed in Figure 4 for having 5 nm and 50 nm layer thicknesses Si_3N_4 insulator between the metal and semiconductor. R_s is given depending conductance and capacitance by:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \tag{1}$$

in here G_{ma} and C_{ma} are measured conductance and capacitance, respectively and ω is angular frequency equal to $2\pi f$. Variations at $R_s$values can be explained that these values deviated from ideal condition and affected from different insulator layers. As can be seen in Figure 4(a), R_s have given a peaks definite voltage interval where interface states can follow ac signal at low frequency, but in the high frequencies, ac signal cannot be followed by interface states and, R_s values do not exhibit peaks. Magnitudes of peaks have increased and peaks positions have changed with negative bias voltage with decreasing frequency. In Figure 4(b), it could be seen only two peaks in 10 and 20 kHz frequencies at the accumulation region, but there is no peak in the high frequencies. This can be attributed not pursuing ac signal at high frequency values and do not exhibiting peaks more insulator layers [5],[15].

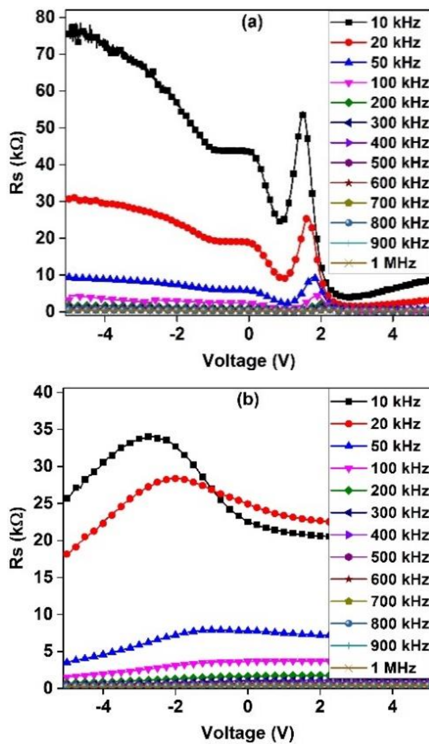

Figure 4: The series resistance (Rs) changing of having 5 nm (a) and 50 nm (b) Al/Si3N4/p type Si contacts with voltage.

C^{-2}–V graphs of Al/Si_3N_4/p type Si contacts have been given in Figure 5(a) and Figure 5(b) for having 5 nm and 50 nm insulator Si_3N_4 layers, respectively. As known that C^{-2}–V plots exhibit a straight line in a wide bias range and diffusion potential can be found extrapolation of this line to the voltage axis. Using the slope of this line can be calculated various parameters such as barrier height, fermi level and doping concentration [12]. These values have been given in Table 1 and Table 2 for 5 nm and 50 nm native layers, respectively. It can be observed that voltage axis extrapolation have changed reverse bias to forward bias by increasing thicknesses of Si_3N_4 layers from 5 nm to 50 nm. As can be seen at Figure 5(b), C^{-2}–V plots have exhibited non-linear curve tendency to high frequencies. This case can be attributed non-uniform doping or not following ac signal at high frequencies by interface states [16].

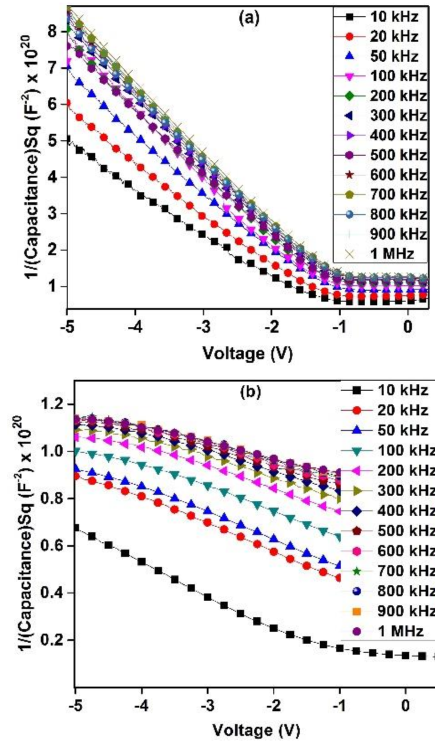

Figure 5: The C^{-2}–V graphs at different frequencies for 5 nm (a) and 50 nm (b) Al/Si3N4/p type Si contacts.

Figure 6(a) and Figure 6(b) has been shown changing values of barrier height (Φ_b) and doping concentration (N_a) values with frequency for different thicknesses insulator layers. In Figure 6a for 5 nm insulator layers, barrier height and doping concentration values decreased with increasing frequency coherently each other. It can be said also that barrier height decreased and doping concentration increased with increasing frequency for 50 nm insulator layers (Figure 6(b)). Incoherently changing for having 50 nm thicknesses layers can be attributed the distribution of particular density in interface states and interfacial layer effects [5]. Values of Φ_b and $N_a$could be seen in Table 1 and Table 2 at various frequencies for 5 nm and 50 nm Si_3N_4 layers.

Figure 7(a) and Figure 7(b) have indicated N_{ss} versus frequency which is obtained Hill-Coleman technique for 5 nm and 50 nm Si_3N_4 layers. From this technique N_{ss} values accounted below formula:

$$N_{ss} = \frac{2}{qA} \frac{(G_m/\omega)_{max}}{((G_m/\omega)_{\max} C_{0x})^2 + (1 - C_m/C_{0x})^2} \tag{2}$$

in here, A is diode area, ω is angular frequency, G_m and $C_m$are measured conductance and capacitance, respectively. C_{0x} is native layer capacitance obtained from below equation at accumulation region (4 V):

$$C_{0x} = C_{ma} \left[\frac{G_{ma}^2}{(\omega C_{ma})^2} \right] \tag{3}$$

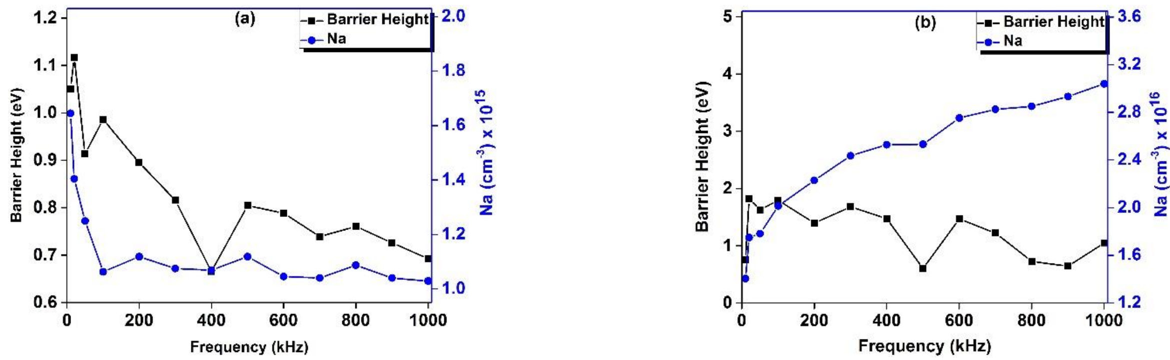

Figure 6: Changing of barrier height and doping concentration values with frequency for having 5 nm (a) and 50 nm (b) Al/Si3N4/p type Si contacts.

Table 1: The experimental parameters obtained from for 5 nm native layer thickness.

f (kHz)	N_a (10^{15} cm^{-3})	V_i(V)	E_F (meV)	$\Delta\Phi_b$ (meV)	Φ_b (eV)	E_m (10^4 V/m)	N_{ss} (10^{10} eV^{-1} cm^{-2})
10	1.645	0.863	178	15.85	1.051	2.077	8.469
20	1.404	0.970	189	15.69	1.117	2.035	5.544
50	1.249	0.762	192	14.34	0.914	1.701	3.363
100	1.063	0.830	196	14.07	0.986	1.637	2.422
200	1.119	0.740	195	13.85	0.895	1.586	1.948
300	1.075	0.659	196	13.32	0.816	1.467	1.824
400	1.069	0.508	196	12.47	0.666	1.285	1.800
500	1.119	0.649	195	13.40	0.804	1.485	1.881
600	1.046	0.631	196	13.09	0.788	1.416	1.866
700	1.040	0.581	197	12.80	0.739	1.355	1.930
800	1.087	0.604	195	13.07	0.761	1.412	1.967
900	1.040	0.568	197	12.73	0.726	1.340	2.066
1000	1.029	0.534	197	12.50	0.693	1.292	2.160

Table 2: The experimental parameters obtained from for 50 nm native layer thickness.

f (kHz)	N_a (10^{16} cm^{-3})	V_i(V)	E_F (meV)	$\Delta\Phi_b$(meV)	Φ_b (eV)	E_m (10^4 V/m)	N_{ss} (10^{10} eV^{-1} cm^{-2})
10	14.04	0.630	123	25.04	0.753	5.185	54.51
20	17.49	1.760	124	34.20	1.823	9.672	39.68
50	17.82	1.563	123	33.36	1.627	9.198	23.36
100	20.15	1.737	120	35.32	1.796	10.31	20.59
200	22.30	1.340	117	33.95	1.397	9.528	19.91
300	24.36	1.627	115	36.43	1.680	10.97	19.58
400	25.28	1.420	114	35.54	1.473	10.44	21.98
500	25.32	0.542	114	27.95	0.602	6.457	23.19
600	27.53	1.420	112	36.31	1.470	10.90	21.54
700	28.25	1.170	111	34.82	1.220	10.02	17.91
800	28.51	0.672	111	30.38	0.727	7.629	16.34
900	29.33	0.587	110	29.58	0.642	7.233	13.84
1000	30.40	1.000	109	34.10	1.049	9.611	12.51

In Figure 7(a), N_{ss} values decreased with increasing frequencies then become constant nearly at high frequencies, but increasing native layers from 5 nm to 50 nm on the contacts (Figure 7(b)), N_{ss} values decreased at 20 kHz frequency and increased again at 50 kHz frequency then become constant to high frequencies after again decreased little. These changing in the interface states attributed not homogeny interfacial layers in the contacts for having 50 nm native layers [17],[18]. N_{ss} values for 5 nm and 50 nm Si_3N_4 layers have been tabulated for different frequencies also in Table 1 and Table 2, respectively.

R_s values can be calculated Equation (1) and R_s versus frequency plots have been shown in Figure 8(a) and Figure 8(b) obtained this formula (Eq. 1) for strong accumulation region for 5 nm and 50 nm native layer thicknesses, respectively. It can be seen from these plots that R_s values decreased exponentially nearly each thickness cases. In it is having 50 nm native layer thicknesses contact, there is a deviation from exponential case in the 20 kHz frequency. This condition can be attributed to inhomogeneous interface states at having more native layer thicknesses [19], [20].

It has been observed in Figure 9 that dual capacitance and conductance characteristics at 500 kHz frequencies for having 5 nm and 50 nm native insulator layer thicknesses because of investigating the memristor behavior. Memristor has low power and nonvolatile operation, variety of physical mechanisms and potentially high density, placing advanced components of future computing systems [21]. Si_3N_4 is commonly used memory contacts for memristive characterizations. In the capacitance-voltage measurements for having 5 nm layers contact has a peak and memory window in the strong accumulation region but 50 nm layers contact has no peak and it has memory window wide voltage range in inversion, depletion and accumulation region and dual plots of conductance-voltage have similar the *C-V* plots have been indicated in Figure 9. It can be said that increasing Si_3N_4 layers causes changing the memory window position with increasing thickness. This changing has been seen in Figure 9 to reverse bias region.

The some experimental parameters were calculated and given in Table 1 and Table 2 for having 5 nm and 50 nm native layers contacts for various frequencies. In the Tables, V_i values are obtained extrapolation of C^{-2}-V plots to the voltage-axis. Fermi energy levels (E_F) can be accounted from below equation:

$$E_F = \frac{KT}{q} Ln\left(\frac{N_v}{N_a}\right) \tag{4}$$

by using,

$$N_v = 4.82 \text{ x } 10^{15} T^{3/2} \left(\frac{m_h^*}{m_0}\right)^{3/2} \tag{5}$$

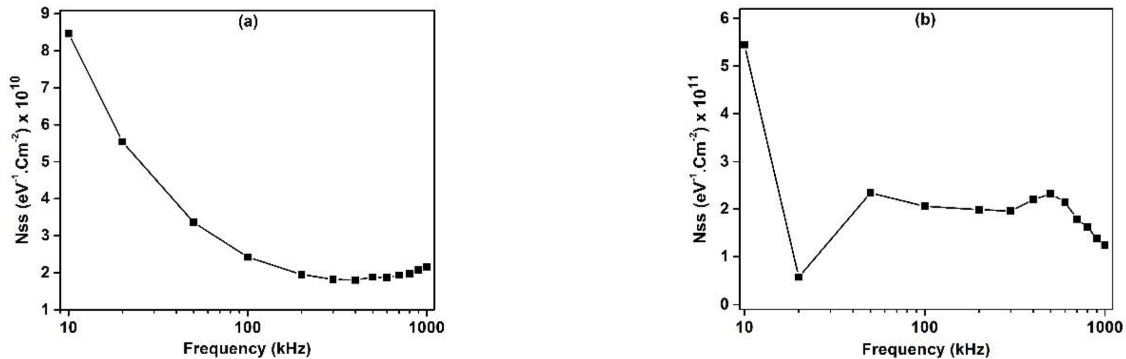

Figure 7: Variation of N_{ss} values with frequency of having 5 nm (a) and 50 nm (b) Al/Si_3N_4/p type Si contacts.

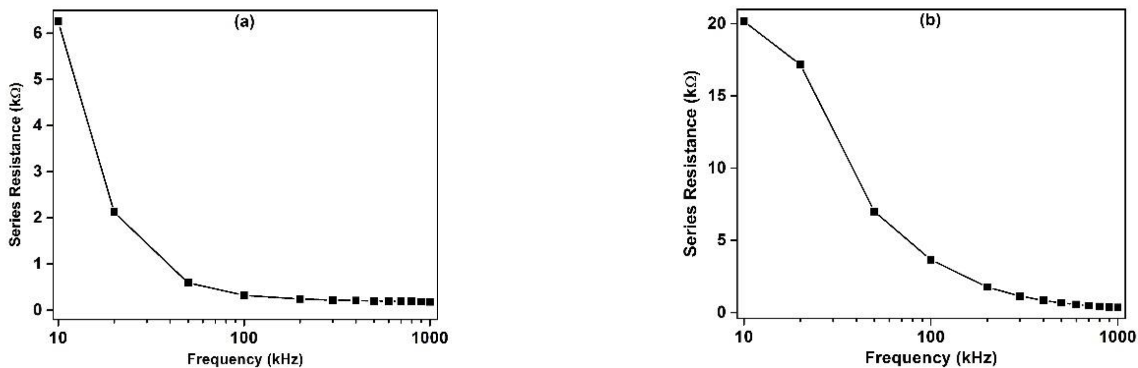

Figure 8: Alteration of R_s values with frequency for having 5 nm (a) and 50 nm (b) native layers Al/Si_3N_4/p type Si contacts.

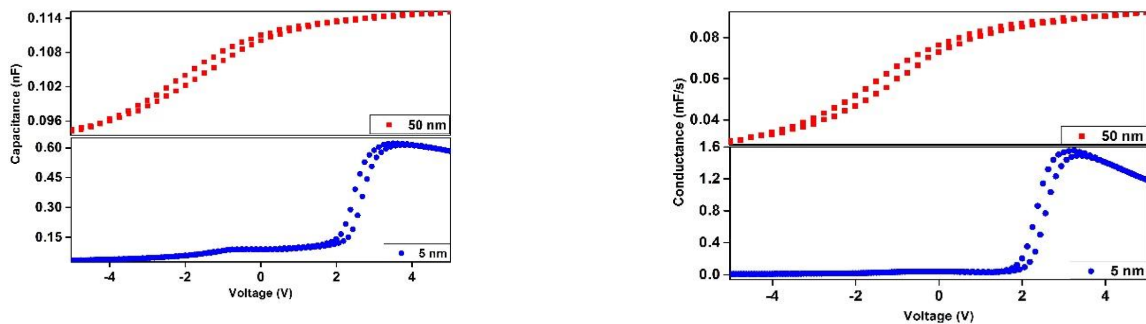

Figure 9: Dual capacitance-voltage and conductance-voltage characteristic for having 5 nm and 50 nm Al/Si_3N_4/p type Si contacts at 500 kHz.

Where N_v is the efficient density of states for Si valance band and value of N_v is 1.04 x 10^{19} cm^{-3}. m_h^* and m_0 (in here m_h^*= 0.16 m_0) are the effective masses of the electrons and halls, respectively. E_F values almost have increased with increasing frequencies for having 5 nm Si_3N_4 layers and it can be seen in Table 1. Values of E_F obtained from having 50 nm native layers contact have decreased by increasing frequency attributing to the increasing doping concentration because of thicker native layer can be observed in Table 2 [22]. E_F values of Al/Si_3N_4/p type Si contacts have decreased with increasing native Si_3N_4 layers from 5 nm to 50 nm could be seen comparing Table 1 and Table 2. This decreasing can be attributed interfacial insulator layer effects between metal and semiconductor.

$\Delta\Phi_b$ is the image force barrier lowering and is given by:

$$\Delta\Phi_b = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right]^{1/2} \quad (6)$$

where E_m is the maximum electric field and calculated with:

$$E_m = \left[\frac{2qN_aV_i}{\varepsilon_s\varepsilon_0}\right]^{1/2} \quad (7)$$

$\Delta\Phi_b$ values almost has linear decreasing by increasing frequency (Table 1) ascribing lower layer effects for having 5 nm Si_3N_4 layers. In 50 nm, there are a lot of fluctuations (Table 2) because of imaging barrier lowering and non-homogenous interface states [23].

Using of V_i values, the diffusion potentials (V_d) at zero bias can be found by use of below equation:

$$V_d = V_i + \frac{KT}{q} \quad (8)$$

After accounting of V_d, E_F and $\Delta\Phi_b$, the values of barrier heights Φ_b (C–V) could be obtained from below relation:

$$\Phi_b(C-V) = V_d + E_F - \Delta\Phi_b \quad (9)$$

Calculated Φ_b values of contacts have been shown in Table 1 and Table 2 for having 5 nm and 50 nm Si_3N_4 layers contacts, respectively. From these tables, it can be seen that there is almost regularly decreasing the Φ_b values, can be ascribed lower native layers, in having 5 nm native layers between metal and semiconductor. But at having 50 nm native layers, there are many floating in barrier height values could be seen in Table 2. This case also can be based on thicker layers and inhomogeneous of interface states or interfacial layer effects [23].

4 Conclusions

The thickness layer effect of Si_3N_4 insulator layer of the Al/Si_3N_4/p-Si contacts were investigated with capacitance-voltage (C–V) and conductance–voltage (G–V) characteristics of the structures at various frequencies and applied bias voltage ranges at room temperature. Changing the Si_3N_4 layer thickness has affected C-V and G-V characteristics of the contact. Capacitance values decreased and conductance values increased with increasing frequencies for 5 and 50 nm Si_3N_4 layers contacts. There are peaks all frequencies in having 5 nm native layers, but adding 50 nm insulator layer between the metal and semiconductor has not shown any peaks. The interface states (N_{ss}) values have decreased with increasing frequency for contacts having various layers thicknesses. The diode parameters such as series resistance (R_s), barrier height (Φ_b) and carrier concentration (N_a) were plotted versus frequency. It can be said that these and other some accounted parameters were affected having different native layers thicknesses. It was also measured and compared C–V and G–V characterizations dual measurement at 500 kHz in room temperature for 5 nm and 50 nm thickness layers. These contacts have similarly memristor structure and can be used as memory devices.

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