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ELECTROTHERMAL CHARACTERIZATION OF PHASE-CHANGE FILMS AND DEVICES

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ABSTRACT

The reversible changes in the optical properties of the phase-change materials have made the rewritable optical storage possible which has revolutionized the dissemination of data since 1990s. For the last two decades, the phase-change materials have been studied extensively for its applications as nonvolatile memory elements (phase-change memory, PCM, devices). While the PCM devices were initially considered as replacements for the flash memory, today they promise a universal memory acting as the main memory and the storage unit. Here we demonstrate a simple alternative to study phase-change films and devices for further fundamental studies. The films are deposited using a single sputtering target and the devices are formed using single lithography, deposition and liftoff steps. The room-temperature electrical resistivity values are characterized as 5 kΩ.cm for amorphous phase, 0.5 Ω.cm for cubic-crystalline phase, 4 mΩ.cm for hexagonal-crystalline phase. The phase-transition temperature values are observed as ~150 °C for the amorphous-cubic crystalline transition and ~200 °C for the cubic-hexagonal transition while varying the film temperature from room temperature to 250 °C. Finally, microscale GST wires are amorphized by self-heating-induced melting and quenching. The electrical current density during amorphization is calculated as $\sim 6\times10^{10}$ A/m^2.

Keywords: Phase-change devices, Nonvolatile memory, Electrothermal effects

1. INTRODUCTION

Phase-change materials exhibit reversible amorphous to crystalline phase transitions. The phase transition is accompanied by a large change in the electrical and the optical properties of the materials. For instance, the electrical resistivity of $Ge_2Sb_2Te_5$, or GST, the most commonly used phase-change material, is $\sim 10^3$ Ω.cm in the amorphous phase, ~0.1 Ω.cm in the face-centered cubic (fcc) crystalline phase and ~ 10^{-3} Ω.cm in the hexagonal crystalline phase [1]. While the phase-change-induced optical properties have been the main enabler of the rewritable optical data storage media, such as RW-CDs, DVDs, and Blu-ray discs [2]; the large variation in the electrical resistivity has enabled the phase-change memory (PCM) devices which is an alternative nonvolatile memory technology to the technology standard flash memory [3]. The operation of the PCM devices relies on the change in the electrical resistance as the active volume within the phase-change material is switched between the low-resistivity fcc crystalline phase and the high-resistivity amorphous phase. Amorphization is achieved by applying a large amplitude, short duration (~ns) electrical pulse that brings the active volume temperature above the melting temperature which quickly drops down to the ambient temperature upon termination of the pulse. Quenching the active volume is necessary for successful amorphization. Crystallization, on the other hand, requires a longer duration (~100 ns) electrical pulse that brings the active volume temperature to a high level below the melting temperature. The actual amplitudes of the electrical pulses depend on the device dimensions.

For nonvolatile memory applications, a vertical geometry is preferred to scale down the footprint of each device, hence to increase the storage capacity (bytes per area) (Figure 1). Fabrication of the vertical devices is, however, challenging as it involves multiple deposition, patterning, and etching steps [4]. The lateral devices, on the other hand, offers an easy fabrication route as they can be fabricated by patterning the metal contacts and the GST layer (Figure 1). The lateral geometry is particularly advantageous for studying the fundamental aspects of the PCM devices such as the temperature-dependent crystallization dynamics [5],

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reduction of amorphization current [6], and resistance drift [7,8]. Furthermore, electron microscopy imaging of the PCM cells is more convenient with the lateral geometry, which sheds light on the device operation either by *in-situ* [9] or *post-mortem* imaging [10]. Beside the fundamental studies, the lateral geometry is preferred for applications of PCM devices other than the nonvolatile memory functionality, such as electrical switches [11], and color pixel structures [12]. Here we offer a simple fabrication route for lateral PCM devices using single photolithography, sputtering, and liftoff steps. We start our study by investigating the films deposited by a sputtering system using a single target.

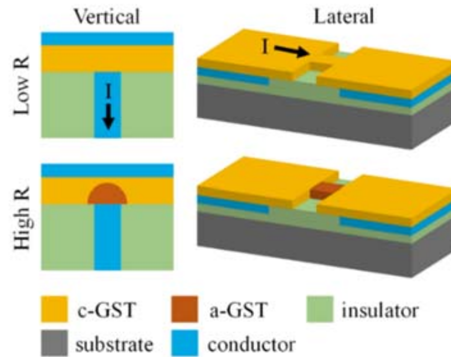

Figure 1. Cross-section illustration of the vertical geometry and 3D illustration of the lateral geometry. The GST layer is capped with an insulator layer that is not shown here for clarity. Top row illustrates the low resistance state with the GST layer in crystalline phase and the bottom row illustrates the high resistance state with an amorphous GST volume blocking the current path. Arrows indicate the electric current directions for read/write/erase operations.

2. DEVICE FABRICATION

Prior to the GST deposition, Si substrates are covered with SiO_2 insulating films using a plasma enhanced chemical vapor deposition system (PECVD). The SiO_2 film thickness is chosen to be thick (~1 μm) to avoid electrical breakdown. Then, the SiO_2 on Si substrates are used to characterize the GST deposition rate as a function of the sputtering parameters, namely the chamber pressure, the argon gas flow rate, and the magnetron power. The chamber pressure is brought to on the order of 10^{-6} Torr level before the deposition process. The results show that while the GST deposition rate does not show a clear trend for varying Ar flow rate, it shows decreasing and increasing trends for varying the chamber pressure and the magnetron power, respectively (Figure 2). The deposition rate is characterized by measuring the GST film thicknesses through imaging the cross-sections of the samples under a scanning electron microscope (SEM) (Figure 3a).

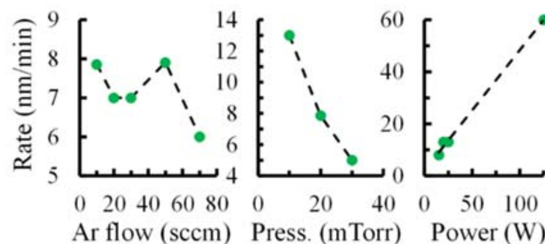

Figure 2. GST deposition rate as a function of the Ar flow, the chamber pressure and the magnetron power. The following settings are used unless it is varied for the study: 10 sccm Ar flow, 20 mTorr pressure, 20 W power.

The surfaces of the deposited GST films are then inspected using SEM. It has been noticed that the films form cracks for increasing Ar flow rate (Figure 3c-d). A similar trend is observed for increasing chamber pressure and magnetron power. Since the cracks are expected to adversely affect the in-plane electrical

conduction, low levels of sputtering parameters, e.g., 10 sccm Ar flow rate, are preferred to achieve crack-free films. For the lowest chamber pressure used for the study, however, the deposition rate is very high. Similarly, the deposition rate is linearly increasing with the magnetron power. Therefore, intermediate levels of chamber pressure (20 mTorr) and magnetron power (20 W) are preferred to keep the deposition rate around 10 nm/min to be able to control the film thickness with nanometer precision. The temperature of the substrate holder is kept at room temperature passively. Hence, a study involving the deposition temperature is not performed. On the other hand, it is worth mentioning that the cracks in the as-deposited films are observable after annealing at elevated temperatures as well. Once the film deposition parameters are optimized the devices are fabricated using single optical lithography, GST deposition, and lift-off steps. The film thicknesses are chosen to be above 100 nm for thickness characterization using cross-section SEM imaging. The films deposited for device fabrication is preferred to be thin, e.g. 40 nm, to limit the electrical current.

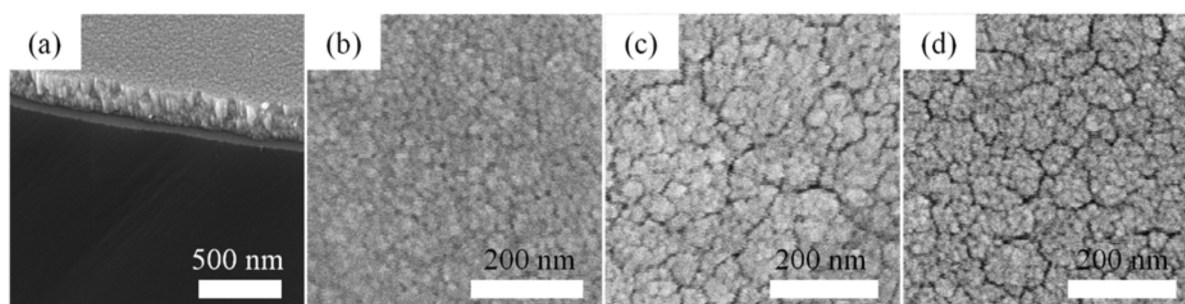

Figure 3. (a) Tilted cross-section SEM image of 180-nm-thick GST film on Si. Top-down SEM images of GST films deposited using 20 mTorr chamber pressure, 20 W magnetron power, and Ar flow rate of (b) 10 sccm, (c) 30 sccm, and (d) 70 sccm. GST film thicknesses for (b)-(d) are ~ 100 nm.

An optical mask is prepared with two-terminal and four-terminal electrical devices. The minimum dimensions of the devices are observed to be submicron on the optical mask. The patterns are then transferred using a mask aligner to AZ 5214E photoresists spin-coated on SiO_2/Si substrates. The devices are formed by GST film deposition followed by a thin HfO_2 film deposition within the same sputtering chamber and subsequent immersion of the samples in acetone for liftoff. HfO_2 is compatible with GST and its sputtering target is readily available, hence it is chosen as the capping layer. The thin HfO_2 film on the GST layer aims to protect the GST film from oxidation and disintegration during the phase-transition. SiO_2 and Si_3N_4 are also used in the literature for the same purpose [10,13]. The fabrication process demonstrated here offers a simple solution to achieve submicron PCM devices. For comparison, the fabrication process to fabricate nanoscale lateral PCM devices developed by Dirisaglik *et al.* [7] is summarized here: The SiO_2 layer is dry etched followed by a photolithography process, TiN (or W) contacts are then deposited and planarized using chemical mechanical polishing. The GST film and a capping Si_3N_4 layer are deposited and patterned using another photolithography and dry etch steps. Finally, the devices are capped with a thin Si_3N_4 layer. The simple fabrication process proposed in this study is achieved by omitting metal contacts, hence the elimination of further deposition, patterning, and etching steps. Although the devices cannot be interconnected without metal contacts, preventing fabrication of integrated circuits, such isolated devices are suitable for fundamental studies, such as characterization of crystallization dynamics and limiting the amorphization current.

3. RESISTIVITY MEASUREMENTS

The initial electrical characterization of GST films is performed using unpatterned films on SiO_2/Si substrates using the collinear 4-point-probe (4pp) technique (Figure 4). The collinear 4pp technique uses 4 aligned probes in contact with the sample. The two probes in the middle measure the voltage difference, while the outer two probes force an electric current through the sample. Since no current flows into the probes in the middle, the effects of any contact resistances associated with these probes

are eliminated; thus, the 4pp method provides the voltage drop across the sample. If the interprobe spacing (s) is constant, the sheet resistance of the film can be calculated as [14]:

$$R_{Sheet} = \frac{\pi}{\ln(2)}\frac{\Delta V}{I} \qquad (1)$$

The sheet resistance expression is valid when the film thickness (t) is much smaller than the interprobe spacing (s), the size of the sample is at least 40 times larger than s, and the distance between any of the probes and the closest nonconducting boundary is at least 4 times larger than s. If, any of these conditions are violated, further correction factors must be accounted for. Alternatively, the Van der Pauw method could be employed for the film measurements [15]. In contrast to the collinear method, the Van der Pauw method can be applied to any sample regardless of its shape or dimensions, however the Van der Pauw method requires two consecutive 4pp measurements to extract the sheet resistance [16]. The resistivity of the film can be calculated as $R_{Sheet} \times t$ after characterizing the film thickness (t). A collinear 4pp system with an interprobe spacing of 4 mm is designed and produced using 3D printing and tungsten needles as shown in Figure 4. The tungsten probes are connected to a Keithley 2400 sourcemeter capable of performing 4pp measurements.

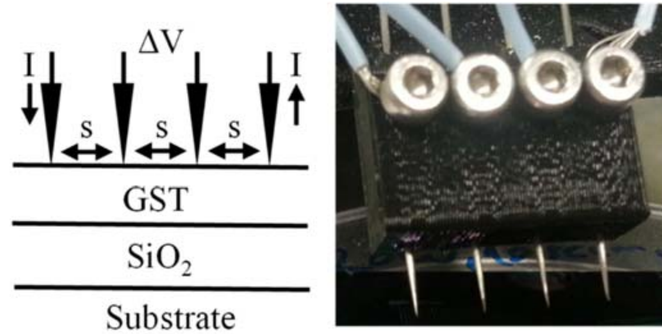

Figure 4. Illustration of the collinear 4-point-probe measurement procedure on a sample and photograph of the 4-point probe system.

The 4pp setup can measure resistance values up to 200 MΩ that is a limit imposed by the sourcemeter. Therefore, the as-deposited amorphous GST films, which are expected to have sheet resistance levels on the order of GΩ, cannot be characterized with this setup. The resistivity of the films can be measured after crystallization of the GST layer. Figure 5a shows ΔV-I curve for 140-nm thick crystalline GST film coated with 90 nm SiO_2. The GST film is crystallized within the PECVD chamber at 250 °C prior to the SiO_2 coating. ΔV and I measurements are repeated for various current levels to test the linearity of the relation between ΔV and I. The ΔV/I ratio is then found as 8.5 kΩ. The sheet resistance and the resistivity of the crystalline GST film are calculated as 38.5 kΩ and 0.53 Ω.cm, respectively.

The resistivity of as-deposited amorphous films is measured using 260-µm-long GST wires with widths varying from 3.1 µm to 29 µm (Figure 5b). Although these devices are fabricated as 4-terminal devices, 4pp measurements cannot be performed due to lack of micromanipulators. Hence, 2-terminal resistance values of devices with varying widths are measured. Owing to the uniform cross-sections of the wires, the total resistance can be modelled as:

$$R_{wire} = R_C + \frac{\rho L}{tW} \qquad (2)$$

where R_C is the contact resistance, ρ is the resistivity, L is the wire length, t is the film thickness, and W is the wire width. Modelling the wire resistance as in Eq. (2) allows for extraction of the unknowns, namely R_C and ρ. When R_{wire} is plotted against $1/W$, the linear fit line reveals R_C as the y-intercept and $\rho L/t$ as the slope (Figure 5c). These parameters for our case are found as R_C= 4 GΩ, ρ=5.48x10^3 Ω.cm. The room temperature resistivity of as-deposited amorphous GST films is 4 orders of magnitude larger than that of crystalline GST films.

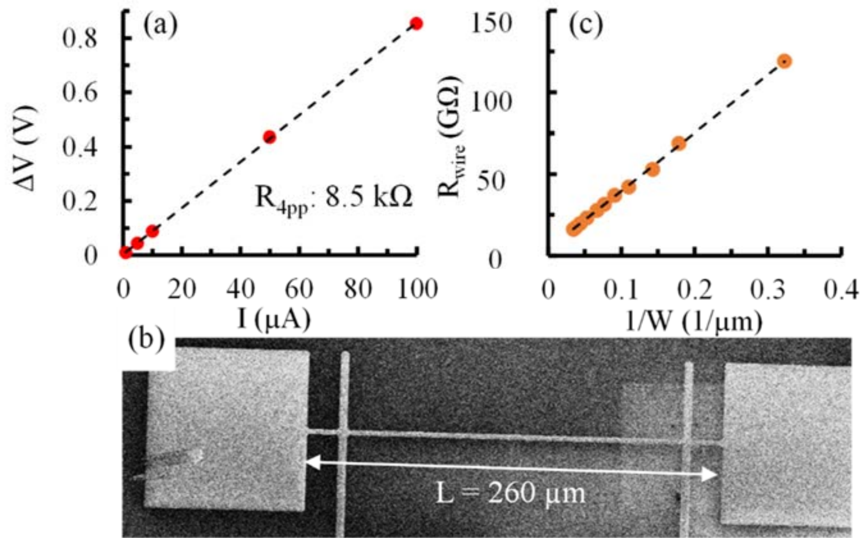

Figure 5. (a) ΔV-I characteristics for 140-nm-thick crystalline GST film measured using the 4pp setup. (b) SEM image of a long GST wire. The contact pad dimensions are 100x100 μm^2. GST film thickness is 40 nm. (c) GST wire resistance as a function of reciprocal of the wire width. Dashed lines in (a) and (b) are linear regression lines.

4. TEMPERATURE-DEPENDENT RESISTIVITY MEASUREMENTS

The change in the electrical resistivity of the GST films can be monitored by measuring the sheet resistance while changing the film temperature gradually. The 4pp setup used for measuring the room-temperature sheet resistance, however, cannot stand the high temperatures (T > 100 °C). Therefore, a large-scale 4-terminal GST structure is included in the design and fabricated together with other small-scale GST wires (Figure 6a). Similar to the collinear 4pp technique, two outer probes force current through the rectangular GST patch, while two probes in the middle monitor the voltage drop across the middle square region. The advantage of using a device with well-defined dimensions is the measured ΔV/I ratio reveals the sheet resistance regardless of the probe positions. For the film level 4pp measurements, however, the measured voltage difference is affected by the probes movements during the measurement. Fixing the probe locations is typically straightforward at a constant temperature, however it can be challenging for varying sample temperatures due to expansions/contractions of the sample. The sheet resistance in this case is the resistance of the square piece in the middle. The resistivity is calculated by multiplying R_{Sheet} by the film thickness of ~40 nm. The film temperature is measured using a k-type thermocouple in contact with the sample. Initially, the sample is placed on a hot plate and the sample temperature is increased from room temperature to 120 °C while recording both ΔV/I and the surface temperature (black dots in Figure 6b). The sheet resistance values are above the detection limit of the sourcemeter until the sample temperature reaches 100 °C. The heating is terminated when the temperature reaches 120 °C. As the sample cools down to room temperature, the amorphous film resistivity values are observed to be lower than those observed for the heating period as a result of partial crystallization. For the second heating cycle, the sample temperature is increased to 170°C during which a complete amorphous to fcc crystalline transition is observed as a sudden drop in the resistivity in a

tight temperature range (140-150°C) (red dots in Figure 6b). The change in the room temperature resistivity value is more than ~4 orders of magnitude after amorphous to crystalline phase transition. For the 3rd and the last heating cycle, the sample temperature is increased to 250 °C, during which fcc to hexagonal crystalline phase transition is observed (orange dots in Figure 6b). The room temperature resistivity for the hexagonal phase is measured as $4x10^{-3}$ Ω.cm, which is ~6 orders of magnitude smaller than the as-deposited amorphous film resistivity. Dashed curve in Figure 6 tracks the complete journey of the resistivity as the GST phase varies from amorphous to fcc crystalline to hexagonal phases with increasing temperature. Although, GST can provide 3 stable phase conditions (amorphous, fcc crystalline, hexagonal crystalline) at room temperature, only the amorphous and fcc crystalline phases are used for practical electronics and photonics applications, as the hexagonal phase can only provide small changes in the material properties compared to fcc phase and requires high energy and long durations to achieve. It is also worth noting that while the amorphous and the fcc-crystalline phases exhibit negative temperature coefficient of resistivity (TCR), the hexagonal phase exhibits slightly positive TCR. The change in the TCR behavior for the hexagonal phase is attributed to its metallic nature, whereas the amorphous and fcc-crystalline phases show semiconducting behavior [17]. The amorphous to fcc transition and fcc to hexagonal phase transition temperatures observed in this study are in agreement with the literature [1]. However, it must be noted that the phase-transition temperatures vary with the heating rate [10], the layers sandwiching the GST film, and the GST thickness [18].

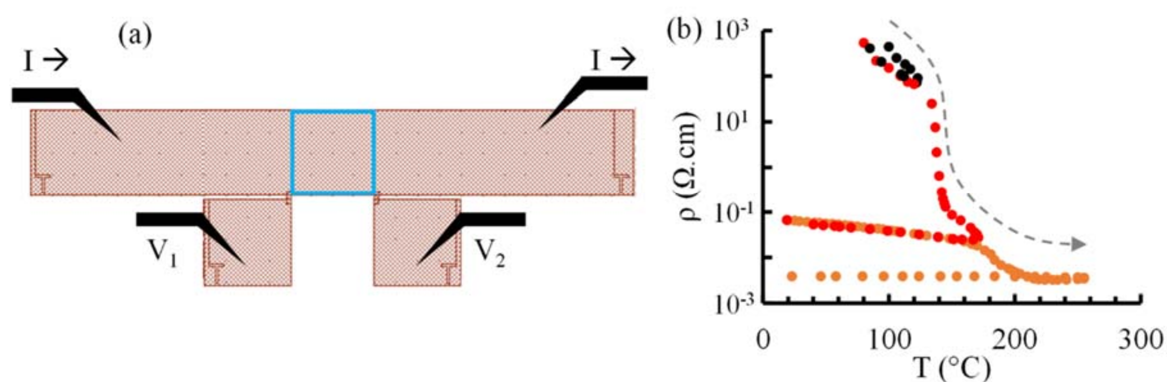

Figure 6. (a) Illustration of the 4-terminal device and the probe placements used for the temperature-dependent measurements. The resistance of the square in the middle, enclosed with a blue lines, is measured as $(V_1-V_2)/I$. The square dimensions are 2x2 cm^2. The GST film is covered with a thin HfO_2 layer. (b) GST film resistivity as a function of the film temperature.

5. CURRENT-VOLTAGE MEASUREMENTS

For the final part of the study, current-voltage (I-V) characteristics of the 2-terminal GST wires are measured using a Keithley semiconductor parameter analyzer. The wire widths range from 0.5 µm to 3 µm. The wires are formed as narrow necks merging two contact pads to achieve submicron critical dimensions (Figure 7a). The I-V characteristics of the wires in crystalline phase show a linear trend for low voltage levels (< 5 V) as what is expected from an ideal resistor (Figure 7b). For increasing voltage level, however, the I-V behavior show a superliner trend owing to the heating effects. When the current reaches a critical level, the narrow region melts and amorphizes. The amorphization is verified by a sudden drop in the current level by a factor of ~1000. The amorphization current, hence the power, scales with the GST wire dimensions (Figure 7c). Therefore, further reduction in the amorphization current may require higher resolution lithography techniques, such as electron beam lithography.

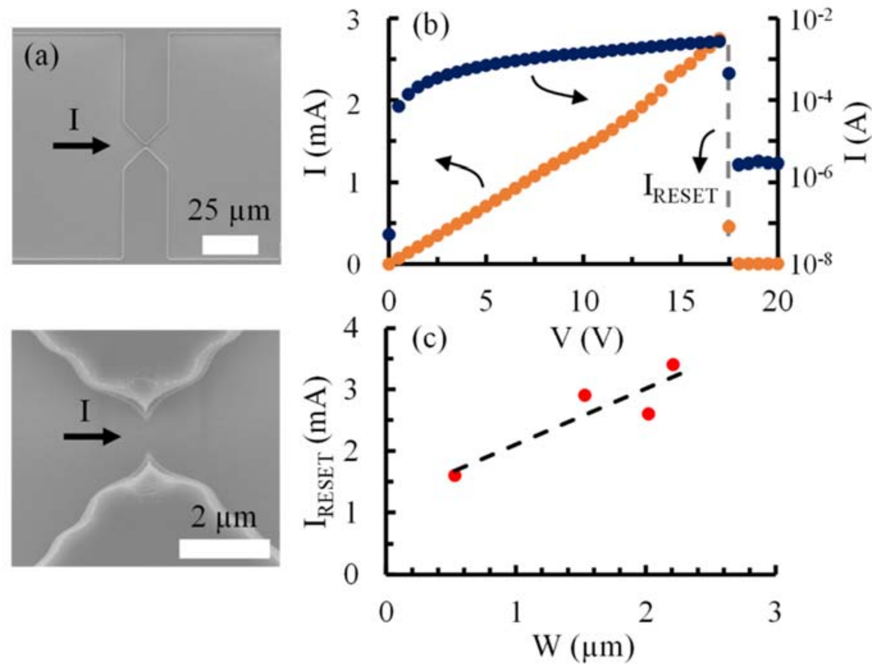

Figure 7. (a) SEM images of a GST wire and contact pads prior to liftoff at the top and the close-up of the wire region at the bottom. The wire width is 0.7 µm. The film thickness is 40 nm. (b) Current-voltage characteristics of a GST wire with W=2.2 µm in linear and semi-logarithmic scales. Vertical dashed line marks the amorphization (RESET) event. (c) Amorphization current as a function of wire width for 4 wires. The dashed line show the increasing trend with width.

6. CONCLUSIONS

In summary, phase-changing GST films are deposited on electrically insulating substrates using sputtering method. The sputtering parameters, namely the Ar gas flow, chamber pressure and magnetron power, are studied to achieve crack-free films, and moderate deposition rates. The deposited films are characterized using SEM by imaging surfaces and cross-sections. 2-terminal and 4-terminal GST devices with various geometries and dimensions are fabricated using photolithography, GST deposition, and liftoff. Room temperature resistivity values of the films in both amorphous and crystalline phases are characterized using a custom built 4-point probe setup and as well as GST wires with well-defined geometries. The room-temperature resistivity values are found as 5 kΩ.cm for amorphous phase, 0.5 Ω.cm for fcc crystalline phase, 4 mΩ.cm for hexagonal phase The change in the film resistivity as a function of the sample temperature is monitored on a hot plate using a larger scale 4-terminal GST structure. The results show amorphous to fcc crystalline and to hexagonal phase as sudden drops in the resistivity at ~150 °C and ~200 °C, respectively, for increasing temperature. As the final study, microscale GST wires are amorphized by sweeping electrical current. The amorphization current is observed to scale with the wire width, creating a current density of $\sim 6\times10^{10}$ A/m^2. The study offers fewer fabrication steps using standard semiconductor processing techniques to achieve phase-change memory devices.

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