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Impedance Response and Phase Angle Determination of Metal-Semiconductor Structure with N-Doped Diamond Like Carbon Interlayer

Nuray URGUN[1*] Aylar FEIZOLLAHI VAHID[2] Jaafar Abdulkareem Mustafa ALSMAEL[3] Barış AVAR[4] Serhat Orkun TAN[5]

[1] *Karabük University, Faculty of Engineering, Department of Mechatronics Engineering, Karabük, Türkiye*
[2] *Zonguldak Bülent Ecevit University, Department of Nanotechnology Engineering, Zonguldak, Türkiye*
[3] *Basrah University, Oil and Gas Engineering, Faculty of Oil and Gas, Basrah, Iraq*
[4] *Zonguldak Bülent Ecevit University, Department of Metallurgy and Material Engineering Faculty of Science, Zonguldak, Türkiye*
[5] *Karabük University, Faculty of Technology, Department of Electrical Engineering, Karabük, Türkiye*

Keywords

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Abstract

With their superior properties over p-n barriers, Schottky Barrier Diodes have a wide usage area, especially as a test tool to produce better-performance devices. The main performance parameter of these devices is measured by their conduction, which can develop with an interlayer addition through the sandwich design. Regarding the DLC, which also has outstanding specifications under thermal, chemical, and physical conditions, is a good candidate for interlayer tailoring, specifically when used with doping atoms. Thus, this study investigates the impedance response of the fabricated device with an N-doped DLC interlayer by employing the electrochemical technique as a combination of electrolysis, RF magnetron sputtering, and thermal evaporation. The measurements were conducted for broad scales of voltage and frequency corresponding between (-3V) and (+4V) and 1kHz and 1MHz, respectively. According to the impedance analysis, complex impedance decreases by rising bias and frequency, from 1.8 MΩ to 2 k Ω at 1MHZ due to the additional insulating layer. At the same time, the phase angle indicates the quality of the dielectric layer with an average of 81.36 ° for the sample logarithmic frequency values with an almost constant-like trend in the inversion stage. In comparison, it reduces to an average of 30.25 ° after the depletion stage by showing the rising conductivity. Moreover, it has some unexpected rising values at the strong accumulation stage, possibly due to the deposited thin film's unique structure. The supported results by phase angle changes, showing frequency-adjustable working conditions, may offer that selective electrical conduction can be tuned.

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Author ID (ORCID Number)

0000-0001-6574-4287 Nuray URGUN
0000-0003-3157-2725 Aylar FEIZOLLAHI VAHID
0000-0002-2426-9421 Jaafar Abdulkareem Mustafa ALSMAEL
0000-0002-6234-5448 Barış AVAR
0000-0001-6184-5099 Serhat Orkun TAN

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1. INTRODUCTION

In electronics technology, Schottky barrier diodes (SBDs) or metal-semiconductor (MS) structures, which are distinguished from other diodes by their fast-switching ability, due to the being unipolar devices, at high frequencies and low-level forward biasing, still have an important place in the scientific community with many different applications (Northrop & Rhoderick, 1978; Sharma, 1984; Soylu & Yakuphanoglu, 2011; Hwang et al., 2013; Tan, 2017). SBDs also have speed adjustments among themselves besides being better performance devices over P-N junctions. In one related work, researchers compared the tri-anode and planar SBDs and found that the tri-anode SBD's switching mechanism was faster than the planar one (Nela et al., 2019). Moreover, SBD applications can be extended from the Schottky structures in scanning electronic microscopes (SEM) to the high-power frequency multiplier designs (Ersöz et al., 2018; Konstantinou et al., 2021).

*Corresponding Author, e-mail: nuray1erkutlu@gmail.com

These applications usually arise by choosing different interfacial layers between metal and semiconductors. Metal-insulator-semiconductor (MIS), metal-ferroelectric-semiconductor (MFS), and metal-polymer-semiconductor (MPS) structures are fabricated by using insulating, ferroelectric, and organic in the interfacial layer, respectively. The characterization of these structures under many external factors such as temperature, irradiation, and illumination intensity has been investigated in many studies (Singh et al., 1990; Sharma et al., 2007; Tataroğlu & Altındal, 2009; Tecimer et al., 2013; Lee et al., 2016; Tan et al., 2016). As a result of these investigations, it was emphasized that the use of the mid-layer has a positive efficacy on the characteristics of the structure by regulating the charge transitions at the interface and improving the device's performance (Card & Rhoderick, 1971; Goetzberger et al., 1976; Lin et al., 2014; Maril et al., 2018). Diamond-like carbon (DLC) films, which have the necessary interlayer properties such as thermal stability, adhesion on the substrate and wear resistance, can be preferred as the interlayer material that can be used to obtain MIS structures with higher barrier heights (Basman et al., 2015; Bootkul et al., 2014).

DLC films can be used in MIS structures in electronic technology as well as in solar cells, microelectronic-mechanical systems and various heterostructures. While factors such as H content, sp^2 and sp^3 bond content and lattice disorder reveal the properties of these films, it is known that sp^2 bonds are effective on electronic act and optical properties, while sp^3 bonds control mechanical and tribological properties (Evtukh et al., 2003; Hajimazdarani et al., 2021; Cetinkaya et al., 2023). To effectively increase the graphitization of carbon films, doping DLC films with dopants such as Si, N, Cu, Ti, and S is beneficial for conduction states (Evtukh et al., 2003; Basman & Varol, 2019; Feizollahi Vahid et al., 2023). DLC films, which are also delineated as amorphous forms of carbon materials, take place in many applications such as magnetic storage disks, wear-resistant films, biomedical coatings, and optical coatings (Basman et al., 2015; Zeng et al., 2014; Zhang et al., 2020). In a study in which DLC layer was electrochemically grown and used as an interlayer in Al/(DLC)/p-Si/Au MIS type structure, the electrical parameters of the structure were calculated, and it was concluded that the electrodeposited DLC interlayer can be used to reduce surface states or dislocations instead of the commonly used oxide/insulator interlayer (Şafak Asar et al., 2023). In another study, the electrical parameters of the MS structure using Ti doped DLC interlayer were investigated in the 1kHz-4kHz range by impedance-spectroscopy method. SEM, EDX and XPS methods were used for the structural characterization of the interlayer grown by electrochemical deposition method and the important effect of interfacial states and their relaxation times in the depletion region at low frequencies and series resistance in the accumulation region at high frequencies was emphasized (Berkün et al., 2023).

In the present study, the impedance and phase angle of a metal-semiconductor structure (Al/N: DLC/p-Si/Au) with an N-doped DLC interfacial layer are calculated for a wide frequency range. The impedance response under varying electric field ($\vec{E}$) was studied between 1MHz and 1kHz to detail the structure's operating characteristics. The impedance data obtained were used to observe the relative impedance variation depending on the conduction states of the structure. It is also important to determine the phase angle to follow the evolution and trend of the conduction mechanisms in terms of low capacitive or inductive effects. From this point of view, the Al/N: DLC/p-Si/Au structure, the frequency dependent impedance and phase angle data are analyzed in detail. The reducing trend for the impedance was observed by rising bias and frequency, which is a proof for rising conduction performance. Besides, the high values of the impedance parameter at the reverse polarization region, which should be directly related to the contribution of the N-doped DLC layer’s dielectric behavior, showed that the studied structure has the capability to store more charge in it when it is not in the conductive phase.

2. MATERIAL AND METHOD

Al/N:DLC/p-Si/Au MIS structure, 100 mL of methanol (CH3OH Sigma Aldrich) (N 99.5%) and 200 mg of urea were stirred with a magnetic stirrer for 15 minutes. A boron-doped p-type Si substrate with <100> surface alignment and ≈300 μm thickness was used as the negative electrode and a graphite plate was placed at 4 mm intervals as the counter electrode. N: DLC thin film layer was deposited on the p-Si substrate by electrolysis. Then, Au back contact was formed by RF magnetron sputtering at 550 V and annealed at 550 °C for achieving better ohmic connection for the device. As the last step, high purity Al rectifier contacts were formed by thermal evaporation to obtain Al/N:DLC/p-Si/Au MIS structure. So, the fabrication process was completed by electrochemical deposition technique by combination of several methods. The measurements were conducted

for a voltage range of (-3V) to (+4V) and a frequency range of 1kHz to 1MHz via impedance spectroscopy method by HP 4192A LF impedance analyzer. The impedance and phase angle calculations were made from the computer processed analyzer outputs of C(ω)-V; G(ω)-V, and C(ω)-f(Hz) ; G(ω)- f(Hz) measurements.

Figure 1, illustrates the variable device capacitance behavior according to the different phases of DLC film as an interlayer specifically in depletion region.

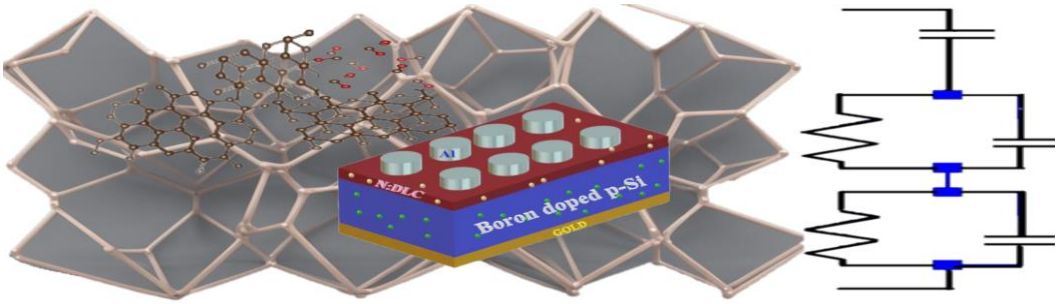

Figure 1. *Illustration of fabricated structure with the DLC dependency effects on capacitance shaping*

3. RESULTS AND DISCUSSION

3.1. Impedance Response

Impedance response of a device gives the detailed working characteristics of the structure under an altering electric field. In this section, we provide a large scale of impedance response of our structure by both (*Z'*, *Z''*, *Z)-V* and *Z''-Z* plots in a wide frequency scale to investigate the behavior change by varying parameters. *Z''-Z'* plots are quite a useful tool to observe the relative impedance change in a structure due to conduction changes. The impedance calculations were done with Equation 1 as follows where *Z** is the complex impedance, and *Z', Z''* are real and imaginary components of it, respectively. All other relations and constants used for this study are given in Table 1.

$$Z^*(\omega) = Z'(\omega) - jZ''(\omega) = \frac{1}{j\omega C_0 \varepsilon^*} = \frac{\varepsilon''}{2\pi f C_0(\varepsilon'^2 + \varepsilon''^2)} - j\frac{\varepsilon'}{2\pi f C_0(\varepsilon'^2 + \varepsilon''^2)} \quad (1)$$

Table 1. *The table gives the employed relations and constants*

Parameter	Symbol	Formula & Value
Complex Dielectric	ε*(ω)	$\varepsilon^*(\omega) = \varepsilon'(\omega) - j \cdot \varepsilon''(\omega)$
Dielectric constant	ε'(ω)	$\varepsilon'(\omega) = \left(\frac{C_m}{C_o}\right)$
Dielectric loss	ε"(ω)	$\varepsilon''(\omega) = \left(\frac{G_m}{\omega \cdot C_o}\right)$
Permittivity of Free Space	ε_o	Constant 8.854×10^{-12} F/m
Vacuum Capacitance	C_o	$C_o = \frac{\varepsilon_o \cdot A}{d_i}$ = 6,95 pF
Measured Capacitance	C_m	Measured value, Variable for 0.55V between 3.77nF for 1khz, and 0.18nF for 1MHz
Measured Conductance	G_m	Measured value
angular frequency	ω	ω=2πf
Interfacial Layer Width	d_i	Constant, $d_i = 10^{-6}$ m
Schottky Contact Area	A	$A = \pi r^2$ = 0.00785 cm²

The given plots in Figure 2 show the impedance variations due to the real and imaginary components of complex impedance (Z^*) value and the magnitude of it $|Z|$ in A, B, and C, respectively. In Figure 2c, impedance decreases with increasing bias voltage, and it changes from 2 MΩ to few kΩ, and then to few hundred Ω and

after that it gets closer to zero at the highest bias voltage. The transition between conduction regions in terms of impedance is also clear in the inset of the plot. The random peaks of real impedance at negative polarization stage are easily seen in Figure 2a, and they are mostly effective at the lowest frequencies. It also exhibits the depletion peaks at around 0 V, followed by smaller secondary peaks around 1 V. The similarity between *Z″*-V and *Z*-V plots implies that *Z″* is more effective in impedance behavior until the conduction. To analyze the physics behind the behavior of the complex impedance response of the interlayered device, the entire conduction path, from the strong inversion to the strong accumulation phases, is offered in Figure 3, and focused on accumulation region in Figure 3g, h, i.

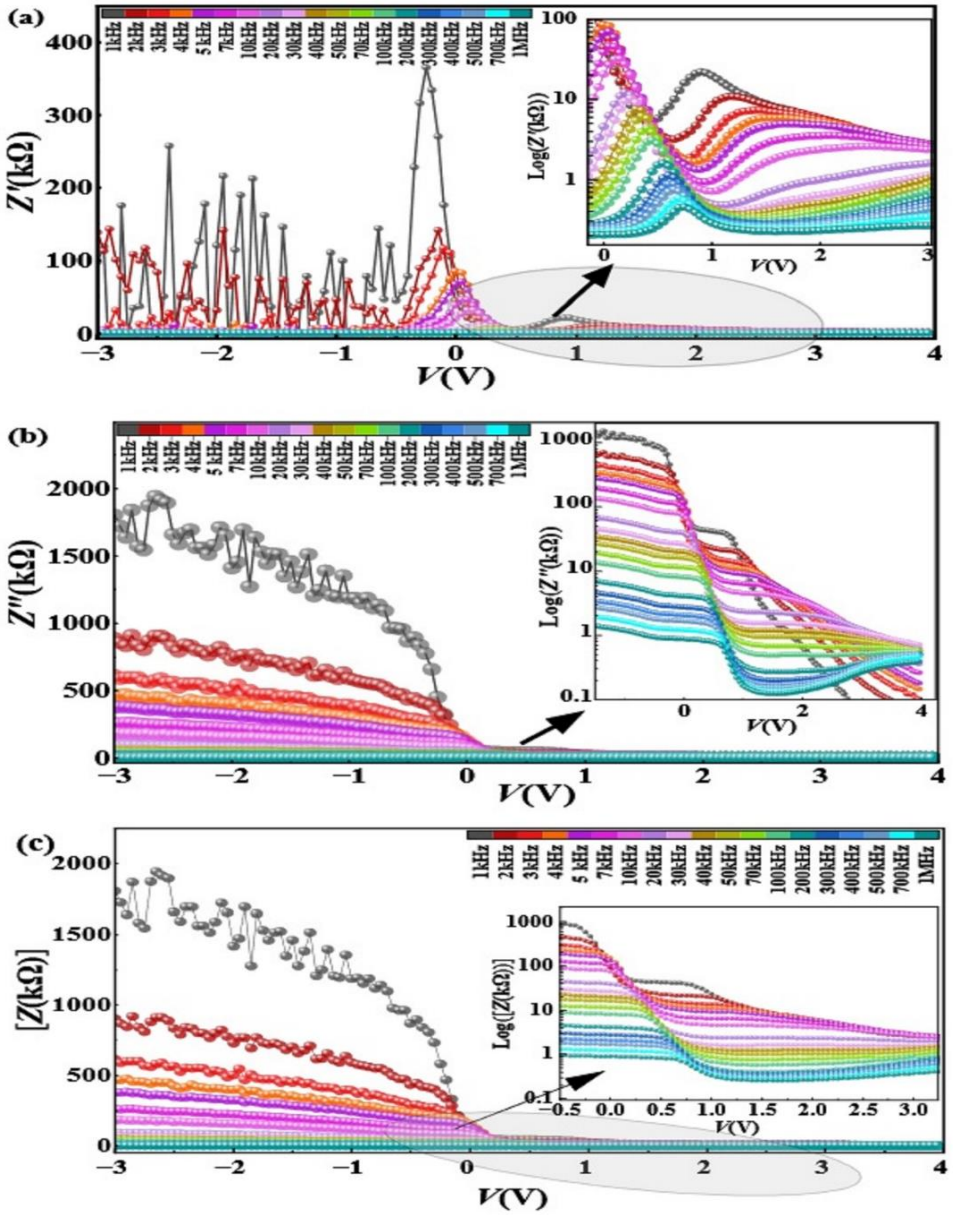

Figure 2. *For (-3) to (+4) V between 1 kHz-1 MHz : a) Z'-V, b) Z''-V, c) Z-V*

One can see that in Figure 3a, there is almost a steep trend in *Z″* vs *Z′* plot for each of the low frequencies. Thus, in Figure 3a, the structure shows strongly capacitive behavior at low frequencies at a few MΩ scale; while the frequency rises from low to medium, it becomes a mix-up of predominantly capacitive and slightly parasitic behavior in Figure 3b at several tens of kΩs.

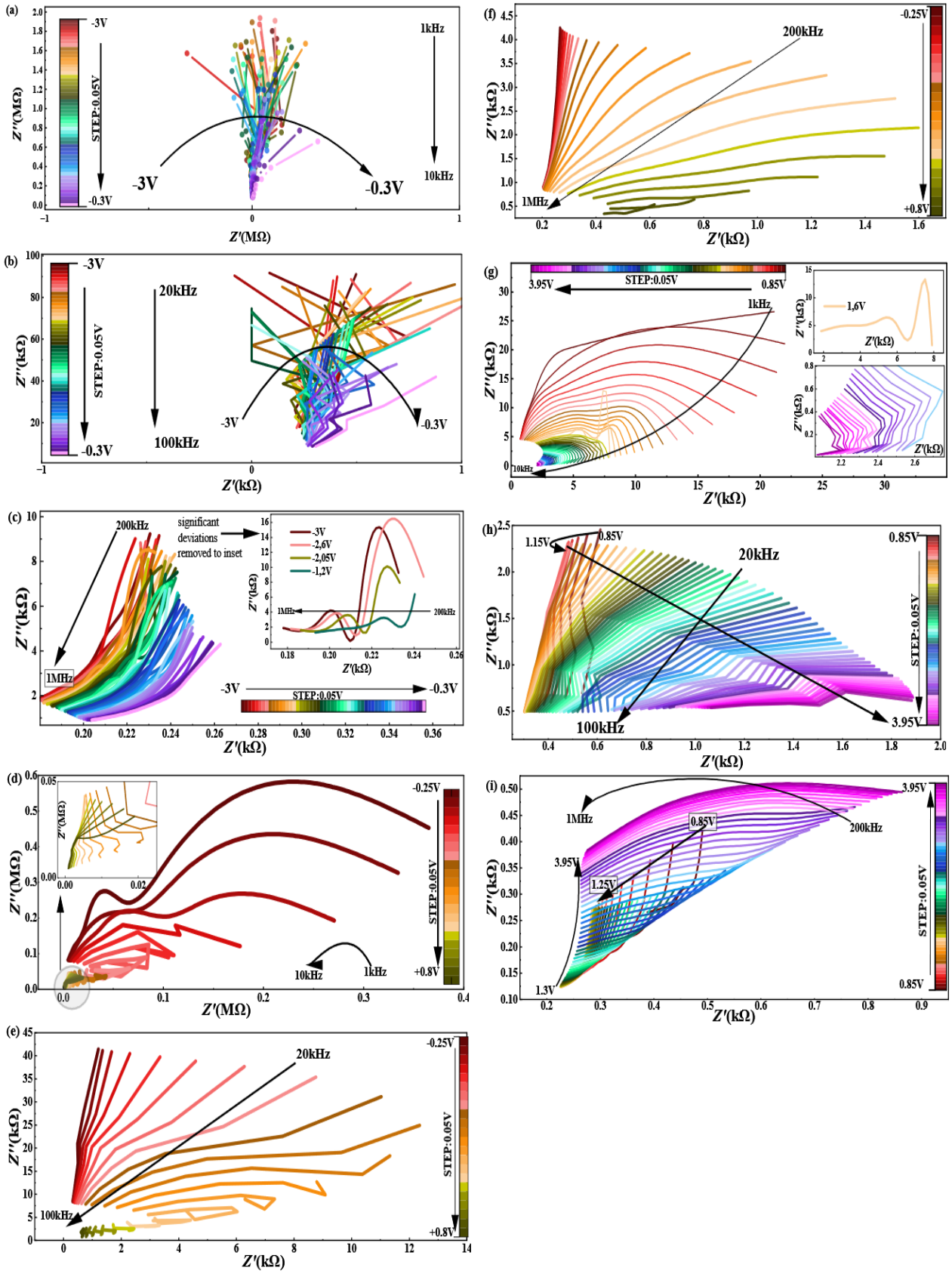

Figure 3. *Z'' vs Z' at:* ***a-c)*** *Inversion (-3V to -0.3V);* ***d-f)*** *Depletion (-0.25 to 0.8V);* ***g-i)*** *Accumulation (0.8 to 3.95V). Frequency Ranges:* ***a, d, g)*** *1-10 kHz; b, e, h) 20-100 kHz;* ***c, f, i)*** *200 kHz-1 MHz*

Lastly, in Figure 3c, Z shows negligibly resistive-like and parasitic-like behavior besides highly capacitive behavior by rising bias for a high-frequency scale at a few kΩ. So, it is a 3-step process at the inversion stage as strong, medium, and weak levels. Overall, Z'' is found to be always greater than Z' in all those inversion stages. These step transitions in the inversion stage are also observable in depletion and accumulation stages in the following plots. When Figure 3d, e and f are compared, the Z'' values decrease almost by 5 orders of its previous value each time, while corresponding Z' values lessen faster. In accumulation stage, impedance has to show small values for device performance, which is observed in studied structure as in Figure 3g, h, i. The first plot is demonstrating right after the depletion region completely loses its effectiveness, so the capacitive impedance still has a value of kΩ around 30 to 2 at low frequencies in Figure 3g. One can see the flattening curves of plots become more apparent since the capacitive effects are lessening and diminishing, instead the total conduction is rising so the real part of impedance is relatively rising compared to imaginer one's change with an overall decreasing in plots from around 2.5 kΩ to 0,5 kΩ in Figure 3h, and from around 0.5 kΩ to around 50 Ω in Figure 3i.

In the low frequency range both Z'' and Z' values are decreasing with increasing frequency and bias. Moreover, at medium frequency range Z" remains decreasing while Z' increases with rising bias and frequency which is a proof for the Rs effect. And at high frequencies, both Z'' and Z' decrease with rising frequency while Z'' increases when Z' stays almost constant with rising bias. These behaviors of conduction can be explained as Rs is effective at medium frequencies and medium to high voltages as in Figure 3h while at high frequencies it almost disappears as in Figure 3i. And employing impedance response in plots, it is possible to define a basic equivalent circuit corresponding to these behaviors of fabricated MIS device.

In Figure 4a, and 4b both Z' and Z'' are rising with lessening frequency and voltage. And after the obvious peak, the impedance plot exhibits opposite behavior. And these kinds of interchanges in the plot mean equivalent circuit should have capacitive reactance and inductive or resistive components. Moreover, the linear like trend at the very first region of this plot where Z'' gets high values when Z' gets ten orders lower values than Z'', meaning that the structure is strongly capacitive at this scale and does not allow any current to flow except metal plates' surface leakage currents. As a basic MOS capacitor equivalent, according to the change at the C-V and G/ω-V values, a study group used an example circuit in their work which is generally appropriate for our structure, as well (Tan et al., 2022). In the structure studied, there is a very unique interface with aligned and randomly located clusters, which has the potential to significantly affect electrical conduction by changing the impedance of the structure through its components. Thus, in addition to operating conditions in different conduction regimes, this situation can also change the impedance by contributing to changes in effective capacitance and conductance values, resulting in deviations from the general trend of the plots. Especially when looking at Figures 2a, 3c, 3g and 4a, these deviations can easily be seen as markedly low voltage and frequency responses, respectively. Therefore, in comparison to a simple MOS capacitor, our structure should be slightly different. In several studies, researchers have mentioned how the structure responds differently to the input signal at high and low frequencies (Rodrigues, 2008; Das et al., 2018). In another work, Kadri et al. (2017) related the low frequency response with grain boundaries while relating the high frequency response with grains, employing by a parameter in their Nyquist plots of Z. Besides the results of these studies, counting on the depletion layer effect on effective capacitance at high and low frequency scales is quite reasonable for our structure, too (Rodrigues, 2008).

Thus, considering the structural changes as a matrix, the deviations from well-known laws like Ohm's law can be explained when changes are counted on both between different dielectric layers as vertical and between more than one phase compounds as horizontal. Since the distribution of clusters, surface and deeper state traps are dramatically important parameters on conduction, they can be used as input variables to adjust the output impedance/capacitance or conductance in a simple equivalent circuit estimation corresponding to our structure. There is one major semicircle after a linear-like region and before a medium-sized semi-circle followed by a third and smallest semicircle. So, the 3 points of tangency at these 3 semicircles show that at the same frequency there are 2 different responses due to the 2 same directional semicircles possibly due to the existence of 2 different structural components in Figure 4a. In other saying the reason for the existence of the materials' relaxation behavior under the ($\vec{E}$), which shows up in different scales of the impedance when frequency stays still is a result of the different material composition existence besides the voltage dependent response of N_{SS}. Upon careful observation of all the plots, it is evident that this structure exhibits an asymmetrical charge

distribution behavior reminiscent of the matrix as illustrated in Figure 5a. According to these descriptions for our model it should be a little leaky capacitor at the beginning when also considering the phase angle in Figure 4c, and then it should be a combination of capacitor and resistance or inductor since there is an interchange in charge storage and release this energy as current flow. And the following semi-circle should have the same components with lower values. So, our probable structure is as in Figure 5b (Rodrigues, 2008; Das et al., 2018).

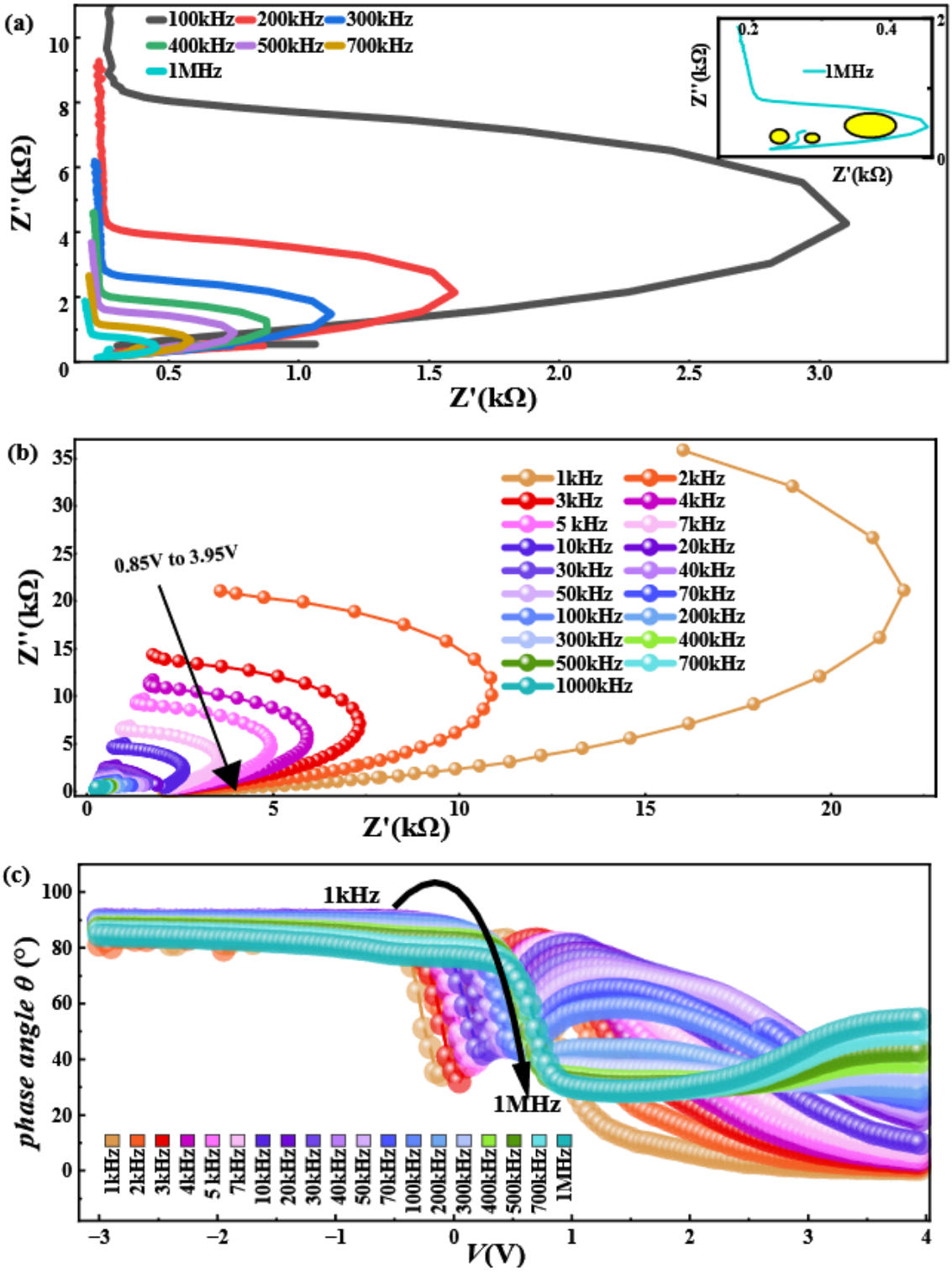

Figure 4. a) *Z'' vs Z' for -3 to 3.95 V at several frequencies,* ***b)*** *Z'' vs Z' for 1 kHz -1 MHz for several biases,* ***c)*** *Voltage dependency of Phase Angle for 1 kHz -1 MHz*

3.2. Phase Angle

Phase angel is another tool to observe conduction mechanisms change and trend in terms of under capacitive or inductive effects. It is calculated as follows in Equation 2.

$$\theta = tan^{-1}\left(\frac{Z''}{Z'}\right) \quad (2)$$

Phase angle ($\theta°$) in Figure 4c, has values around almost 90 degrees in reverse polarization which shows the combination of N: DLC and p-Si is dramatically capacitive in this region since the capacitive current follows the resistive current almost 90 degrees lagging. Thus, it is evidence for the added interlayer is serving as a good dielectric barrier in inversion region which is desired to be. After inversion region, phase angle's values exhibit mixed behaviors by decreasing halfway, and increasing again in depletion region, and then flattening in accumulation region. The trend in depletion stage shows that effective current type changes in time by mostly applied biases, besides frequency which also approves Figure 2a. As it can be seen after around 1 V, the current losses its charge storage function gradually and the distinguishing features of conduction mechanisms components lessen by decreasing phase difference.

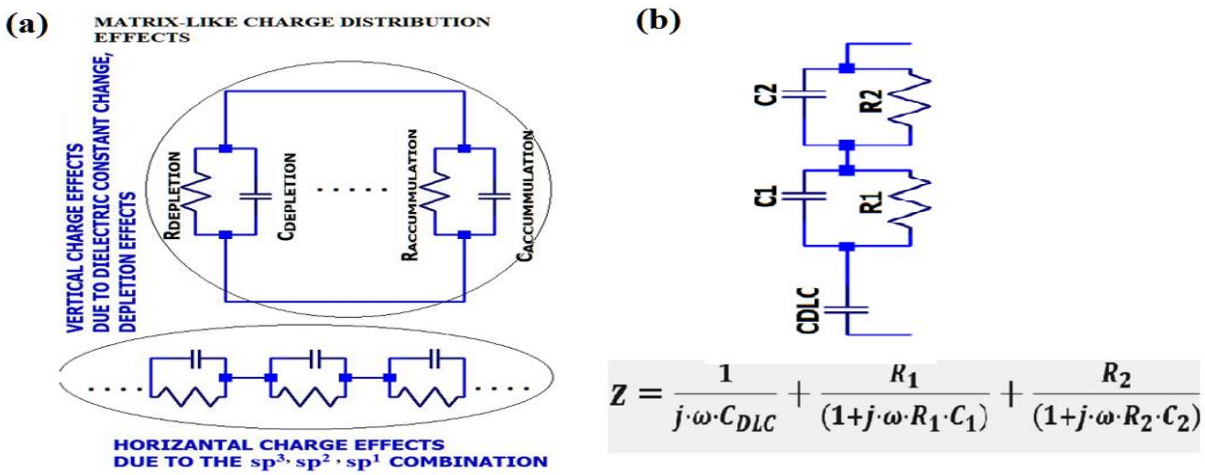

Figure 5. a) *Matrix approach of interfacial states between more than one structural component,* ***b)*** *Equivalent circuit of fabricated structure according to altering N-DLC, depletion effects and surface parameters with MOS capacitor approach*

To show how the device parameters change altogether over frequency and voltage, Table 2 is given below for logarithmic steps of frequency at few voltage points from the expected non-conductive stage to the conductive stage. When comparing any value of the samples with the corresponding value at the same, previous, and next voltages and frequencies, if the general behavior of the structure, as aforementioned in the plots' explanations above, stays still but shows only slight deviations, they can be categorized as ignorable changes. For example, phase angle has a regular trend as high constant-like values at first in the inversion stage, then falls for the depletion stage, and after that follows another rise into transition to the accumulation stage and falls again due to the Rs and complete discharging process of capacitive charges. So, a rise from 86.89 ° (at -3 V and 1 kHz) to 89.89 ° (at -3 V and 10 kHz) shows the components of Z* become 3° distant from each other, and this can be a slight deviation from the regular trend due to the surface charges' ignorable capacitive effects at low frequency. However, the change from 30.38°at (2 V and 1 MHz) to 44.98° (at 3 V and 1 MHz) shows a notable deviation. Since the real and imaginary parts of the impedance at 3V and 1 MHz are identical as 0.27kΩ and their phase angle is almost 45°, they can be interpreted as somehow in resonance, but when considered the real part of Z*, which contributes as RS effect and should be responsible for the maximum power transfer, there are lower values for Z' than 0.27 k Ω as 0.23 k Ω for the same frequency at 2V. This change seems ignorable, but when counting on the regular falling trend for Z*, this rise can be sourced from rising bias-sensitive material composition, which can be helpful for tunable parameters. Similarly, at 3.95V, the phase angle has another unexpected rise.

Table 2. *Device parameter changes comparation according to applied bias and frequency*

BIAS (V)	Frequency f (kHz)	REAL IMPEDANCE Z' (kΩ)	IMAGINARY IMPEDANCE Z'' (kΩ)	COMPLEX IMPEDANCE Z^* (kΩ)	PHASE ANGLE θ (°)
- 3V	1	97.86	1803.60	1806.25	86.89
	10	-0.33	181.51	181.51	89.89
	100	0.23	18.23	18.23	89.27
	1000	0.18	1.88	1.88	84.58
-2V	1	120.31	1411.03	1416.15	85.13
	10	1.43	154.53	154.54	89.47
	100	0.26	15.41	15.41	89.03
	1000	0.19	1.58	1.59	83.31
-1V	1	28.20	1187.27	1187.61	88.64
	10	0.94	116.02	116.02	89.53
	100	0.26	11.68	11.68	88.73
	1000	0.19	1.19	1.20	80.66
0V	1	62.93	71.30	95.10	48.57
	10	20.79	72.03	74.97	73.90
	100	0.45	8.10	8.11	86.79
	1000	0.20	0.88	0.90	76.88
1V	1	19.71	12.01	23.08	31.37
	10	0.71	4.56	4.61	81.09
	100	0.38	0.57	0.69	56.23
	1000	0.29	0.17	0.33	30.12
2V	1	5.63	0.65	5.66	6.56
	10	2.38	3.27	4.04	53.92
	100	0.35	0.50	0.61	54.47
	1000	0.23	0.14	0.27	30.38
3V	1	2.58	0.07	2.58	1.51
	10	2.37	1.07	2.60	24.22
	100	0.73	0.52	0.89	35.38
	1000	0.27	0.27	0.38	44.98
3.95V	1	2.08	0.02	2.08	0.65
	10	2.08	0.36	2.11	9.87
	100	1.06	0.54	1.19	26.76
	1000	0.28	0.38	0.47	54.33

4. CONCLUSION

In the present study, the impedance and phase angle of a metal-interlayer-semiconductor structure (Al/(N: DLC)/p-Si/Au) have been analyzed both in the wide frequency range of 1kHz-1MHz and voltage range of -3V – (+4V) at room temperature to get more information on the relaxation phoneme depend on frequency and voltage. The (N: DLC) thin interfacial layer was grown between Al and p-Si by using electrochemical deposition technique. The analysis of impedance and phase angle of the Al/(N: DLC)/p-Si/Au (MIS) structure shows that the used (N: DLC) interfacial layer leads to an important increase in device performance when compared to metal-semiconductor (MS) structure with an oxide/insulator layer. The phase angle change from 86.89° to 0.65° even at the lowest frequency by rising bias effect, is one of the samples among these significant behavior changes. Also, the device showed similar decreasing behavior for higher frequency scales, too. For instance, (N: DLC) thin interfacial layer served as a high-quality dielectric interlayer in cut-off region with a sharp phase angle below the breaking voltage to prevent any possible conduction. Moreover, after this specific voltage, it showed good electrical conductivity, with some intersections related to capacitance change outcomes through the structure, which allows for a future study to adjust the device working scale for desired band-enhancing filter component designs. The frequency-dispersion of the complex impedance was analyzed using modified Cole-Cole model, and the diameter of the semi-circles in the plot decreased with increasing frequency. A plain resistance-capacitance parallel circuit diagram is enough to explain the N-doped DLC film's inner-grain and grain-boundary effect. The observed an important decrease in the impedance's imaginary part and real part with increasing well agreed with Debye's type relaxation.

AUTHOR CONTRIBUTIONS

Conceptualization and manuscript-original draft, N.U; measurements and laboratory, A.F.V; visualization, N.U.; manuscript-review and editing, N.U., J.A.M.A, and S.O.T; supervision, B.A., and S.O.T. All authors have read and legally accepted the final version of the article published in the journal.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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