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A Low-Power 30MHz,6th Order Bandpass Differential Gm-C Filter on Chip Utilizing Floating Current Source

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Abstract: This work employs a leap-frog Gm-C structure to design a sixth-order Butterworth and elliptic bandpass filter that the cutoff frequency (Fo = 30MHz). A continuous-time differential Gm-C biquad and its corresponding voltage-mode version are elucidated, utilizing F.C.S (Floating Current Source) circuits as fundamental components. The enhanced current source architecture exhibits a streamlined configuration. It incorporates a reduced number of transistors, which facilitates optimal utilization of the chip's area and introduces a streamlined approach to circuit design. The suggested filter topology lacks a crucial resistor component, vital in achieving integration functionality. The suggested filter incorporates a grounding configuration for all capacitors, thereby mitigating the detrimental impact of parasitic effects. The filter design has been effectively realized utilizing TSMC's 0.18µm CMOS process. The findings from simulations have been provided to validate the theoretical analysis.

Keywords: Continuous-Time, Gm-C Bandpass Filter, Floating Current Source (F.C.S), TSMC's 0.18µm CMOS

Öz: Bu çalışma, bir altıncı derece Butterworth ve eliptik bant geçiren filtre tasarlamak için kesim frekansı (Fo = 30MHz) olacak şekilde bir sıçrama (leap-frog) Gm-C yapısını kullanır. Sürekli zamanlı bir diferansiyel Gm-C biquad ve buna karşılık gelen voltaj modlu versiyonu, temel bileşen olarak F.C.S (Floating Current Source - Yüzen Akım Kaynağı) devrelerini kullanarak açıklanmıştır. Geliştirilmiş akım kaynağı mimarisi, basitleştirilmiş bir yapı sergiler. Bu, transistör sayısını azaltır ve çip alanının optimal kullanımını kolaylaştırarak devre tasarımına akıcı bir yaklaşım getirir. Önerilen filtre topolojisi, entegrasyon işlevini başarmada önemli olan bir direnç bileşenini içermez. Önerilen filtre, tüm kapasitörler için bir topraklama konfigürasyonu içerir, bu da parazit etkilerin olumsuz etkilerini azaltır. Filtre tasarımı, TSMC'nin 018µm CMOS süreci kullanılarak etkili bir şekilde gerçekleştirilmiştir. Simülasyonlardan elde edilen bulgular, teorik analizi doğrulamak için sunulmuştur.

Anahtar Kelimeler: Sürekli Zamanlı, Gm-C Band Geçiren Filtre, Yüzen Akım Kaynağı (F.C.S), TSMC'nin 0.18µm CMOS'u

1. Introduction

Gm-C filters have been widely utilized, from consumer products to computer peripherals, owing to their exceptional high-frequency performance and straightforward design [1-5]. With a reduced power supply voltage, the significance of this factor becomes more pronounced, particularly as the demand for portable systems continues to increase. The high-frequency operation of Gm-C filters poses challenges due to the rapid degradation of F.C.S performance [1]. The integrator serves as the primary constituent in the Gm-C filter topology, wherein it may be implemented through a transconductor component coupled with a capacitor [2]. One of the various techniques employed in the design of active filters [4]. It has the capability to instantiate low-voltage filters based on the trans conductor design methodology for the purpose of designing low-voltage signal processing filters. A transconductor's configuration typically resembles an operational amplifier, albeit with a distinct variation in output impedance. Novel techniques were devised and implemented to enhance the performance of trans conductors.

2. Method

Improved Floating Current Source (F.C.S)

The schematic representation of the generic (F.C.S) and its corresponding electrical symbol are depicted in (Figure 1) [8]. The system primarily comprises two interconnected complementary Long-Tailed Pairs (LTPs) denoted as M7-M8 and M5-M6. These LTPs generate tail currents supplied by the output stages of the two current mirrors, M3-M4 and M1-M2. Assuming that the input terminals INP and INM are subjected to a relatively small differential signal, it can be observed that the nodes ComoutP and ComoutM exhibit characteristics of small signal virtual grounds, which implies that the small signal voltages at these nodes are effectively zero, and the currents delivered by M1-M2 and M3-M4 remain constant despite finite output impedance. It can be deduced that the small signal output currents I_{out} - = I_{out} + are equivalent, and

the floating current source (F.C.S) remains unaffected despite the presence of a standard mode (CM) DC offset between them, given that I (M1, M2) is not equal to I (M3, M4). The (F.C.S) has demonstrated its versatility as a fundamental component, well-suited for utilization as a standard cell, exhibiting a performance that surpasses the Long-Term Potentiation (LTP) [3]. The (F.C.S) is designed to deliver two symmetrical output currents, as depicted in the block diagram illustrated in Figure 1. The currents flowing through these two output terminals are determined by

$$I_{O1} = -I_{O2} = -\frac{1}{2}.vd\left[\sqrt{Kn}.\sqrt{2I_B - \frac{Kn.vd^2}{4}} + \sqrt{Kp}.\sqrt{2I_B - \frac{Kn.vd^2}{4}}\right] \tag{1}$$

$$Vd = V_1 - V_2 \tag{2}$$

V2 and V1 refer to the applied voltages to Y2 and Y1, respectively. 2IB refers to the F.C.S bias current. Kp and Kn are technology factors of the pMOS and nMOS transistors, respectively, and specified by:

$$Kn = \mu_n Cox \frac{W_1}{L_1}$$
$$Kp = \mu_p Cox \frac{W_4}{L_4} \tag{3}$$

Where μ_p and μ_n are the PMOS and NMOS transistors mobility, respectively. Cox refers to the oxide capacitance/unit area. $\frac{W_4}{L_4}$ and $\frac{W_1}{L_1}$ refer to the aspect proportions of transistors M4 and M1, respectively [4].

The enhanced (F.C.S) exhibits a highly streamlined architecture, as depicted in Figure 1. Utilizing two distinct transconductance magnitudes, Gm, and its frequent application in contemporary research render the Field-Effect Current Source (F.C.S) a valuable tool. The transconductance (Gm) of the system can be dynamically adjusted by utilizing bias current in the operational transconductance amplifier (OTA) configurations. The operational principle of developmental Field-Effect Transistor (FET) Current Source (F.C.S) bears resemblance to that of Operational Transconductance Amplifier (OTA). However, it is essential to note that the operational transconductance amplifier (OTA) typically has a single transconductance magnitude, denoted as Gm. On the other hand, in the case of the fully differential cascode stage (F.C.S), there are two distinct transconductance magnitudes, referred to as Gm1 and Gm2. The Improved Floating Current Source's output impedance exhibits a higher magnitude than the floating current source originally suggested by Arbel and Goldminz [5]. The conventional Floating Current Source is enhanced by incorporating M5, M6, M7, and M8 transistors to achieve elevated output resistance magnitudes. The presence of a high output resistance is imperative in voltage-mode configurations, as depicted in the formula. Consequently, the conventional Enhanced Floating Current Source is favoured per established electrical engineering principles. A high output resistance yields superior performance in the low-frequency domain. The output current of the Enhanced Floating Current Source can be determined by performing the multiplication operation between the voltage disparity across the P and N terminals and the transconductance (Gm). The transconductance (Gm) for the P terminal can be expressed as the ratio of g3 to g4 divided by 2. On the other hand, the transconductance for the n terminal can be calculated as the negative sum of g1 and g2 divided by 2. The capacitors are electrically coupled to the structure to avoid including resistive elements [11-12]. In this research, a suggested Gm-C filter application is presented. The output impedance of the system will be reduced as the circuit's output voltage is enhanced, eventually leading to VDSsat oscillations. The output resistance is specified in Farads per Coulomb-second (F.C.S) [6].

$$r_{out+} = r_{out-} \cong \left[\left(\frac{gm4gds3gds8}{gm8(gm3+gm4)}\right) + \left(\frac{gm1gds2gds6}{gm6(gm2+gm1)}\right)\right] \tag{4}$$

The advantage of the structure of the F.C.S's simplicity and use for high-frequency applications, while being suitable for connecting the four or eight transistors utilized in a row due to low supply voltage for buildings, constitutes the disadvantage.

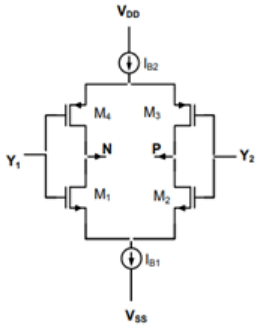

Figure 1: Diagram showing the enhanced floating current source [7]

Table 1 provides the dimensions of the transistors, while Table 2 presents the circuit's direct current (DC) magnitudes. The operational characteristics of the suggested circuit are exemplified on a 6th-order bandpass ladder filter configuration, as depicted in Figure 1.

Table 1: Transistor dimensions

Device	W(μm)	L(μm)
M_1,M_2	18	0.18
M_3,M_4	72	0.18

Table 2: DC magnitudes of enhanced Floating Current Source

Parameters	Magnitude
V_{DD}=-V_{SS}	0.9V
I_{B1} = $I_{B\,2}$	300μA

A 6th-order bandpass ladder passive filter

A 6th-order leap-frog filter has been implemented utilizing the transconductor depicted in Figure 2. The filter is obtained through the utilization of the passive LC ladder filter. [6].

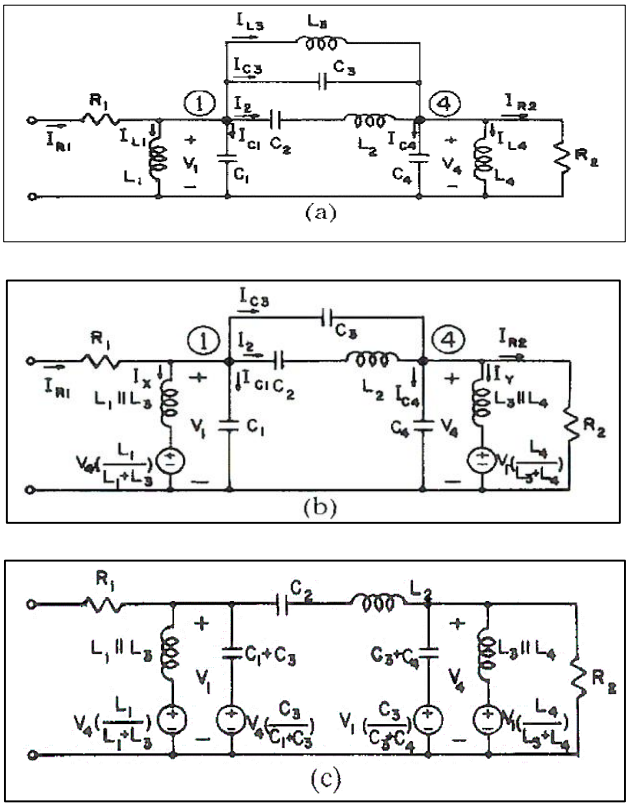

Figure. 2. (a) Doubly terminated sixth-order elliptic bandpass LC ladder, (b) Inductor L, represented by a voltage-controlled voltage source, (c) Final Thevenin equivalent circuit of Figure 2(a) [4]

As depicted in Figure 2, a doubly terminated sixth-order elliptic bandpass filter is illustrated. It has been needed to determine the Final Thevenin equivalent circuit to transform this circuit into a Butterworth bandpass filter. By formulating the nodal formula at node (l), it can derive the following expression.

$$I_{R1} - \frac{V_1}{SL_1} - I_{C1} - I_2 - I_{C3} - \frac{V_1 - V_4}{SL_3} = 0 \tag{5}$$

Rewriting (4), to be;

$$V_1 = (I_{R1} - I_{C1} - I_2 - I_{C3}) \frac{SL_1L_3}{L_1 + L_3} + V_4 \frac{L_1}{L_1 + L_3} \tag{6}$$

In a similar vein, formulating the nodal formula at node (4) will yield:

$$V_4 = (I_{C3} + I_2 - I_{C4} - I_{R2}) \frac{SL_3L_4}{L_3 + L_4} + V_1 \frac{L_4}{L_3 + L_4} \tag{7}$$

Based on equations (5) and (6), it can be observed that the inductor L3 can be equivalently modelled utilizing two voltage-controlled voltage sources, each associated with a specific alteration in the inductor characteristics, as depicted in Figure 2(b). Similarly, to eliminate capacitor C_3, it has been formulated the nodal formula at node (1) as depicted in the diagram. 2 (b) can be expressed as an electrical engineering notation.

$$I_{R1} - I_X - I_2 - V_1(SC_1) - (V_1 - V_4)SC_3 = 0 \tag{8}$$

Or

$$V_1 = (I_{R1} - I_X - I_2) \frac{1}{S(C_1 + C_3)} + V_4 \frac{C_3}{C_1 + C_3} \tag{9}$$

Likewise, for node (4)

$$V_4 = (I_2 - I_Y - I_{R2}) \frac{1}{S(C_3 + C_4)} + V1 \frac{C_3}{C_3 + C_4} \tag{10}$$

Equations (9) and (10) resulting in the final circuit shown in Figure. 2(c).

3. Result

Simulations

The simulations use the LTSPICE software, employing the TSMC CMOS 0.18 μm process variables. The block diagram depicting the suggested 6th-order Elliptic and Butterworth Gm-C bandpass filters is illustrated in Figure 3 and Figure 4 correspondingly. The proposed filter block diagram represents the filter equivalent to the ladder filter depicted in [Figure 1a] and [Figure 1c]. The Butterworth and Elliptic ladder filter component magnitudes are provided in Table 3, showcasing the crucial electrical engineering aspects of these filters, which comprise passive elements. The Gm-C filter component magnitudes and performance variables are presented in Table 4, as per the electrical engineering specifications.

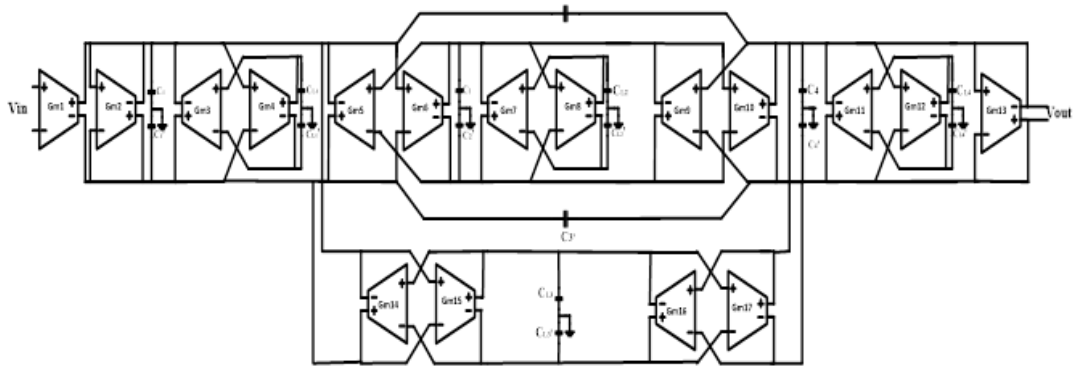

Figure 3: Sixth-order elliptic differential Gm-C bandpass filter block diagram

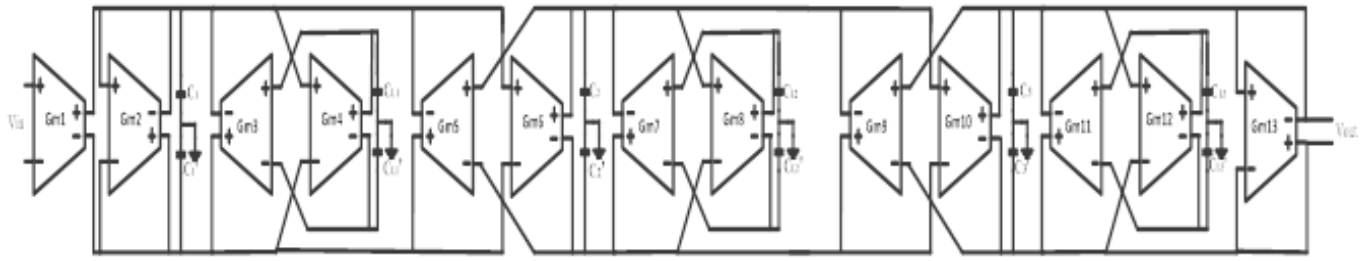

Figure 4: The sixth-order Butterworth differential Gm-C bandpass filter block diagram

Table 3. Ladder filter component magnitudes

Component	Magnitude Elliptic filter	Magnitude Butterworth filter
R_1, R_2	100Ω	100Ω
L_1	125nH	125nH
L_2	2.251µH	2.251µH
L_3	2.251µH	125nH
L_4	125nH	-
C_1	225pF	225pF
C_2	12.5pF	12.5pF
C_3	12.5pF	225pF
C_4	225pF	-

Table 4: Gm-c filter component magnitudes and performance parameters

Component	Magnitude Elliptic filter	Magnitude Butterworth filter
$C._{L1}$	0.4pF	0.4pF
$C._{L2}$	12.3pF	12.3pF
$C._{L3}$	0.4pF	0.4pF
$C._{L4}$	12.2pF	-
I_L	400µA	150µA
I_R	100µA	400µA
G_M Parameter		
$g_{m1}==g_{m3}==g_{m4}==g_{m5}==g_{m6}==g_{m7}==g_{m8}==g_{m9}$ $==g_{m10}==g_{m11}==g_{m12}==g_{m14}==g_{m15}==g_{m16}==g_{m17}$	2.817mA/V	-
$g_{m1}==g_{m3}==g_{m4}==g_{m5}==g_{m6}==g_{m7}==g_{m8}==g_{m9}==g_{m10}==g_{m11}==g_{m12}$	-	1.389mA/V
$g_{m2}==g_{m13}$	0.98mA/V	2.816mA/V

The current outputs at the n and p terminals of the enhanced Floating Current Source in response to the input voltage (VY1-VY2) can be observed in Figure 5. The output currents exhibit a variation of ± 300µA. Figure 6 demonstrates the Gm (transconductance) performance of the enhanced Floating Current Source, showcasing its commendable operation in the vicinity of 100 MHz frequencies. Furthermore, Figure 7 provides an insightful depiction of the alternating current (AC) features of the Floating Current Source (F.C.S). The ladder circuit depicted in Figure 3 and the suggested design illustrated in Figure 4 have been simulated utilizing the component magnitudes specified in (Table 3, 4). The outcome is depicted in Figures 8 and 9.

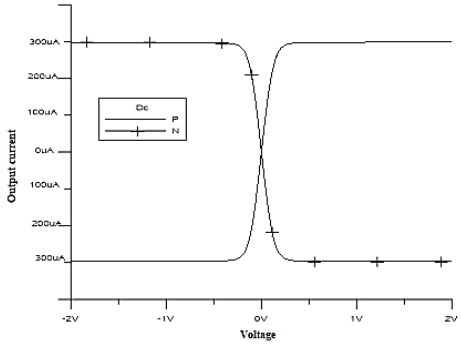

Figure 5: The enhanced floating current source's DC transfer feature.

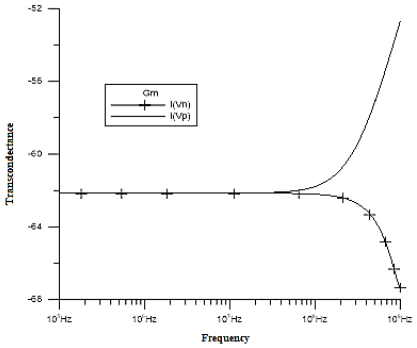

Figure 6: The enhanced floating current source G_m AC transfer feature

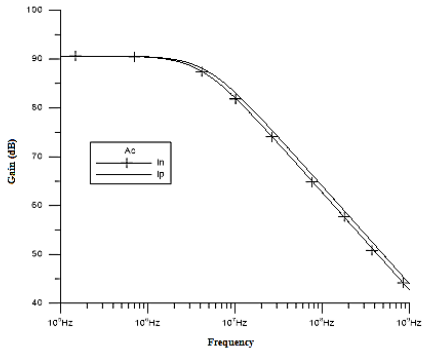

Figure 7: An enhanced floating current source with AC features

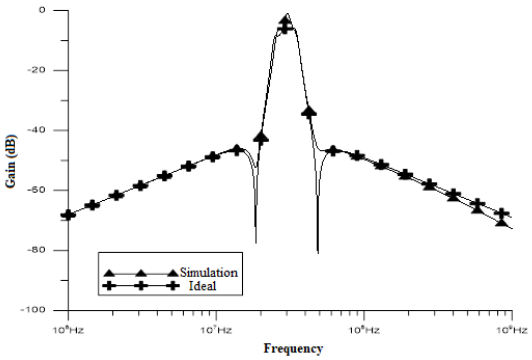

Figure 8: Ideal and simulated Elliptic the sixth order differential Gm-C bandpass filter frequency responses.

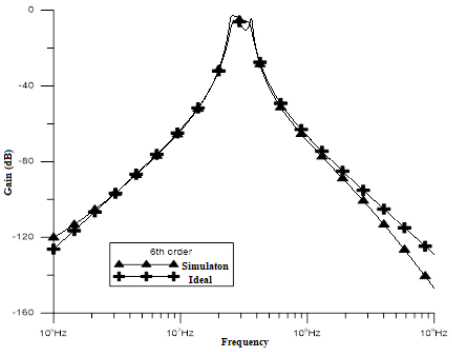

Figure 9: Ideal and simulated Butterworth the sixth order differential Gm-C bandpass filter frequency responses.

The simulation outcomes of the ideal and suggested sixth-order differential Gm-C bandpass filter are presented. The simulated filter responses in LTSPICE exhibit a center frequency of 30MHz. The theoretical center frequency was determined by evaluating $\omega 0 = 2\pi \times 30.05$ MHz, utilizing the data provided in Table 4. The simulation findings obtained from our experiments exhibit a satisfactory correspondence with the theoretical outcomes. Figures 8 and 9 exhibit the

potential applicability of the suggested filters within contemporary RF communication circuits, given that the filters function at intermediate frequencies within a superheterodyne (superhet) receiver. The suggested bandpass filter was subjected to significant signal analysis, wherein a sinusoidal signal with varying amplitudes at a frequency of 10 MHz was applied to the input. Simulations conducted on the filters have demonstrated a Total Harmonic Distortion (T.H.D) below 4% at a frequency of 10MHz. The cumulative harmonic distortion gradually increases proportionately to the input voltage, which remains below 400m Vpp [8-10].

4. Conclusion

This work describes a Gm-C filter implemented in a standard CMOS process, operating at high voltage and low power. Utilizing (F.C.S) made it feasible to achieve high-frequency operation while maintaining a low supply voltage. The (F.C.S) exhibits similarities to the Operational Transconductance Amplifier (OTA). However, the Fully Differential Cascode Structure exhibits superior performance compared to the Operational Transconductance Amplifier (OTA) due to its inclusion of two distinct transconductance (Gm). In contrast, OTA only possesses a single Gm. The (F.C.S) exhibits a straightforward and uncomplicated architecture. The transconductance (Gm) of the device can be dynamically adjusted by utilizing bias current control techniques. The center frequency of the filter is approximately 30 megahertz (MHz). The simulation findings exhibit a favorable correspondence with the theoretical outcomes. The sixth-order bandpass filter (BPF) was realized utilizing standard CMOS TSMC 0.18μm technology, incorporating capacitors. Figure 10 exhibits a die photograph of the filter, wherein the circuit's overall size, encompassing the pads, amounts to 2.4mm^2 for the elliptic filter.

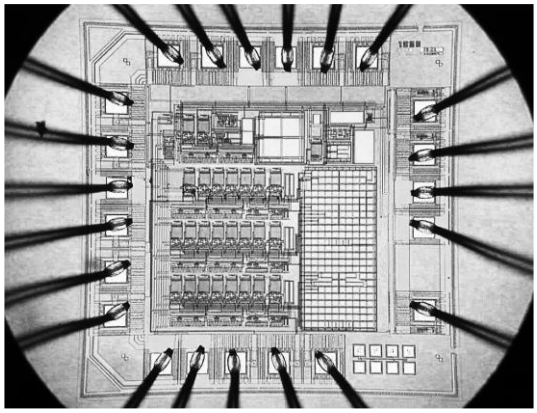

Figure 12: Die photograph of elliptic BP Gm-c filter.

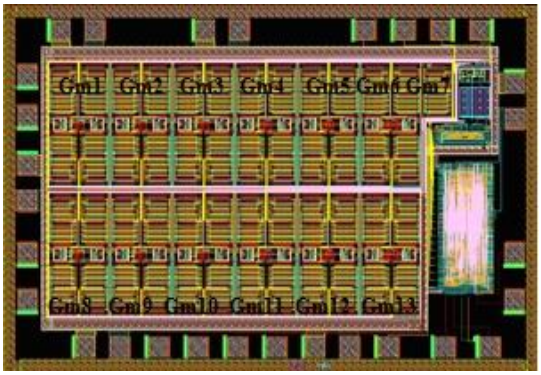

Figure 13: Die photograph of Butterworth BP Gm-c filter

Furthermore, Figure 12 portrays the layout of the receiver. The die, encompassing the pads, occupies a compact area measuring 2.66mm x 2.22mm. Figure 11 illustrates the schematic representation of the (13 part) Gm and capacitor Butterworth filter. The proposed filter functions at intermediate frequencies and applies to contemporary RF communication circuits. The LTSPICE simulations demonstrate satisfactory circuit performance with minimal total harmonic distortion. The enhanced current source architecture exhibits a streamlined configuration with fewer transistors. Hence, it can achieve enhanced circuit design simplicity by effectively utilizing the chip area and mitigating investment costs. The filter lacks the presence of a resistor, and all capacitors are effectively connected to the ground. Hence, it is well-suited for seamless integration and exhibits reduced susceptibility to parasitic influences.

Conflict of Interest

The authors have no conflicts of interest to declare.

Ethics Committee Approval

Not applicable

Author Contribution

Conceptization: HD, AAM; methodology and laboratory analyzes: HD, AAM; writing draft: HD, AAM; proof reading and editing: HD, AAM. Other: All authors have read and agreed to the published version of manuscript.

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