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# New FinFet Transistor Implementation of Floating and Grounded Inductance Simulator Based on Active Elements.

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## ABSTRACT

This research presents a new Finfet transistor that utilizes current mode active device technology to construct a floating and grounded inductance simulator. In this work, the grounded inductance circuit (GIC) uses only two Z-copy current follower transconductance amplifiers (Zc-CFTA's) and one grounded capacitor, and the floating inductance circuit (FIC) in the suggested simulator uses just three Z-copy current follower transconductance amplifiers (ZC-CFTA's) as active elements with only a single grounded capacitor as an active inductor simulation. The aim of this work is to realize an active inductance simulator with only one capacitor, which is commercially available as an active building block (ABB). In addition, the designed circuit shows low incremental active and passive hypersensitivity and non-interactive electronic control of the quality factor (Q) and natural angle frequency ($w_0$). Through computer simulation results with a fourth-order Butterworth band-pass filer using LT-spice and a cadence virtuoso program with a 7nm process parameter, the suggested circuits' performances were assessed.

**Keywords:** Finfet transistor, floating and grounded inductance simulator, Z-copy CFTA (ZC-CFTA).

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# Aktif Elemanlara Dayalı Yüzen ve Topraklanmış Endüktans Simülatörünün Yeni FinFET Transistör Uygulaması.

## ÖZ

Bu araştırma, yüzen ve topraklanmış bir endüktans simülatörü oluşturmak için Akım mod aktif cihaz teknolojisini kullanan yeni bir Finfet transistörü sunmaktadır. Bu çalışmada, topraklanmış endüktans devresi (GIC) yalnızca iki Z-kopya akım takipçisi traniletkenlik amplifikatörü (ZC-CFTA'ler) ve bir topraklanmış kapasitör kullanır ve önerilen simülatördeki yüzen endüktans devresi (FIC), aktif bir indüktör simülasyonu olarak yalnızca tek topraklanmış kapasitörle aktif elemanlar olarak sadece üç Z-kopya akım takipçi traniletkenlik amplifikatörü (ZC-CFTA) kullanır. Bu çalışmanın amacı, ticari olarak aktif yapı taşı (ABB) olarak temin edilebilen tek bir kapasitörle aktif endüktans simülatörü gerçekleştirmektir. Ek olarak, tasarlanan devre düşük artımlı aktif ve pasif aşırı duyarlılık ve kalite faktörünün (Q) ve doğal açı frekansının ($w_0$) etkileşimli olmayan elektronik kontrolünü gösterir. Dördüncü dereceden Butterworth bant geçişli filtre kullanan LT-SPICE ve 7nm işlem parametresine sahip cadence virtüöz programı ile bilgisayar simülasyon sonuçları ile önerilen devrelerin performansları değerlendirildi.

**Anahtar Kelimeler:** Finfet transistör, yüzer ve topraklanmış endüktans simülatörü, Z-kopya CFTA (ZC-CFTA)

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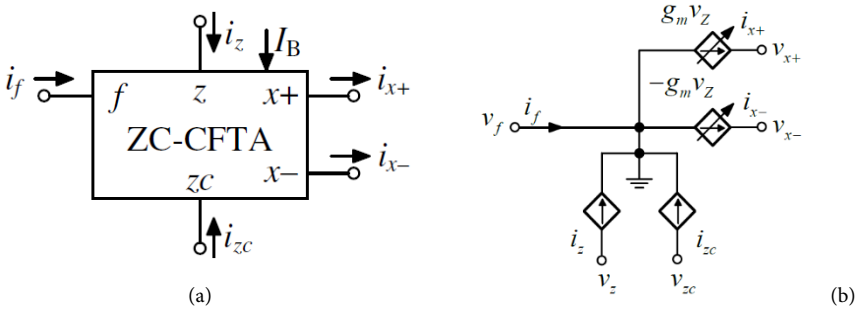
## 1. Introduction

Current differential conduction amplifiers (CDTA) are a new type of current mode device that offers flexibility and full functionality. It has been widely used in analog inductor, analog filter, and sinusoidal oscillator designs. However, in most of the circuits that have been reported, 2 or more CDTAs have been used, and useless P- or N-terminals have appeared, which not only creates a success rate It's wasteful, and it can also cause noise interference. For this reason, an improved version of CDTA has appeared, and people call it a current follower transconduction amplifier (CFTA). CFTA-based general filters have been reported, but CFTA-based ground-analog inductors and floating analog inductors are not common. The author was inspired by literature [1-7] to replace CDTA in simulated inductor circuits with CFTA, which realizes a grounded analog inductor and a floating analog inductor, respectively. The circuit uses ground capacitors, has minimal active components, and has no suspended input and output terminals. It is an analog inductor circuit with minimal components. To prove the reliability of the circuit operation, based on this floating and ground analog inductor, a fourth-order Butterworth band pass filter was designed separately using component replacement methods. The main feature is that the pole frequency can be adjusted linearly by electric regulation. Computer simulation shows that the circuit designed correctly is effective.

## 2. Description Of Active Elements

It is an active device suitable for use in analog signal processing in both voltage and current modes. The CFTA is a three-pole active device. On the input side, there will be only one terminal, the f-terminal, and the output will have the same structure as CDTA, that is, it will consist of a z terminal, and the symbol x and the electrical equivalence circuit of the CFTA are represented in Figure 1. The relationship between the incoming and outgoing currents is explained as follows: The current at the z pole will be equal to the current flowing at the f pole, while the current at the x pole will be the transmission, transferred from the voltage at the z pole, so at the z pole there will be a voltage. external loads will have to be brought in. The ± design indicates the direction of the current at the x pole; normally, the current at the x pole flows out. On the ideal side, the CFTA is designed to have a resistance value; on the input side, the f terminal has a value of zero, while the z and x terminals are designed to have an infinite resistance value based on said property. The root can be represented by a metric equation, as in equation 1 [7-9].

$$\begin{bmatrix} Vf \\ Iz \\ Izc \\ +Ix \\ -Ix \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & +gm & 0 & 0 & 0 \\ 0 & -gm & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} Vf \\ Vz \\ Vzc \\ +Vx \\ -Vx \end{bmatrix} \quad (1)$$




(a) (b)

Figure 1. Zc-CFTA (a) Electrical Symbols and (b) Electrical Equivalent Circuits.

When gm is the transfer conductance value, the gm value can be controlled by adjusting the bias current ($I_B$) on the input side.

The *gm* values of Zc-CFTAs designed with Finfet transistor technologies are shown in equations (2) and (3), respectively. The internal circuits designed for the Zc-CFTA with Finfet transistor technology are shown in Figure 2.

$$Iz = Izc = If, Vf = 0, Ix\pm = \pm gmVz \quad (2)$$

$$g_m = \frac{I_B}{2.V_T} \tag{3}$$

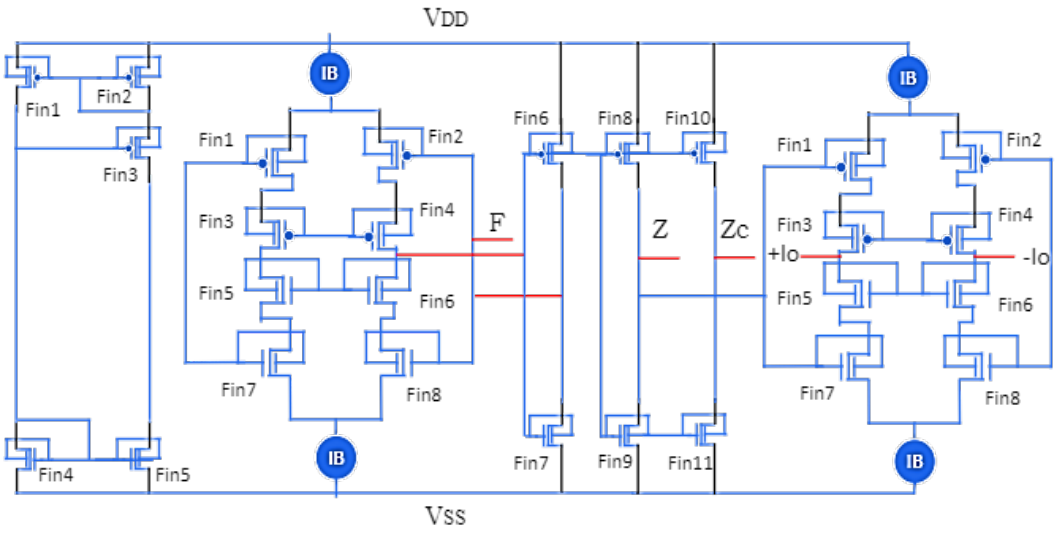



Figure 2. Finfet transistor realization of the z-copy CFTA used in simulations.

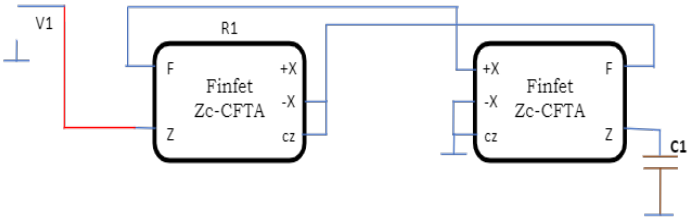
Among them, gm is the transconductance gain of the Zc-CFTA, VT is the thermal voltage, and IB is the bias current of the transconduction amplifier. It is the bias current of the transconduction amplifier, and the x can be freely taken between the x- and x-end of the transconduction amplifier [10-12]. Figure 3 shows a new active analog inductor simulator. Figure 3 (a) is a ground-analog inductor simulator based on Zc-CFTA. It can be obtained from Figure 3 (a).

$$I_1 == -I_{z1} == -I_{x2} == \pm\frac{g_{m2}.I_{z2}}{s.C_1} = \frac{g_{m1}.g_{m2}.V_1}{s.C} \tag{4}$$

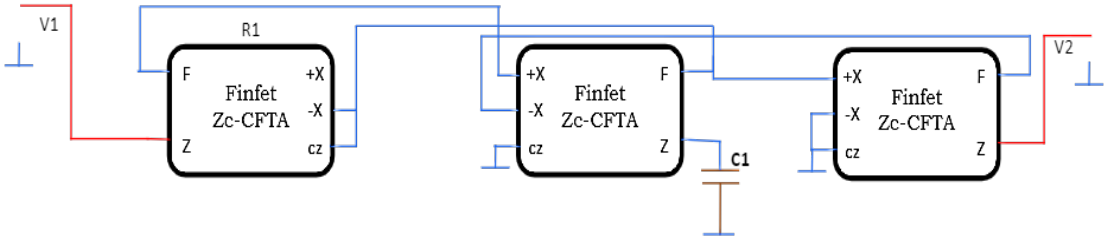
$$Z_1 = \frac{V_1}{I_1} = \frac{s.C}{g_{m1}.g_{m2}} \tag{5}$$

Therefore, from the above equation and formula (2), the equivalent inductance can be obtained as:

$$Lequ. = \frac{4.V_T{}^2.C_1}{I_B} \tag{6}$$




(a)




(b)

Figure 3. New active analog inductor simulation based on Zc-CFTA: (a) Finfet Zc-CFTA-based grounded analog inductor simülatör (b) Finfet Zc-CFTA based on floating analog inductor simulator.

Figure 3 (b) is a floating-simulated inductor simulator based on Zc-CFTA. And select gm=gm1=gm2. From

Figure 3 (b), we can get:

$$I_1 == -I_{x3} == -I_z = \frac{-g_{m3}(I_{x2}-I_{x1})}{sC} = \frac{g_{m3}g_{m2}g_{m1}(V_1-V_2)}{sC} \quad (7)$$

$$I_2 = I_1 == I_{x3} == I_{z3} == \frac{g_{m3}.I_{z3}}{sC} \quad (8)$$

It can be obtained from the above equation:

$$Z_1 = \frac{(V_1-V_2)}{I_1} = \frac{sC}{g_{m1}.g_{m2}.g_{m3}} \quad (9)$$

Therefore, from the above equation (9), the equivalent inductance can be obtained as

$$L_{equ} = \frac{4.V_T{}^2.C}{I_B} \quad (10)$$

## 3. Application Of A Novel Active Analog Inductor

The suggested floating and grounded inductance simulator is implemented in a fourth-order Butterworth band-pass filter realization to demonstrate its usage. The passive circuit in Fig. 4 has a transfer function that is provided by:

$$T.F_{BPF} = \frac{s(R_2/L_{equ}.)}{s^2+s(R_2/L_{equ}.)+(1/L_{equ}.C)} \otimes \frac{s(R_2/L_{equ}.)}{s^2+s(R_2/L_{equ}.)+(1/L_{equ}.C)} \quad (11)$$

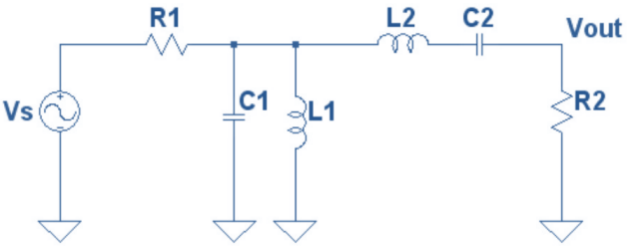



Figure 4. Passive circuit fourth order Butterworth band-pass filter

The cutoff frequency and quality factor of the bandpass filter can be calculated by:

$$Fo = \frac{1}{2\pi}\sqrt{\frac{1}{Lequ.C}} \quad (12)$$

$$Q = \frac{1}{R1}\sqrt{\frac{Lequ.}{C}} \quad (13)$$

Figure 4 shows a classic fourth-order Butterworth band-pass filter, where $R_1$ and $R_2$ are the internal resistance of the signal source and the load resistance, respectively. Where the value of $C_1$=$C_2$=0.1uF, $R_1$=$R_2$=1Ω and the passive inductance values $L_1$=$L_2$=0.41 H. the cutoff frequency of the band pass filter to be designed $F_o$=1kHz with Q=1.2,

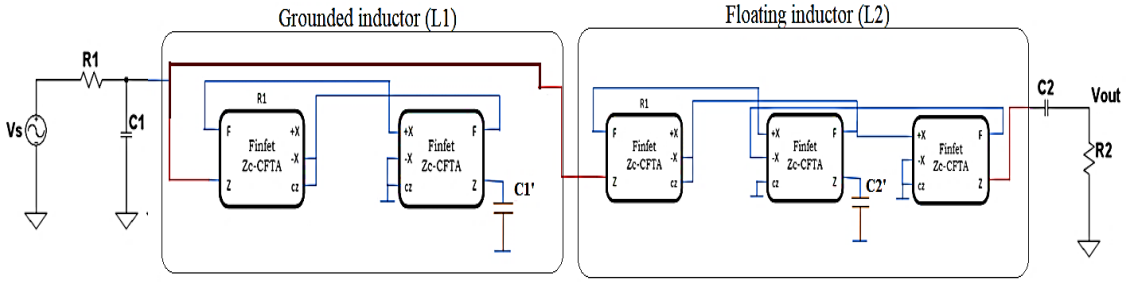



Figure 5. Fourth-order Butterworth band-pass filter based on Zc-CFTA.

By replacing L1 and L2 in the Figure 4 circuit with the flouting and grounded analog inductor in Figure 3, a fourth-order Butterworth band-pass filter based on Zc-CFTA can be obtained, as shown in Figure 5. The values of C1 and C2 are equal to 1pf and the bias currents ($I_B$) in the analog inductors $L_1$ and $L_2$ are 173nA. Similarly, the cutoff frequency of the fourth-order Butterworth band-pass filter also satisfies Equation 12, so its cutoff frequency can also be adjusted by linear electronic control of the bias current.

## 4. Results of the simulation

The simulation results were obtained using the Cadence virtuoso and Lt-SPICE simulation programs, which demonstrated the performance of the suggested floating and grounded inductance simulators illustrated in Figure 3 (a and b). With supply voltages $V_{SS}$=$V_{DD}$ = 0.1 V, the Finfet transistor implementation presented in Figure 2 is used to emulate the active components of ZC-CFTAs. The 7nm process characteristics are used to model Finfet transistors. The active parameters and passive element values given below were used to simulate the proposed grounded and variable-inductance active circuit seen in Figure 3. (a and b): $I_B$ = 173nA, $R_1$ = $R_2$ = 1 Ω, and $C_1$ = $C_2$ = 0.1 uF, which provides Leqe. = 1 uH. Fig. 6(a and b) illustrates the magnitude and phase responses for both grounded and flouting inductance, both theoretical and simulated. Using the circuit from Fig. 5, a fourth-order band-pass filter has been constructed. The obtained Q values from the simulations equal 1.2. In Figure 7, the ideal and simulation magnitude responses of the fourth-order BPF are displayed.

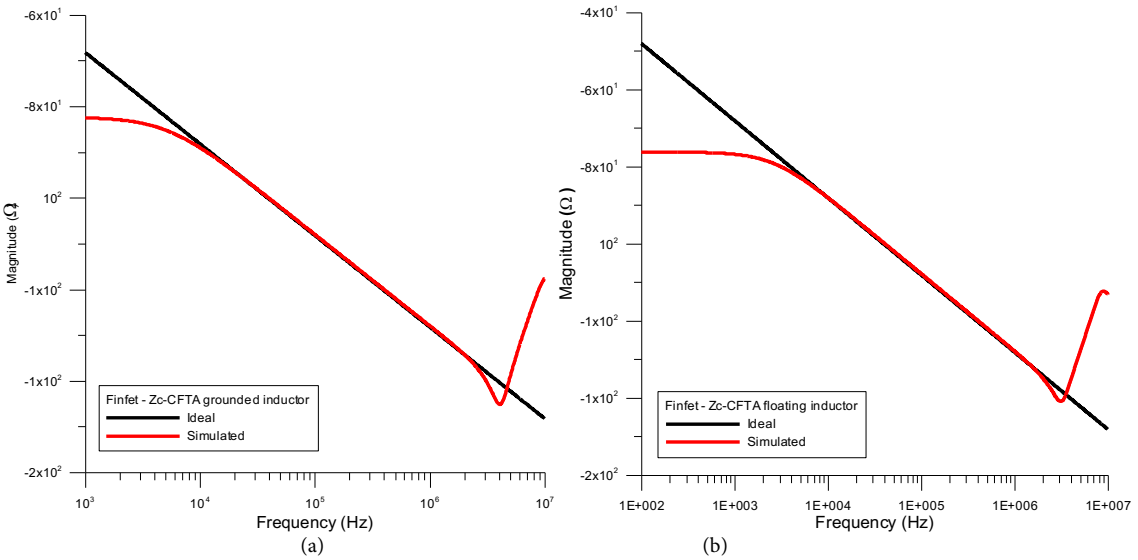



Figure 6. The ideal and simulated magnitude of a Finfet Zc-CFTA-based (a) grounded (b) floating analog inductor simulator.

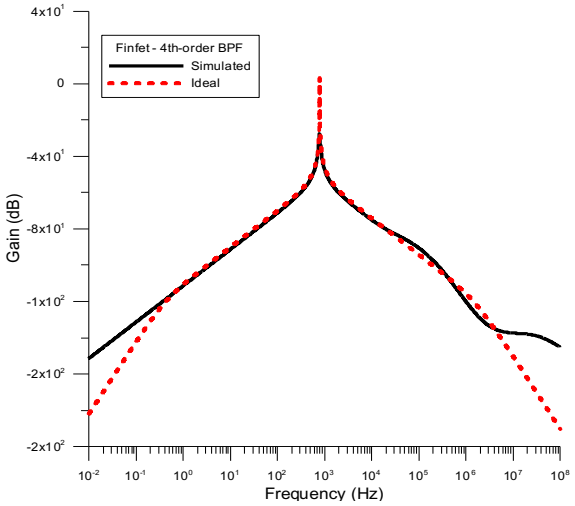



Figure 7. The fourth-order BPF filter's ideal and simulation gain outputs are illustrated in Fig. 5.

## 5. Conclusion

This article uses Finfet transistors for the internal design stage instead of CMOS, BJT, or any other type of transistor. Using Z-copy CFTAs as an active element, a grounded analog active inductor simulator and a floating analog active inductor simulator were designed and used for the design of a fourth-order Butterworth band-pass filter in the voltage mode. Compared with relevant literature, the characteristics of this analog inductor simulator are: whether it is a ground or floating analog inductor, it is non-destructive, so it is flexible to use; it uses a ground capacitor, so it is suitable for integration; there are few active components; and the number of input and output terminals is minimal. Thus, the circuit stability is high and the power consumption is low. Through used cadence virtuoso and LT-SPICE as a computer simulation of a fourth-order Butterworth band-pass filter, the analog inductor design is shown. It's correct and effective for analog filters, its shown in figure 7 that the cutoff frequency is equal to 1KHz, so it can be used in various analog signal processing circuits. In future can used other parameter like 3nm and 1nm to change the electronic revolution from microelectronics to nanoelectronics that is used in new technology.

## Conflict of Interest Statement

The authors declare that there is no conflict of interest.

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