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Research Article

Design and Testing of a Wireless Communication Enabled FPGA Development Board: A Comprehensive Education and Application Platform from IoT to Circuit Design

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ABSTRACT

Field Programmable Gate Array (FPGA) is an integrated circuit (IC) that can be reprogrammed or configured by the customer or designer after production for rapid prototyping and post-process development. In this study, a cost-effective FPGA development board is designed to create basic engineering education applications and implement them in real-time. The Printed Circuit Board (PCB) design of the FPGA development board layout was precisely crafted using EasyEDA software to ensure robust and reliable connectivity between the FPGA and its peripherals. The FPGA development board utilizes an Altera Cyclone IV E-series chip and includes Bluetooth and Wi-Fi modules to provide a wider range of applications. This integration simplifies the use of wireless communication in various projects and applications for researchers and engineers. To verify the accuracy of the proposed board, simulations of selected digital designs and Bluetooth applications were first performed in VHDL (Very High Speed Integrated Circuit Hardware Description Language) using Intel® Quartus® Prime Lite Edition software. Then, experiments were performed on the board following the pin assignment configurations. It was observed that the developed applications worked successfully on the FPGA development board. As a result, this board, equipped with Bluetooth and Wi-Fi modules, offers a fast and cost-effective solution for users in various fields such as mobile, robotics, smart home systems, and remote monitoring and control devices.

1. INTRODUCTION

Digital Logic Design course has an important position in the curriculum for both computer engineering and the electrical engineering departments [1]. The objective of this course is to provide students to get their exposure to the hardware design by learning the basic concepts of digital design and performing their corresponding experiments. It is very important that the content of the digital design course reflects the current design styles used in the industry. For this reason, FPGA (Field Programmable Gate Array) technology has been incorporated into the experimental education of digital logic design course in order to train expert engineers to adapt to the development trend of digital electronic technology that the industry requires.

FPGAs are programmable, reconfigurable semiconductor devices developed for the purpose of implementing and testing the digital circuits required by the designer [2-4]. FPGAs are generally used to create prototypes of newly designed ASIC circuits or to test the physical implementation of an algorithm. Today, FPGAs are used in a wide range of areas, especially in the military and defense industry [5], communications [6], audio [7] and image processing [8], automotive [9,10] and consumer electronics [11,12].

When developing FPGA-based applications, usually existing development boards are preferred. Procuring these development boards from abroad and their high costs create difficulties in accessing development boards for researchers who want to improve and progress in this field. For this reason, in this study, a low-cost FPGA development board has been designed that can be easily accessed by students studying in universities, especially engineering faculties and vocational schools, academicians who want to develop applications, and anyone interested in hardware design as a hobby. Thus, with this developed board, students studying in relevant departments of universities will be able to access this development board in

a cost-effective manner and thus, students who are more equipped on FPGA can be trained. By adding Bluetooth and Wi-Fi modules that are not included in the Altera DE2 board, which is closest to it in the market, a wider range of application development areas have been created in this designed board.

The study is organized as follows: Related works about applications developed using the FPGA board are described in the second section, and the development of the FPGA development board is described in the third section. The VHDL software of the applications implemented using the FPGA development board and the processes regarding the results obtained as a result of assignment to the board are explained in the fourth section. In the fifth and last chapter, the cost study of the developed board was conducted and the results were interpreted.

2. RELATED WORKS

This chapter deals with FPGA technology under two separate subheadings. The first part presents the applications performed with the existing FPGA boards available in the market and produced by various companies. The second part presents new FPGA boards specially designed and developed by researchers for specific needs and the applications performed with these boards.

2.1. Studies Performed Using FPGA Development Board

Saif and et all. designed and implemented an educational processor based on RISC-V architecture on FPGA. Additionally, an assembler was designed and developed that can translate assembly code into RISC-V standard machine codes that can help the users to operate the CPU easily [13].

Surekha and et all described the VLSI (Very Large Scale Integration) design of an Arithmetic Logic Unit (ALU). The design has been simulated and tested by using Xilinx ISE design suite 14.7 that is a prominent tool in FPGA development. The proposed ALU design is generated a delay of 125.711 ns [14].

Panigrahi and et all. designed a 4-bit ALU using Xilinx VIVADO 2016.2 and analyze the design parameters on FPGA by using VERILOG. They simulated and synthesized the various parameters such as speed improvement, less power consumption and better utilization of ALU to measure the efficiency of an algorithm [15].

Sağlam and Kaçar designed a 64-bit ALU by using the VHDL and Altera FPGA families, synthesized and simulated with the help of Altera Quartus II and Modelsim-Altera v10.1d software. The proposed design allows the processing of the signed numbers and also Conditional Sum Adder (COSA) is used in addition operation instead of Carry Ripple Adder (CRA) or Carry Look-ahead Adder (CLA). The output of the addition operation was obtained in a shorter time that the adder with COSA is approximately 6 times faster than adder with CRA [16].

Karakaya and et all. introduced a systematic methodology for implementing digital piecewise linear (PWL) functions within nonlinear dynamical systems, enabling the representation of complete behaviors within a single model. The proposed design takes the number of scrolls as input and efficiently generates chaotic PWL signals using a reduced number of FPGA resources. The implementation stage of the study realized by using Xilinx Kintex-7 KC705 Evaluation Board [17].

2.2. Studies Designing and Developing FPGA Development Board

Keskin and Koyuncu designed an FPGA-based development board in their study. The development board was developed by selecting the FPGA chip of the XC2C64A-7-VQ44 family from Xilinx, and half adder and up counter applications were implemented as sample applications [18].

Zhao and et all designed a pocket development board that consists of two parts: the core circuit and the peripheral circuit. The core circuits include Altera company Cyclone IV series EP4 CE10 f-17 type FPGA chip, as the core of the hardware circuit of the control unit. Also the hardware circuit of the development board consists of the peripheral circuits that are LED lights, 6 seven-segment digital tubes, buttons and buzzers. These peripheral circuits can carry out independent experiments, and they can be combined with each other [19].

Gao developed Altera EPM7164S chip based FPGA Experiment and Development Board that has high on-board resource utilization, expandable, easy self-design and reasonable cost to overcome the shortcomings of fixed connections, large and fully functional of FPGA experimental box. FPGA Experiment and Development Board can use Quartus II integrated development environment to complete the design. It is suitable for VHDL hardware language and Verilog hardware language [20].

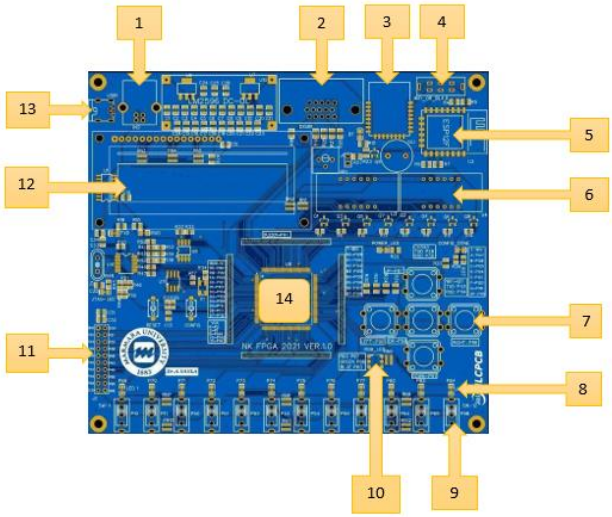
3. DESIGN PROCESS OF FPGA DEVELOPMENT BOARD

In this study, an FPGA development board was designed to execute fundamental digital logic design applications as well as Bluetooth and Wi-Fi applications. EP4CE6E22C8N chip from the Altera Cyclone IV family was used as the FPGA chip in the design of the development board.

In the development of the FPGA board, first the connections of the FPGA chip with the peripherals were determined and the necessary PCB drawings were made using the EasyEDA program.

The features of the developed FPGA board can be listed as follows: EP4CE10E22C8N was used as the FPGA chip. There is an integrated JTAG interface for programming and debugging FPGA chip, 50MHZ crystal, 5 button inputs and AT24C04 Serial EEPROM for I2C serial communication protocol on the board. With the USB-TTL serial port on the board, it will be possible to communicate with external hardware units such as PCs and embedded systems in accordance with RS232 standards.

The board also includes 1 X 12 slide switches to obtain input at logic 0 and logic 1 levels in the experiments, 12-bit LEDs, 8 pieces of 7 segment displays with common anode coded 3461BS (4x2 indicator block) and a buzzer. There is also a 1602 character-type LCD (Liquid Crystal Display) interface, VGA display port for visual applications, Input/ Output Pins, a Bluetooth and Wi-Fi modules communicating with UART protocol on the board. The FPGA development board PCB layout and feature callout is shown in Fig. 1.



Callout	Component Description	Callout	Component Description
1	USB Type B	8	12 X LEDs
2	VGA Connector	9	12 X slide switches
3	Wi-Fi Module	10	RGB Led
4	Select jumper (Wi-Fi/Bluetooth)	11	GPIO Pins
5	Bluetooth Module	12	LCD Display
6	8 digit 7 Segment display	13	UART/JTAG USB Port
7	5 X push buttons	14	Altera Cyclone IV FPGA

Figure 1. FPGA board PCB layout design and feature callout

4. SAMPLE APPLICATIONS REALIZED ON DEVELOPMENT BOARD

Altera Intel® Quartus® Prime Lite Edition design software was used for testing this FPGA-based development board and coded using the VHDL language. 4-bit Arithmetic Logic Unit (ALU) design, 3- bit Down Counter design and Bluetooth application were realized on this board.

4.1. ALU Design

ALU is the main component of the central processing unit in the computer system, which means arithmetic logic unit and performs arithmetic and logic operations [14]. ALU mainly handles arithmetic operations such as addition, subtraction, division, multiplication, and logical operations such as “AND”, “OR”, “EXCLUSIVE OR (XOR)”, etc., and performs scroll-rotation operations [15].

In this study, a 4-bit ALU design, the diagram of which is shown in Fig. 2, was realized by using the switches and LEDs on the designed FPGA development board.

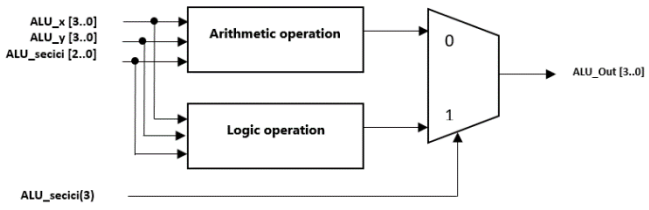


Figure 2. ALU Design Diagram

In this application, which is carried out using the VHDL hardware description language, the x and y inputs given as N bits, are set to 4 bits. The first 3 bits of the selective inputs, which is determined as 4 bits, are used to select arithmetic and logical operations, and the 4th bit determines which operation result will be transferred to the output in the MUX circuit. The table of arithmetic and logic operations that can be performed with this ALU design is given in Table I.

In this application, which was carried out using VHDL structural style, the necessary VHDL code files were first created to perform arithmetic and logical operations. Then, a main file called ALU was created to interconnect the components (arithmetic and logic) within an architecture. The VHDL code of the ALU main file is shown in Fig. 3.

TABLE I
ALU OPERATIONS AND SELECT LINES

Operation	Selective inputs	Function
Arithmetic operation	0 0 0 0	transfer the x value to the output
	0 0 0 1	x value increased by 1
	0 0 1 0	x value decreased by 1
	0 0 1 1	transfer the y value to the output
	0 1 0 0	y value increased by 1
	0 1 0 1	y value decreased by 1
	0 1 1 0	add the value of x to the value of y
	0 1 1 1	subtract the value of y from the value of x
Logical operation	1 0 0 0	NOT x
	1 0 0 1	NOT y
	1 0 1 0	AND (x and y)
	1 0 1 1	OR (x or y)
	1 1 0 0	NAND (Not AND)
	1 1 0 1	NOR (Not OR)
	1 1 1 0	XOR (Exclusive OR)
	1 1 1 1	XNOR (Exclusive NOR)

Before testing the created ALU application on the FPGA development board, it is necessary to test whether the codes work correctly or not as a simulation. MODELSIM program was used for this. For this process, first a test file was created. The testbench file of the ALU design is shown in Fig. 4.

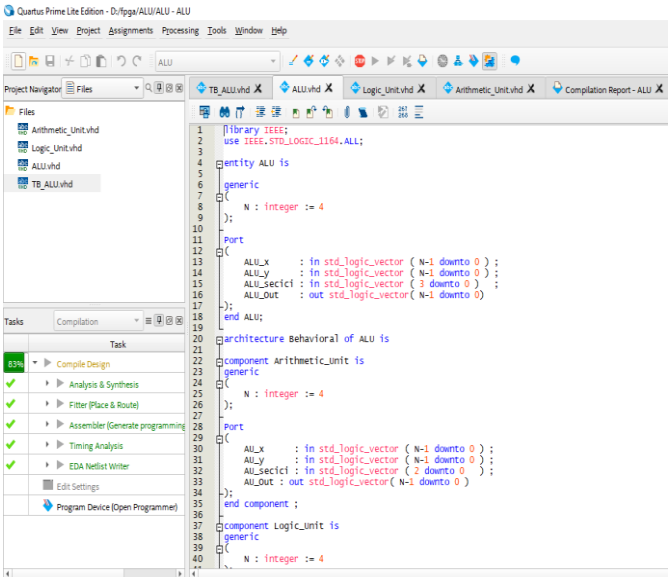


Figure 3. ALU Design VHDL File

RTL (Register Transfer Level) diagram visually illustrates how a design written in a hardware description language will be converted into gate-level logic during the logic synthesis process. This visualization allows the designer to evaluate the behavior and performance of the design and make improvements where necessary. The RTL diagram of the ALU design is shown in Fig 5.

```
library IEEE;
use IEEE.Std_logic_1164.all;
use IEEE.Numeric_Std.all;

entity ALU_tb is
end;

architecture bench of ALU_tb is

constant N : integer := 4;

  component ALU
  generic
  (
      N : integer := 4
  );
  Port
  (
      ALU_x      : in std_logic_vector ( N-1 downto 0 ) ;
      ALU_y      : in std_logic_vector ( N-1 downto 0 ) ;
      ALU_secici : in std_logic_vector ( 3 downto 0 )  ;
      ALU_Out    : out std_logic_vector( N-1 downto 0)
  );
  end component;

  signal ALU_x: std_logic_vector ( N-1 downto 0 );
  signal ALU_y: std_logic_vector ( N-1 downto 0 );
  signal ALU_secici: std_logic_vector ( 3 downto 0 );
  signal ALU_Out: std_logic_vector( N-1 downto 0) ;

begin

  -- Insert values for generic parameters !!
  uut: ALU generic map ( N          =>  N )
            port map ( ALU_x      => ALU_x,
                       ALU_y      => ALU_y,
                       ALU_secici => ALU_secici,
                       ALU_Out    => ALU_Out );

  stimulus: process
  begin

    ALU_x   <=  "0101";
    ALU_y   <=  "1010"; wait for 50 ns ;

    ALU_secici <=   "0000"; wait for 20ns; ALU_secici <=   "0001"; wait for 20ns;
    ALU_secici <=   "0010"; wait for 20ns; ALU_secici <=   "0011"; wait for 20ns;
    ALU_secici <=   "0100"; wait for 20ns; ALU_secici <=   "0101"; wait for 20ns;
    ALU_secici <=   "0110"; wait for 20ns; ALU_secici <=   "0111"; wait for 50ns ;
```

Figure 4. Testbench File for ALU Design

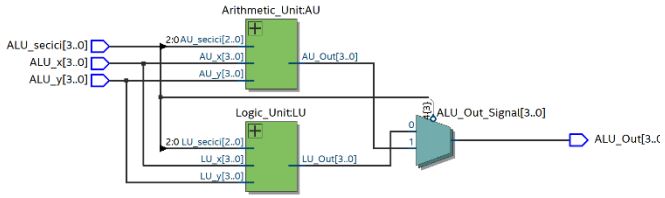


Figure 5. RTL Schema for ALU Design

In the test file, x input value was selected as “0101 (Decimal 5)” and y input value was selected as “1010 (Decimal 10-Hexadecimal A)”. The first 8 states of the 4-bit selective bit are used to select arithmetic operations and the last 8 states are used to select logic operations. The result screen obtained by running this simulation, in which all arithmetic and logic operations are tested, is shown in Fig. 6.

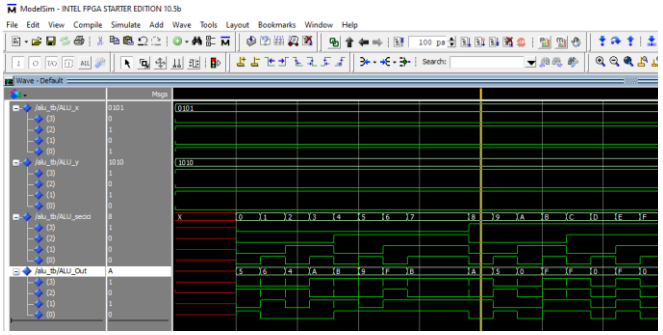


Figure 6. MODELSIM Simulation Result for ALU Design

In the next stage, the pin assignments of the FPGA chip are carried out so that the code tested to work correctly as a result of the simulation can be tested by placing it on the FPGA development board. The first 4 keys of the 12 keys of the FPGA board are designated for the selector bits, the next 4 keys are determined for the x value, and the last 4 keys are determined for the y value. In order to observe the results, 4 LEDs were selected as seen in Fig. 7.

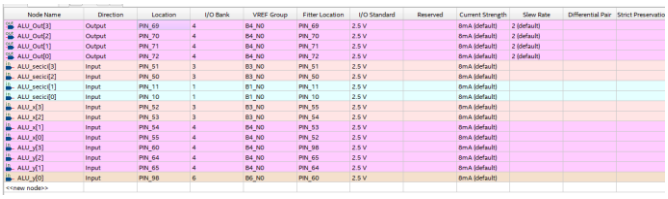


Figure 7. Pin Assignment for ALU Design

After the pin assignment is completed, the FPGA development board is programmed. Images of the ALU application performed on the designed FPGA development board are presented in Fig. 8 and Fig. 9, respectively.

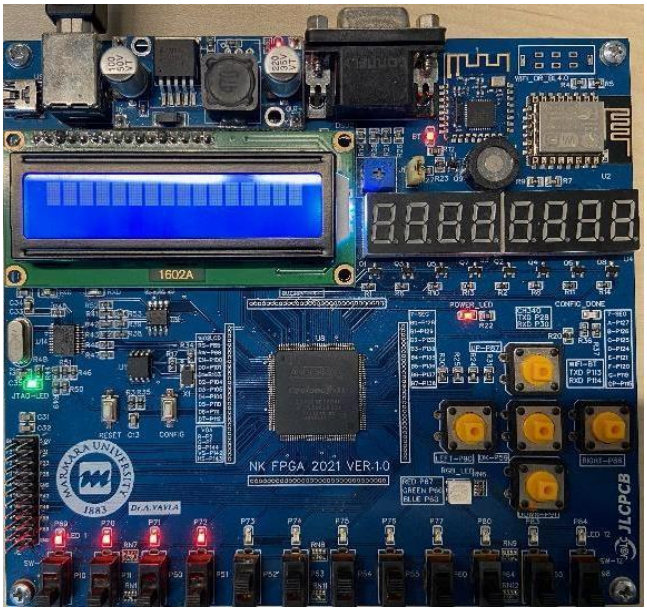


Figure 8. Selection Bits 0000 and s<= x (x =1111)

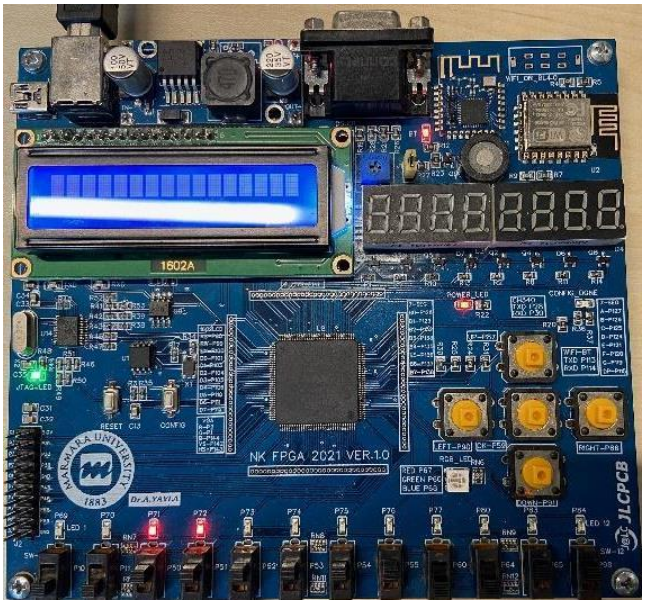


Figure 9. Selection Bits 0011 and s<= y (y =0011)

4.2. 3- bit Down Counter (Schematic Application)

3-bit down counter circuit has been designed as a schematic application in the Quartus® Prime Lite Edition design software, where both schematic and code design is possible. Since the designed FPGA development board has a 50 MHz crystal oscillator, changes that will occur in a counter application using this internal clock pulse may not be discernible by the human eye. For this reason, in the design of this application, a schematic design for a five-bit frequency divider using J-K Flip Flop which is the one-bit memory element was initially designed to reduce the internal clock pulse as seen in Fig. 10.

This frequency divider schematic file saved as symbol to be used in the 3-bit down counter circuit. The down counter designed by using J-K FF and 7447 BCD to Seven Segment Decoder was used to transfer the counter values to the seven segment display as seen in Fig. 11.

In this application designed with positive-edge triggering, after creating BDF files, the developed study was tested in a simulation environment to verify its correct functionality. In this study simulated using the University Program VWF, the necessary signals for driving the seven-segment display are illustrated in Fig. 12.

After the successful completion of the testing process in the simulation environment, the necessary pin assignments for the seven-segment display have been implemented, and the counting process has occurred as depicted in Fig. 13.

4.3. Bluetooth Application

In the board design, a Bluetooth module is placed on the development board to enable easy communication between mobile applications and the FPGA. This module communicates with the FPGA chip via Universal Asynchronous Receiver Transmitter (UART) communication protocol. The oscillator on the development board operates at 50 MHz Bluetooth supports UART protocol communication utilizing a range of baud rates, from 1200 to 115200 baud and in this application, the baud rate was chosen 115200 baud. In the VHDL code, a generic is used to determine how many clock cycles there are in each bit by using the code: (Main Frequency) / (UART Baud Rate). The VHDL implementation of UART receiver is shown in Fig. 14.

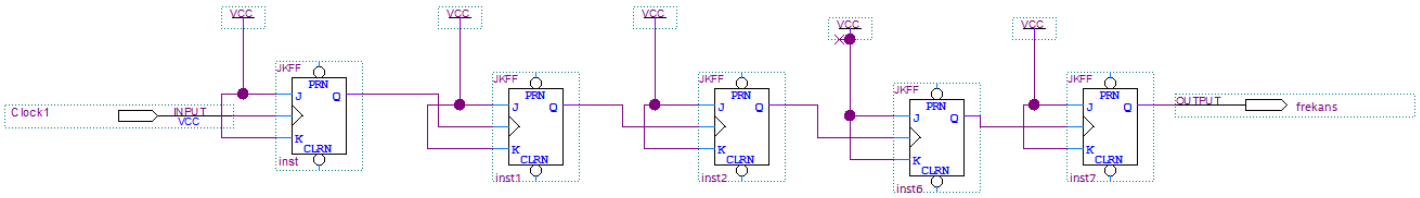


Figure 10. Frequency Divider (f clock /5) bdf file

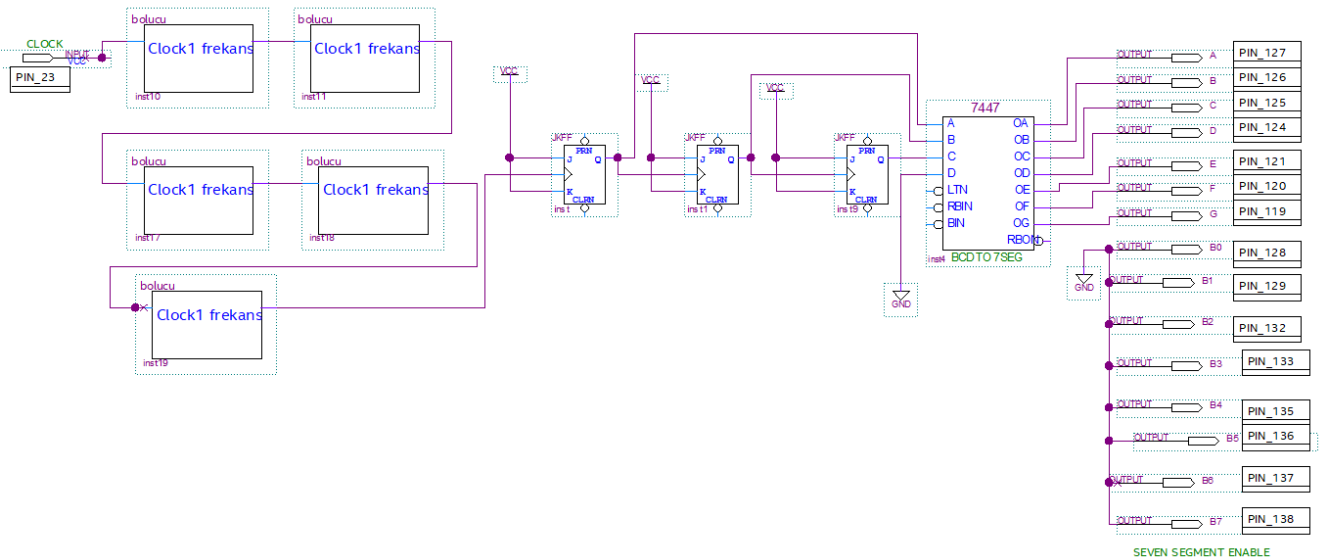


Figure 11. 3-bit down counter bdf file

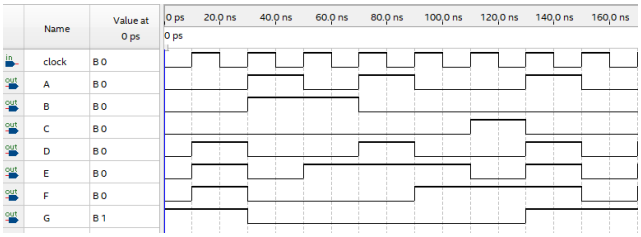


Figure 12. 3-bit down counter wave chart

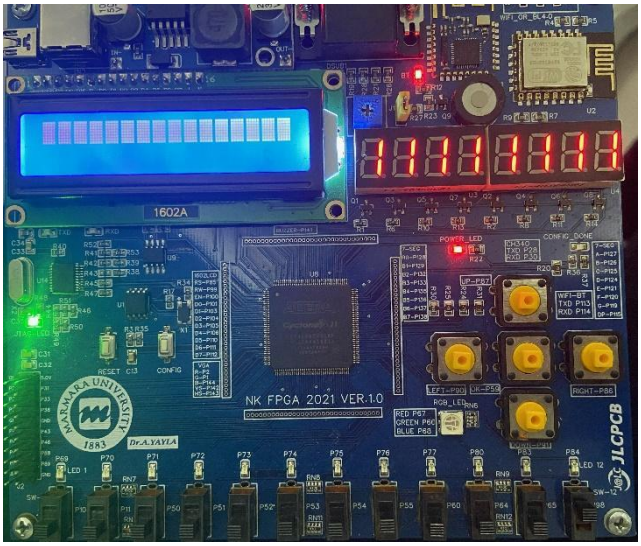


Figure 13. 3-bit down counter 7 Segment Display Result

In this study, an application was developed to display the binary equivalent of the data in the ASCII table on LEDs that we send from devices (tablet or phone) running on the Android operating system. Additionally, in this application, the RGB LED on the development board is set to light up in different colors for a few values. For example, when the value 1 is sent, it turns red, when the value 2 is sent, it turns blue, and when the value 3 is sent, it turns green. When a value outside of these specified values is encountered, the LED displays white, which is a combination of the three primary colors at equal intensities. In Fig. 15, the screenshot of the application is shown for the value G.

```
library ieee;
use ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;
entity UART_RX is
  generic (
    CLKS_PER_BIT : integer := 434     -- 50.000.000/115200=434 Baudrate için
    );
  port (
    rst         : in  std_logic;--reset pin 25
    i_Clk       : in  std_logic;--clock giriş 50 MHZ pin 23
    i_RX_Serial : in  std_logic; -- Uart rX data pin 114
    o_RX_DV     : out std_logic; -- uart data geçerli pin 28 led
    o_RX_Byte   : out std_logic_vector(7 downto 0);
    r_LED_Pin1  : out std_logic;---pin 66 green
    r_LED_Pin2  : out std_logic; ---pin 67 red
    anode : out STD_LOGIC_VECTOR (7 downto 0);
    cathodes : out STD_LOGIC_VECTOR (7 downto 0)
    );
end UART_RX;
architecture rtl of UART_RX is
  type t_SM_Main is (s_Idle, s_RX_Start_Bit, s_RX_Data_Bits,s_RX_Stop_Bit, s_Cleanup);
  signal r_SM_Main : t_SM_Main := s_Idle;
  signal r_RX_Data_R : std_logic := '0';
  signal r_RX_Data   : std_logic := '0';
  signal r_Clk_Count : integer range 0 to CLKS_PER_BIT-1 := 0;
  signal r_Bit_Index : integer range 0 to 7 := 0; -- Toplam 8 bit
  signal r_RX_Byte   : std_logic_vector(7 downto 0) := (others => '0');
  signal r_RX_DV     : std_logic := '0';
begin
  p_SAMPLE : process (i_Clk)
  begin
    if rising_edge(i_Clk) then
      r_RX_Data_R <= i_RX_Serial;
      r_RX_Data   <= r_RX_Data_R;
    end if;
  end process p_SAMPLE;
```

Figure 14. VHDL file for UART application

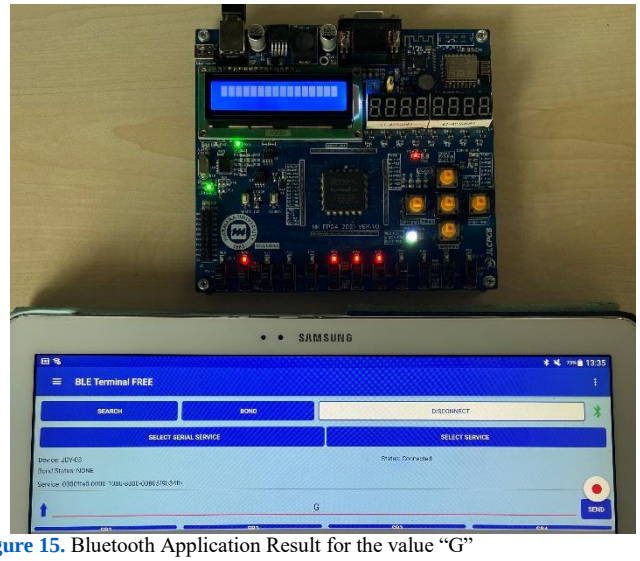


Figure 15. Bluetooth Application Result for the value "G"

5. DISCUSSIONS AND RESULTS

Without the need for additional wireless components, users may quickly and affordably develop and test design solutions for IoT applications with the help of the suggested FPGA evaluation board. Table II contains the table that displays the cost of this board. Additionally, this FPGA development board is approximately 50% below the price of other boards available on the market [21].

The integration of an FPGA development board with internal modules for Bluetooth and Wi-Fi can prove to be especially helpful in fields like defense, aerospace, automotive, medical devices, and smart city infrastructure that demand high-performance hardware solutions and wireless communication. Since internal modules are usually pre-tested and integrated, their usage may be simple. In difficult environments, wireless communication is very beneficial.

TABLE II
COMPONENT PRICES USED IN FPGA DEVELOPMENT BOARD

Component	Quantity	Unit Price (Dollars)	Total Price (Dollars)
Altera Cyclone IV EP4CE6E22C8N	1	16	16
PIC16F45	1	0.8	0.8
LCD	1	0.8	0.8
Bluetooth Module	1	0.6	0.6
ESP 12F Wi-Fi Module	1	0.8	0.8
7 Segment Display	2	0.2	0.4
Switches	12	1	12
Power Module	1	0.5	0.5
VGA Socket	1	0.2	0.2
SPI Flash and EEPROM	1	1	1
Other Materials (Led, resistor, buzzer, transistor, etc.)	1	2	2
PCB	1	2	2
	Total		**37.1**

6. CONCLUSION

In this study, FPGA development board with the necessary hardware components has been designed in order to implement the real-time implementation of fundamental digital applications and designs in the field of engineering. EasyEDA program has been used to design the PCB for the FPGA development board. The development board is equipped with Bluetooth and Wi-Fi modules to offer a wider range of application development areas such as mobile, robotics, smart home systems, and remote monitoring and control devices. FPGA development board has been tested using Intel® Quartus® Prime Lite Edition software for sample digital design and Bluetooth applications that have been coded in VHDL language. Testing of sample digital system design projects was initially carried out in a simulation environment.

After the successful execution of simulation tests, the necessary pin assignments for inputs and outputs have been done, and subsequently, FPGA chip has been programmed via JTAG interface. As a result, it was observed that sample digital system design projects and the Bluetooth project worked successfully on the FPGA development board.

With the FPGA development board presented in this study, a cost-effective FPGA development board that can be used in basic engineering education fundamental applications as an alternative to the FPGA development boards procured from abroad at high expenses has been successfully implemented.

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