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-RESEARCH ARTICLE-

The impact transconductance parameter and threshold voltage of MOSFET's in static characteristics of CMOS inverter

Milaim Zabeli[1], Nebi Caka[1], Myzafere Limani[1], Qamil Kabashi[1*]

[1]Faculty of Electrical and Computer Engineering, University of Prishtina, Prishtina, Kosovo

Abstract

The objective of this paper is to research the impact of electrical and physical parameters that characterize the complementary MOSFET transistors (NMOS and PMOS transistors) in the CMOS inverter for static mode of operation. In addition to this, the paper also aims at exploring the directives that are to be followed during the design phase of the CMOS inverters that enable designers to design the CMOS inverters with the best possible performance, depending on operation conditions. The CMOS inverter designed with the best possible features also enables the designing of the CMOS logic circuits with the best possible performance, according to the operation conditions and designers' requirements.

Keywords:

CMOS inverter, threshold voltage, voltage critical value, noise margins, transconductance parameter.

Article history:

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Introduction

CMOS logic circuits represent the family of logic circuits which are the most popular technology for the implementation of digital circuits, or digital systems. The small dimensions, low power of dissipation and ease of fabrication enable extremely high levels of integration (or circuits packing densities) in digital systems (Lundager, Zeinali, Tohidi, Madsen, & Moradi, 2016; Pal, 2015; Plummer, Deal, & Griffin, 2009; Zant, 2014; Salman & Friedman, 2012).

By noise margins, CMOS technology is the dominant of all the IC technologies available for digital circuits design. The fundamental circuit of CMOS logic circuit is the CMOS inverter. Electrical and physical parameters that characterize the complementary MOS transistors (or

* *Corresponding Author: Qamil Kabashi, e-mail: qamil.kabashi@uni-pr.edu*

complementary MOSFET transistors) determine the behavior of CMOS inverter, as for static conditions of operation, as well as dynamic conditions of operation (Kang & Leblebici, 2016; Sedra & Smith, 2015; Caka, Zabeli, Limani, & Kabashi, 2010; Karl, et al., 2013).

The CMOS inverter consists of two complementary MOS transistors (of an enhancement-type NMOS transistor and an enhancement-type PMOS transistor, because the enhancement-type of MOSFETs have high performance on depletion- type of MOSFETs), interconnected as in Figure 1 (Kang & Leblebici, 2016; Taur & Ning, 2013).

The NMOS transistor is called pull-down transistor, while the PMOS transistor is called pull-up transistor (Rani & Latha, 2016). Complementary MOS transistors in the CMOS inverter operates in complementary mode depending on voltage level applied to the input terminal (to the gates of MOS transistors). In the CMOS inverter, the contribution of both MOS transistors is equal to the circuit operation characteristics, therefore both transistors are considered as driver transistors. By circuit topology for input high voltage (high level), the NMOS transistor drives (pulls down) the output node while the PMOS transistor acts as the load (nonlinear resistor), and for input low voltage (low level) the PMOS transistor drives (pulls up) the output node while the NMOS acts as load (Kang & Leblebici, 2016; Sedra & Smith, 2015; Baker, 2010).

It's very important that the CMOS inverter has the static power of dissipation nearly zero, when the subthreshold conductions and leakage currents are neglected (Sedra & Smith, 2015; Baker, 2010; Weste & Harris, 2011; Zhang, Huang, Zhang, Li, & Yoshihara, 2013; Uddin, Nordin, Reaz, & Bhuiyan, 2013).

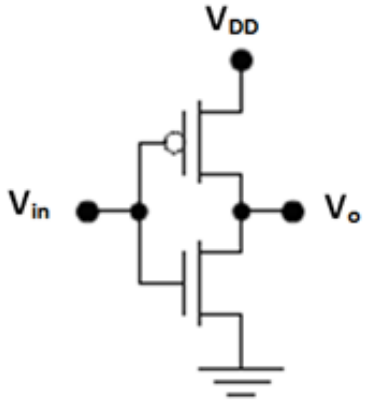

Figure 1. The structure of the CMOS inverter which contains two complementary enhancement-type MOS transistors.

The role of the complementary MOSFET (NMOS and PMOS) transistors parameters in characteristic properties of the CMOS inverters

The behavior of the CMOS inverter for static conditions of operation is described by the voltage transfer characteristic (VTC), and for dynamic operation conditions is described by the time response during switching conductions (Kang & Leblebici, 2016; Sedra & Smith, 2015). The typical VTC of the CMOS inverter is shown as in Figure 2.

In the CMOS inverter, the NMOS transistor and PMOS transistor can be treated as a switch which operates in complementary mode (Baker, 2010).

For construction of the VTC of the CMOS inverter, five different combinations of operation modes of the NMOS and PMOS transistors should be examined, which are the results of the various

ratios of the input voltage levels and the output voltage levels. Operation modes of complementary MOS transistors within particular regions of the VTC are presented in Table 1.

The characteristic properties that characterize the VTC are some voltage critical values at the input and output terminal of the CMOS inverter, as: V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_{th} (Kang & Leblebici, 2016; Sedra & Smith, 2015).

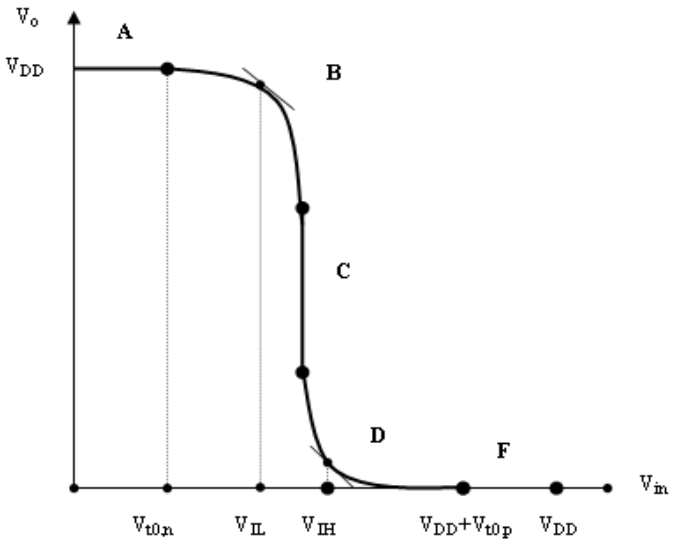

Figure 2. The typical VTC of the CMOS inverter.

Table 1. Operation modes of complementary MOS transistors (NMOS and PMOS transistors)

Region	***V_{in}***	***Vo***	***NMOS***	***PMOS***
A	$< V_{to,n}$	V_{OH}	cut-off	Linear
B	V_{IL}	$\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturatio
D	V_{IH}	$\approx V_{OL}$	linear	n
E	$>$	V_{OL}	linear	saturatio
	$(V_{DD}+V_{to,p})$			n
				cut-off

V_{OH} – output high voltage when output level is a logic "1" (high logic level),
V_{OL} – output low voltage when output level is a logic "0" (low logic level),
V_{IL} – maximum input voltage which can be interpreted as logic "0",
V_{IH} – minimum input voltage which can be interpreted as logic "1".

The voltage critical values at input and output of the CMOS inverter are determined by using combinations of operation regions (operation modes) of the NMOS transistor and the PMOS transistor, depending on the level of the output voltage values relative to the voltage values at the input of the CMOS inverter.

The critical value of output voltage V_{OH} can be calculated by using the A region of VTC's, when the NMOS transistor operates in the cut-off mode, while the PMOS transistor operates in the linear mode, and after calculation will have voltage level of:

$$V_{OH} = V_{DD} \tag{1}$$

when

V_{DD} – power supply voltage (source voltage).

By using the B region of the VTC, the definition for V_{IL} critical value (the smaller of the two input voltage value at which the slope of the VTC becomes $dV_o/dV_{in} = -1$) and the operation modes of complementary MOS transistors according to Table 1 (the NMOS transistor operates in saturation mode, while the PMOS transistors operates linear mode) it can be obtained the expressions for the critical input voltage and the critical output voltage, as:

$$V_{IL} = \frac{2V_o - |V_{to,p}| - V_{DD} + k_r V_{to,n}}{1 + k_r} \tag{2}$$

$$V_o = (V_{in} - V_{t0,p}) + \sqrt{(V_{in} - V_{DD} - V_{t0,p})^2 - k_r (V_{in} - V_{t0,n})^2} \tag{3}$$

when

$V_{t0,n}$ – the threshold voltage of the NMOS transistor,
$V_{t0,p}$ – the threshold voltage of the PMOS transistor,
k_r – the transconductance parameters ratio of the NMOS and the PMOS transistors,
V_{in} – input voltage.

$$k_r = \frac{k_n}{k_p} = \frac{k_n^{'}(W/L)_n}{k_p^{'}(W/L)_p} \tag{4}$$

k_n – transconductance parameter of the NMOS transistor,
k_p – tranconductance parameter of the PMOS transistor,
$k_n^{'}$ - process transconductance parameter of the NMOS transistor,
$k_p^{'}$ - process transconductance parameter of the PMOS transistor,
W – channel width of the MOS transistor,
L – channel length of the MOS transistor,

whereas indexes *n* and *p* indicate the NMOS and PMOS transistor.

The body effect of NMOS and PMOS transistor is not present in the CMOS inverter, because V_{SB} of both transistors is zero. This will have to be taken into consideration in other types of MOS inverters, as in NMOS inverter, when it will influence the threshold voltage of NMOS and PMOS transistors, as well as the VTC shape of inverters.

Also, by using the definition for obtaining the expression for input voltage critical value V_{IH} (the larger of the two input voltage values at which the slope of the VTC becomes $dV_o/dV_{in} = -1$), and by using D region in VTC of CMOS inverter, and operation modes of the NMOS, and the PMOS transistors according to Table 1, we can obtain the expressions for the critical voltage value V_{IH} and the output voltage V_o, as:

$$V_{IH} = \frac{V_{DD} + V_{to,p} + k_r\left(2V_o + V_{to,n}\right)}{1 + k_r} \quad (5)$$

$$V_o = (V_{in} - V_{t0,n}) - \sqrt{(V_{in} - V_{t0,n})^2 - 1/k_r (V_{in} - V_{DD} - V_{t0,p})^2} \quad (6)$$

In the CMOS inverter, it is also important to consider an electrical parameter which represents the threshold voltage of the CMOS inverter V_{th}, which is calculated under the condition that $V_o = V_{in}$. For calculation of the threshold voltage of CMOS inverter V_{th}, the C region of VTC is used, where both transistors (NMOS and PMOS devices) operate in saturation mode and will have:

$$V_{th} = \frac{V_{to,n} + \sqrt{\frac{1}{k_r}}\left(V_{DD} + V_{to,p}\right)}{1 + \sqrt{\frac{1}{k_r}}} \quad (7)$$

The low output critical voltage value V_{OL} is calculated using the E region of VTC, when the NMOS transistor operates in linear mode and the PMOS transistor operates in cut-off mode, resulting in:

$$V_{OL} = 0V \quad (8)$$

The critical input and output voltage values are also determinative to the noise margins values which characterize CMOS inverter for two logic levels (NM_L and NM_H) in static condition of operation (steady state). The noise margins for two logic levels are expressed as:

$$NM_L = V_{IL} - V_{OL} \quad (9)$$

$$NM_H = V_{OH} - V_{IH} \quad (10)$$

From the expressions of the input voltage critical values (V_{IL} and V_{IH}) and the output voltage critical values (V_{OL}, V_{OH}) achieved above, impact on these characteristic-voltage values will have: the values of the power supply voltage (source voltage), the values of the threshold voltage of the complementary MOS transistors, as well as the values of transconductance parameters which characterize the complementary MOS transistors.

Relaying on fabrication processes advances of MOS transistors, it is possible that electrical and physical parameters which characterize MOS transistors can be controlled during fabrication process (Lundager, Zeinali, Tohidi, Madsen, & Moradi, 2016; Plummer, Deal, & Griffin, 2009; Kang & Leblebici, 2016). Therefore, we will examine the impact of these parameters on the particular magnitudes that characterize the CMOS inverter and based on them, can be defined the routes which lead to the design of the CMOS inverter with favorable performance according to the operation conditions and digital circuits based on CMOS logic (Lundager, Zeinali, Tohidi, Madsen, & Moradi, 2016; Karl, et al., 2013; Uddin, Nordin, Reaz, & Bhuiyan, 2013; Chang, Liu, Zhang, & Kong, 2016; Zeinali, Madsen, Raghavan, & Moradi, 2015).

Results and Discussion

The dependence of the input voltage critical value V_{IL} on the ratio of MOS transistors tranconductance parameters for two different values of the threshold voltage of NMOS driver transistor, when the value of the PMOS transistor threshold voltage (PMOS can be treated as a load) remains constant, is presented in Figure 3.

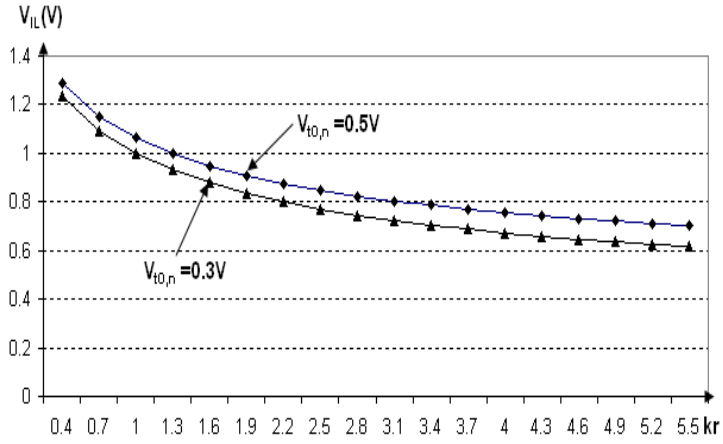

Figure 3. The dependence of input voltage critical value V_{IL} on ratio of MOS transistor transconductance parameters (the ratio of NMOS transconductance parameters on PMOS transconductance parameters) k_r for two different values of NMOS threshold voltage ($V_{t0,n}$), when threshold voltage of PMOS transistor has a constant value of $V_{t0,p}$ = - 0.5 V.

In Figure 4 is shown the dependence of input voltage critical value V_{IL} on the ratio of MOS transistor transconductance parameters for a case when threshold voltage of PMOS transistor has two different values (parametric values), whereas the NMOS transistor threshold voltage remains constant.

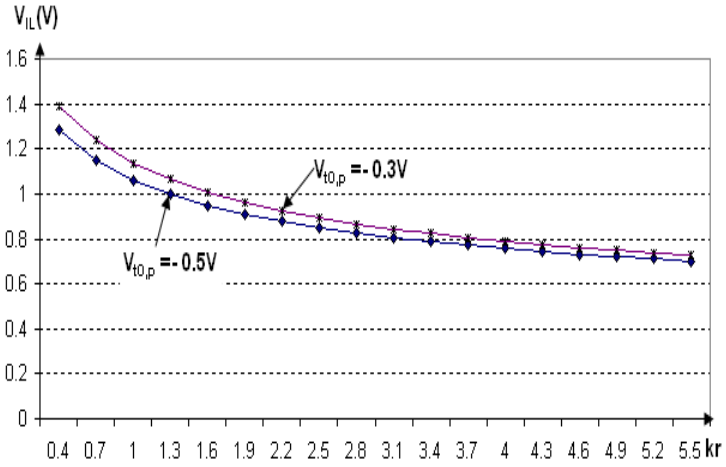

Figure 4. The dependence of input voltage critical value V_{IL} on the ratio of MOS transistor transconductance parameters k_r for two different values of PMOS threshold voltage ($V_{t0,p}$), when threshold voltage of NMOS transistor has constant value of $V_{t0,n}$ = *0.5 V.*

For low critical value of input voltage V_{IL}, the output voltage value is slightly smaller than value of the voltage source, but also it depends on dimensions of the MOS transistors and their threshold voltage values. The impact of MOS transconductance parameters ratio on output voltage value V_o, for some parametric values of complementary MOS transistor threshold voltages, is shown in Figure 5.

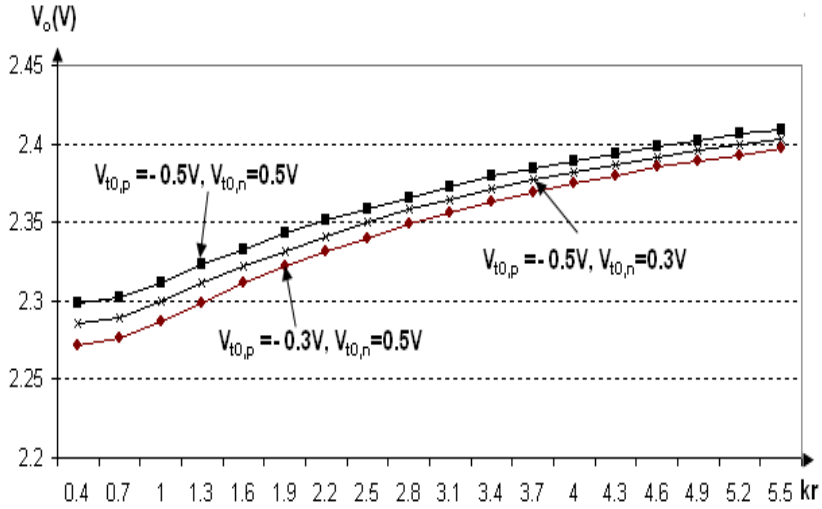

Figure 5. Influence of MOS transistor transconductance parameters ratio *(k_r)* on output voltage value V_o, when the input terminal of CMOS inverter is biased by voltage $V_{in} = V_{IL}$, for several parametric values of complementary MOS transistor threshold voltage.

From the results presented in Figures 3 and 4 for the input voltage critical value V_{IL}, we note that as the higher the value of the transconductance parameter ratio of complementary MOS transistors is, the low critical value of input voltage V_{IL} will decrease. For higher values of the NMOS threshold voltage, the input voltage critical value V_{IL}, will shift to higher values. Also, for the higher value of the absolute value of PMOS transistor threshold voltage, the input voltage critical value V_{IL} will shift to the lower values.

The results presented in Figure 5 show that when the MOS transconductance parameters ratio have higher value, the output voltage value V_o will have higher values, when the input terminal is biased by $V_{in} = V_{IL}$ (or by input low voltage critical value). Also, the impact on output voltage value V_o will have likewise the values of MOS transistors threshold voltage, but this impact is less important compared to the ratio of MOS transistors transconductance parameters. However for lower values of the complementary MOS transconductace parameters ratio, the impact of threshold voltage of complementary MOS transistors will be more significant.

The impact of the MOS transistor transconductance parameters ratio, the MOS transistor threshold voltage values in input voltage critical value V_{IH} (high critical value of input voltage) are shown in Figures 6 and 7.

Presented results show that the higher value of MOS transistors transconductance parameters ratio k_r will decrease the high critical value of input voltage V_{IH}. When the value of the threshold voltage of NMOS transistor is decreased, then the high critical value of input voltage V_{IH} will be decreased and this decreasing will be more prominent for the higher value of the MOS transistor transconductane parameters ratio k_r. Also, when the value of the threshold voltage of PMOS

transistor increases by absolute value, the input critical voltage values V_{IH} will decrease, especially the impact will be more significant for the smaller values of MOS transistors transconductance parameters ratio.

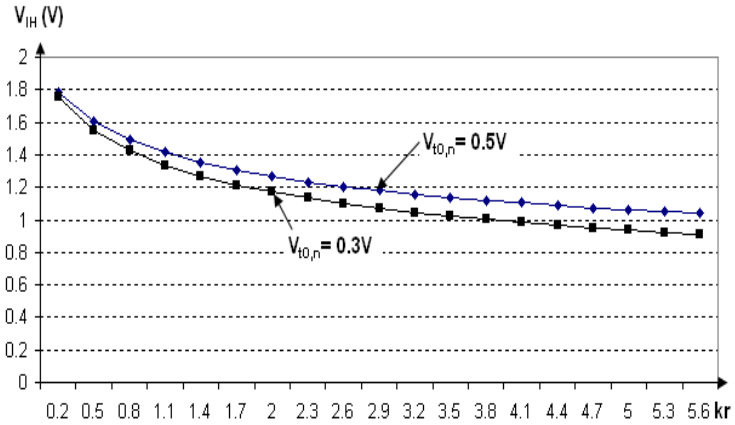

Figure 6. The dependence of the voltage critical value V_{IH} on *MOS* transistors transconductance parameters ratio k_r for two parametric values of NMOS transistor threshold voltage, when PMOS transistor threshold voltage remains constant $V_{t0,p}$ = - 0.5 V.

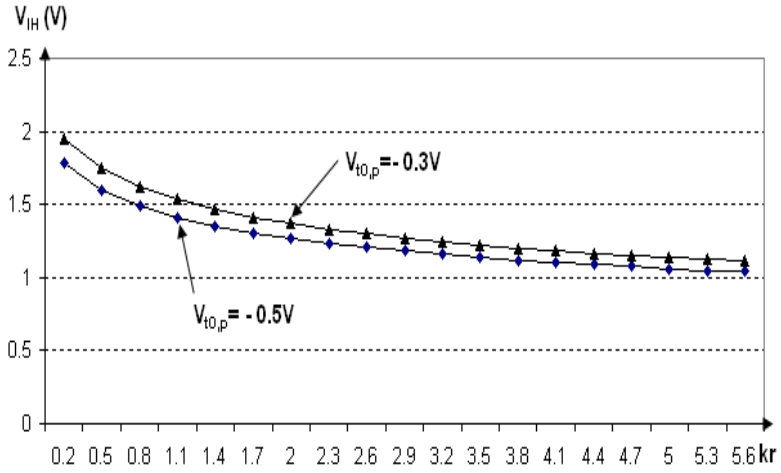

Figure 7. The dependence of voltage critical value V_{IH} on MOS transistors transconductance parameters ratio k_r for two parametric values of PMOS transistor threshold voltage, when NMOS transistor threshold voltage remains constant $V_{t0,n}$ = 0.5 V.

Presented results show that the higher value of MOS transistors transconductance parameters ratio k_r will decrease the high critical value of input voltage V_{IH}. When the value of the threshold voltage of NMOS transistor is decreased, then the high critical value of input voltage V_{IH} will be decreased and this decreasing will be more prominent for the higher value of the MOS transistor transconductane parameters ratio k_r. Also, when the value of the threshold voltage of PMOS transistor increases by absolute value, the input critical voltage values V_{IH} will decrease, especially the impact will be more significant for the smaller values of MOS transistors transconductance parameters ratio.

The MOS transistors transconductance parameters ratio and the values of the MOS transistors threshold voltage will have impact on the CMOS inverter characteristic value which is called the CMOS threshold voltage value (or switching threshold).

In Figures 8 and 9 is shown the impact of the MOS transistors transconductance parameters ratio that constitute CMOS inverter on the CMOS inverter threshold voltage value V_{th} for several parametric values of complementary MOS transistors threshold voltage (NMOS and PMOS threshold voltage).

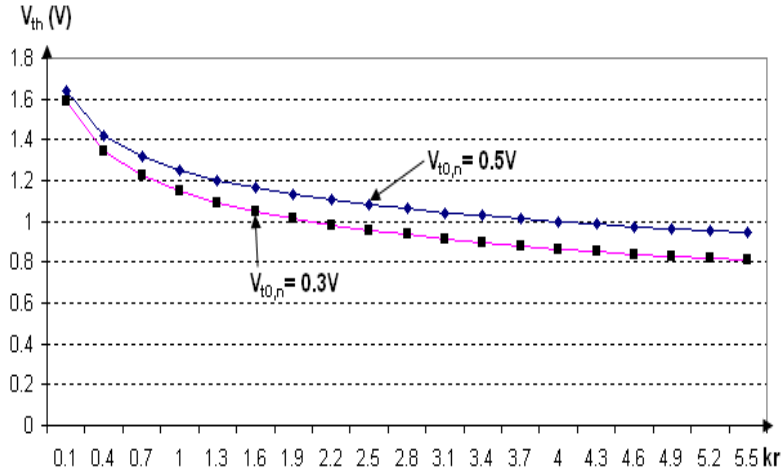

Figure 8. The impact of the transconductance parameters ratio *(k_r)* of MOS transistors (NMOS and PMOS) on value of the CMOS inverter threshold voltage (on value of CMOS inverter switching threshold voltage) for two different values of the NMOS threshold voltage, when $V_{t0,p}$ = - 0.5 V and source voltage V_{DD} = 2.5 V.

Based on the obtained results, it is shown that the higher value of MOS transconductane parameters ratio is, the CMOS threshold voltage value will be decreased, respectively, it will be shifted towards the logical lower value. For higher values of the NMOS threshold voltage, the value of the CMOS threshold voltage V_{th} would increase in value, especially the impact will be more prominent for greater values of the transconductance parameters ratio k_r ($k_n > k_p$). While when the threshold voltage of the PMOS transistor has a higher value by absolute value, the value of the CMOS threshold voltage V_{th} will be decreased, and this decreasing will be more significant when the transconductance parameter ratio k_r has lower values ($k_p < k_n$).

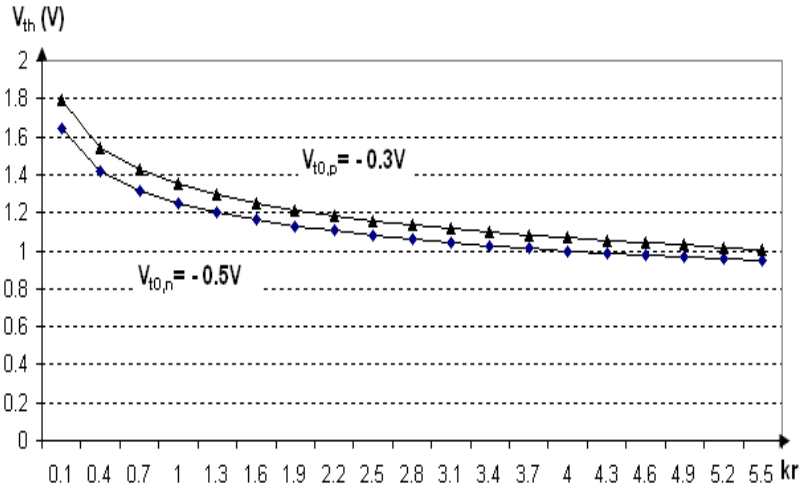

Figure 9. The impact of the transconductance parameters ratio *(k_r)* of MOS transistors (NMOS and PMOS) on value of the CMOS inverter threshold voltage V_{th} *(*on value of CMOS inverter switching threshold voltage) for two different values of the PMOS threshold voltage, when $V_{t0,n}$ = 0.5 V and V_{DD} = 2.5 V.

The immunity of CMOS inverter on unwanted signals is expressed through the noise margins for both logical levels (for low level and for high level). The parameters that characterize the complementary MOS transistors in a CMOS inverter determine the noise margins level for both logical levels. The dependence of noise margins (*NM*) on the complementary MOS transistors transconductance parameters ratio, for several parametric values of MOS transistors threshold voltages in both logic levels are shown in Figures 10 and 11.

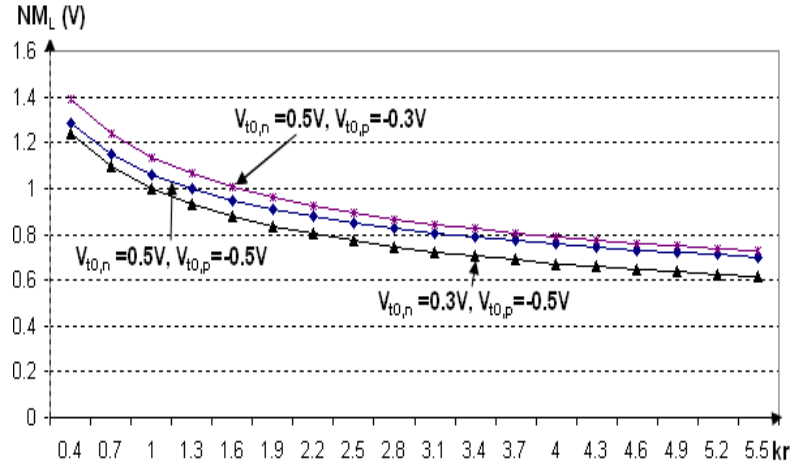

Figure 10. The dependence of the noise margins for low logic level NM_L on complementary MOS transistors transconductance parameters ratio k_r, for three cases of different MOS transistor threshold voltage (NMOS and PMOS transistors), when V_{DD} = 2.5 V.

The results in Figure 10 indicate that the higher values of the MOS transconductance parameters ratio k_r, noise margin for the low level will be lower. For the lower value of the NMOS transistor threshold voltage ($V_{t0,n}$), the level of noise margins NM_L (noise margins for low level) will decrease, resulting in the significant reduction in the band of higher values of the

transconductance parameter ratio k_r. Also, the smaller the PMOS transistor threshold voltage value ($V_{t0,\,p}$) by absolute value, the level of noise margins NM_L will increase, especially in the range of small values of the transconductance parameters ratio k_r.

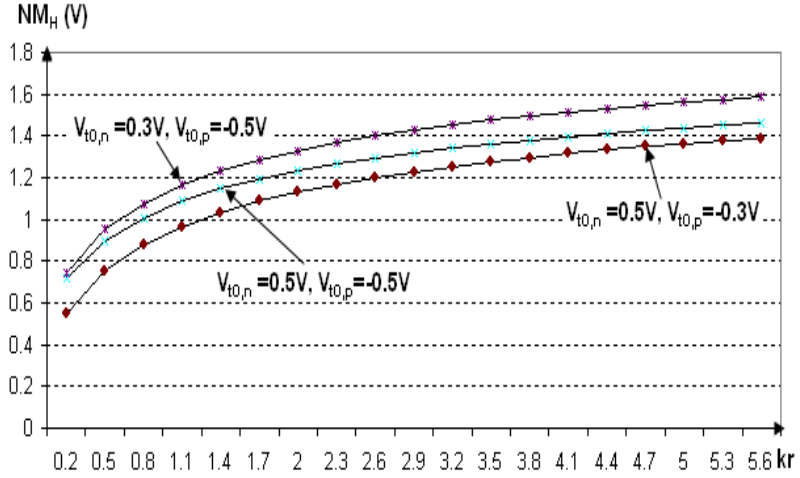

Figure 11. The dependence of the noise margins for high logic level NM_H on complementary MOS transistors transconductance parameters ratio k_r, for three cases of different MOS transistor threshold voltage (NMOS and PMOS transistors), when V_{DD} = 2.5 V.

The level of noise margins NM_H (noise margins for high level) will increase when the MOS transconductance parameter ratio is designed to be higher, Figure 11. For smaller value of NMOS threshold voltage, the noise margin for high level NM_H will increase especially in the range of higher values of the transconductance parameter k_r. While the lower value of PMOS threshold voltage by absolute value ($V_{t0,p}$), the level of noise margins NM_H will decrease, especially with significant impact in the range of low values of the transconductane parameter ratio k_r.

By matching the values of complementary MOS transconductance parameters and values of their threshold voltage, the CMOS inverter can be designed with higher performance, depending on the requirements of designer that dictate operation conditions. For CMOS inverter with matched parameters as: $k_n = k_p$ and $V_{t0,\,n} = |\,V_{t0,\,p}\,|$ will be achieved that the noise margin to be equal to both logic levels and the value of the threshold voltage of the CMOS inverter will be half of voltage source $V_{th} = V_{DD}/2$. The CMOS inverter which possesses these features is called symmetric inverter and it must satisfy the condition:

$$\left(\frac{k_n}{k_p}\right)_{symetric} = 1 \qquad (11)$$

$$\left(\frac{k_n}{k_p}\right) = \frac{\mu_n C_{ox}\left(W/L\right)_n}{\mu_p C_{ox}\left(W/L\right)_p} = \frac{\mu_n\left(W/L\right)_n}{\mu_p\left(W/L\right)_p} \quad \Leftrightarrow \left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$

and although the MOS transistors built by equal length of channel defined by lithographic process, it appears that:

$$\left(W\right)_p \approx 2.5\left(W\right)_n) \qquad (12)$$

The behavior of CMOS inverter is described through the VTC in DC mode of operations (steady state mode). The parameters that characterize the complementary MOS transistors influence in the shape of the VTC. At the design phase of CMOS inverter, the requirements of CMOS inverter behavior are presented, so the task of the designer is to adjust the parameters of the NMOS and PMOS transistors as much as possible, which enable the design of the CMOS inverter with acceptable performance. The impact of NMOS and PMOS transistor parameters in shape of the VTC is shown in Figure 12.

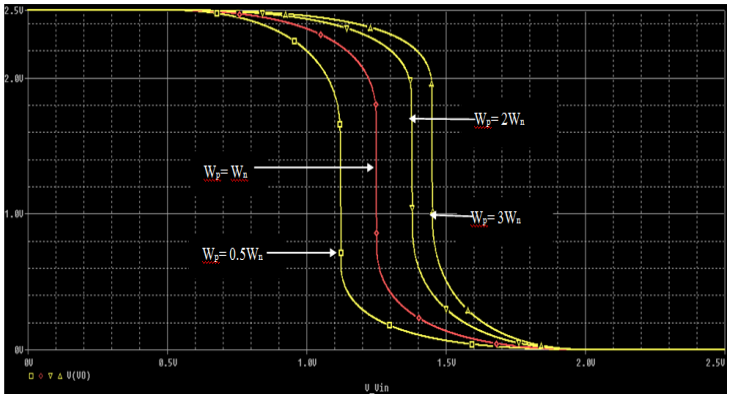

Figure 12. The impact of complementary MOS transistors channel length ratio *(W_n/W_p)* on VTC shape, when $L_n = L_p$, $V_{t0,n} = |V_{t0,p}| = 0.5$ V and $V_{DD} = 2.5$ V.

From the VTC shape presented in Figure 12 we can see the impact of the channel width (respectively the ratio of the transconductance parameter k_r) in the shape of VTC, resulting in displacement of the VTC's left or right, depending on the channels widths ratio, and reflecting in the characteristic values of VTC's.

When the value of NMOS transistor threshold voltage increases, and the PMOS transistor threshold voltage remains unchanged, the VTC of CMOS inverter shall shift to the right from the lower value of the NMOS threshold voltage ($V_{t0.n}$), which is reflected in the voltage critical values, Figure 13.

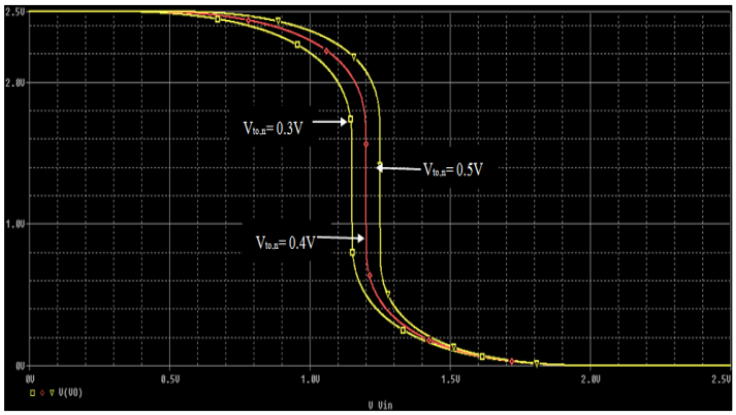

Figure 13. The impact of the NMOS transistor threshold voltage *($V_{t0,n}$)* on VTC shape, when PMOS transistor threshold voltage is $V_{t0,p}$ = - 0.5 V, and transistors have identical dimensions.

In Figure 14 is shown the impact of the PMOS transistor threshold voltage value in VTC shape of CMOS inverter when the NMOS transistor threshold voltage has a fixed value. When the PMOS

transistor threshold voltage has lower value by an absolute value, then the CMOS inverter VTC will shift to the right from the larger value.

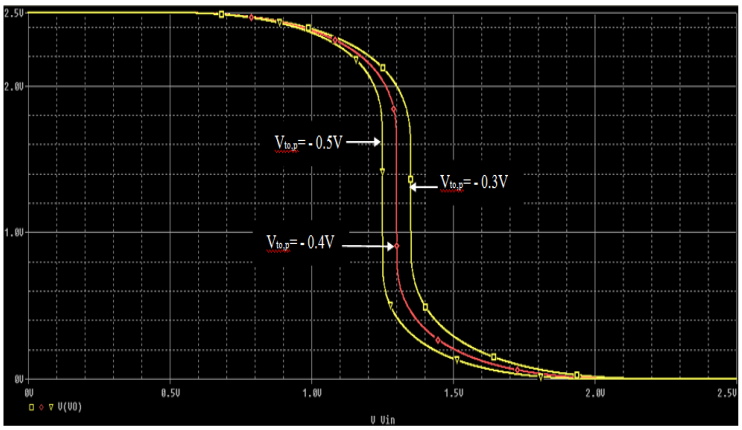

Figure 14. The impact of PMOS transistor threshold voltage *($V_{t0,p}$)* on CMOS inverter VTC shape, when NMOS transistor threshold voltage value is $V_{t0,n}$ = 0.5 V, and transistors have identical dimensions.

According to the shapes of VTC of the CMOS inverter presented in Figure 12-14 the slope of VTC in particular regions is indicted. It's very important that the slope of VTC in region named by C is same in all cases, which differs for other types of MOS inverters.

Conclusions

If during the design phase of the CMOS inverter, the threshold voltage values of complementary MOS transistors (with the threshold voltage of NMOS ($V_{t0,n}$) and PMOS transistor ($V_{t0,p}$)) and the ratio of complementary MOS transistors transconductance parameters (the ratio between transconductance parameters of NMOS transistor (k_n) and PMOS transistor (k_p), $k_r = k_n/k_p$) are controlled, or matched, the CMOS inverter can be designed with high performance as for static conditions of operation, as well as for dynamic conditions of operations, depending on the designer requirements and operating conditions.

As for the output voltage critical values V_{OL} and V_{OH} (or for high and low logic level at output), the transconductance parameter ratio of the complementary CMOS transistors (k_r) and the complementary MOS transistor threshold voltages ($V_{t0.n}$ and $V_{t0,p}$) don't have impact, but their values are determined by zero volt (ground voltage) and source voltage value (V_{DD}).

For the higher values of complementary MOS transistors transconductance parameters ratio (k_r), lower value of the NMOS transistor threshold voltage ($V_{t0,n}$) and higher value by absolute value of the PMOS transistor threshold voltage ($V_{t0.p}$), the input voltage critical value V_{IL} and noise margin for low level NM_L will decrease.

For the higher values of complementary MOS transistors transconductance parameters ratio (k_r), lower value of the NMOS transistor threshold voltage ($V_{t0,n}$) and higher value by absolute value of the PMOS transistor threshold voltage ($V_{t0.p}$), the input voltage critical value V_{IH} will decrease, whereas noise margin for high level NM_H will increase.

As for the output voltage value V_o when $V_{in} = V_{IL}$, for the higher values of complementary MOS transistors transconductance parameters ratio (k_r), lower value of the NMOS transistor threshold voltage ($V_{t0,n}$) and higher.

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