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Research Article

A single-phase solid-state fault current limiter: Simulation and experimental study

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ABSTRACT

Various methods are used to reduce fault currents in fault situations occurring in power systems. In this study, a developed single-phase power electronics-based solid-state fault current limiter is presented. The proposed single-phase solid-state fault current limiter is designed as preliminary prototype of the three-phase low voltage solid-state fault current limiter. The maximum current and voltage capability of the fault current limiter is 16 A and 480 V. This limiter works according to the principle of series and parallel resonance. In normal operation, the current passes through the inductance and capacitor, which are in series resonance. Thus, extra voltage drops and power loss in the system are prevented. In the event of a fault, the limiter switches to parallel resonance, and its impedance increases. Therefore, the fault current is decreased. The developed circuit and control algorithm reduces the first peak of fault current with a rather high percentage by comparison with the fault current without fault current limiter. In addition, the amplitude of current oscillation is decreased, and the current is recovered in a short time because the control algorithm determines the fault start and end time fast. The effect of the limiter is demonstrated with the simulation results in Matlab/Simulink. The simulation results are verified with the application study carried out in the laboratory environment. The fault current reaches up to 58.5 A in case of fault current limiter is not used, whereas the developed fault current limiter suppresses the current to around 9 A. The value of maximum fault current decreases to 15% according to the non-fault current limiter used situation. In the study, detailed application notes of the limiter circuit are shared.

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INTRODUCTION

The increase in energy consumption that occurs with technological developments increases the stress on power systems. Therefore, as a result of excessive currents drawn in fault situations, the thermal stress in the system increases even more. With the integration of renewable energy systems and distributed power systems into power grids, the probability of malfunctions that may occur in the system

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increases. In case of short-circuit faults in power systems, the equipment in the system is damaged due to high current. Therefore, additional cost and power outages appear. For this reason, it is necessary to protect the power systems against environmental effects, to ensure stable operation in case of failure, and to prevent the components in the system from being damaged in case of failure [1,2].

Fault current limiters (FCLs) are developed in order to reduce the high currents drawn in fault situations in power systems. The most basic and simple fault current limiter (FCL) is to use resistors in series on the fault current path. In the limiter consisting of a parallel-connected resistor and a semiconductor switch, while the current passes through the switch in normal operation, the switch opens when a fault occurs, and it allows the current to flow over the resistor. Thus, the fault current decreases [3, 4]. Another example of using series resistors is superconductor applications. The superconducting material placed in series on the main current path shows high resistance against the high current that flows through it and so it limits the current. When the fault situation disappears, the resistance value decreases to its normal value [5,6]. In addition to inserting resistance to the system, inductance is added to limit the fault current. In the event of a fault, a high value of inductance is connected in series to the circuit, and the high fault current is limited. In the method using a parallel switch, the current flows through the switch in normal operation. The switch is opened in the fault event, and therefore the current flows through the inductance [7]. Another commonly used FCL type is the bridge type. There are bridge-type FCL circuits in different topologies [8,9]. The impedance of the transformer is controlled by using a DC reactor, a resistor in series with it, and a semiconductor connected in parallel to the resistor at the output of a diode rectifier on the secondary side of a transformer connected in series to the system [10,11]. Series and parallel type resonance circuits are also used as FCL types. In case of applying series resonance, since the impedance is very low, losses do not occur in normal operation [12]. When the bidirectional switch connected in parallel to the capacitor is activated after the fault begins, the resonance is disturbed, and the fault current is limited by increasing the impedance [13]. In series resonance FCL circuits made by using a full-bridge thyristor rectifier, DC voltage is applied to the inductance through the rectifier in case of failure, and a short circuit is ensured. Thus, series resonance ends, and the capacitor reduces the current by its impedance [14]. There are different types of series resonance circuits in which a part of the inductance is deactivated, and the capacitor is deactivated instead of the inductance in the FCL circuit where the series resonance is disrupted by using a thyristor [15]. In parallel type resonance FCL circuits, parallel resonance is activated in the event of a fault, providing high impedance and limiting the fault current [16,17]. In the FCL circuit where series resonance and parallel resonance are used together, the FCL impedance is increased, and the fault current is limited by ensuring that the series resonance is disrupted by switching while the current passes through the series resonance [18]. In parallel resonance FCL that diode bridge model is applied in, the current flows through DC reactor and diodes in normal operation. In case of fault, the semiconductor switch that is connected in series with the inductance is opened, and therefore the inductance becomes disabled. As a result, the fault current starts to flow through the parallel resonance circuit, and the fault current is limited by the high impedance effect [19].

In this study, the simulation and details of the laboratory prototype of the developed single-phase solid-state fault current limiter that is used in the power grid to suppress the phase-to-ground fault current are presented. The presented circuit is the single-phase preliminary study of the three-phase FCL system that will be developed later. It consists of series and parallel resonance circuits. During the normal operation, the main current flows through the series resonance. Thus, extra voltage drops do not occur on the components of the inductor and capacitor. When the fault occurs, the switch that is connected in parallel to the capacitor is closed, and the series resonance is corrupted. Thus, the total impedance of FCL gets higher with parallel resonance and it suppresses the fault current.

Fault current limiting performance of the developed solid-state FCL is investigated with simulations and experimental short-circuit tests. The proposed single-phase solid-state FCL is designed as preliminary prototype of the three-phase low voltage solid-state FCL. The maximum current and voltage capability of the FCL is 16 A and 480 V. It has a simple structure and can effectively limit fault current in phase-to-ground fault. FCL does not affect the normal operation of the system and works stably during the fault. It can protect all system equipment from high fault currents and can work in harmony with circuit breakers in the power systems. It is an advantageous topology in terms of its probable cost and economic benefit potential. The developed FCL circuit decreases the 58.5 A fault current without FCL to 9 A with rate of %85.

The main knowledge about the topology and the control algorithm, detail of the prototype, the simulation and experimental study, discussion and conclusions are given in sections 2, section 3, section 4, section 5 and section 6, respectively. The results that are verified with simulation and experiment are presented. The results show the effectiveness of the developed system.

TOPOLOGY AND CONTROL OF THE DEVELOPED SYSTEM

The topology of the developed system is seen in Figure 1. The solid-state fault current limiter circuit is a type of series-parallel resonance. In the normal operation, the FCL operates as a series resonance circuit. The impedances of L_{sp} and C_{sr} components are equal each other as given in (1),

$$j\omega L_{sp} = \frac{1}{j\omega C_{sr}} \tag{1}$$

where ω, L_{sp} and C_{sr} defines angular frequency of the grid, inductor and capacitor of FCL, respectively. There is a series resonance between them, and the sum of impedances is zero. Therefore, the line current flows over these components. It provides low voltage drop and low power loss on the FCL circuit. The upper side of the FCL circuit is open-circuit, and current does not flow, theoretically. When the short-circuit fault occurs in the system, solid-state switches are switched depending on the control algorithm to suppress the line current during the fault exists. Thus, the impedance of C_{sr} is added or removed from the circuit. When the C_{sr} is switched off, FCL starts to operate as a parallel resonance to suppress the line current with increasing the total impedance. As seen in Figure 1, it is assumed that the short circuit fault occurs at the connection point of the load. The control algorithm switches the solid-states (S_1 and S_2) in the FCL circuit.

When the switches are closed, series resonance is disturbed and parallel resonance occurs with C_{pr}, R_{pr} and L_{sp}. The parallel resonance circuit provides high impedance and thus, fault current decreases. The impedance equation of the FCL in parallel resonance is given in.

$$Z_{FCL} = \frac{j\omega L_{sp} - \omega^2 L_{sp} C_{pr} R_{pr}}{1 - \omega^2 L_{sp} C_{pr} + j\omega C_{pr} R_{pr}} \tag{2}$$

The detailed block diagram of the control block that is seen Figure 1 is given in Figure 2. In the algorithm, voltage at the point of common coupling (v_{pcc}), load bus voltage (v_{Load}), line current (i_L) and load current (i_{Load}) are used to suppress high fault current. The voltage and current of the load and grid side of FCL are measured and compared to control the switches. Firstly, line and load current waveforms are taken

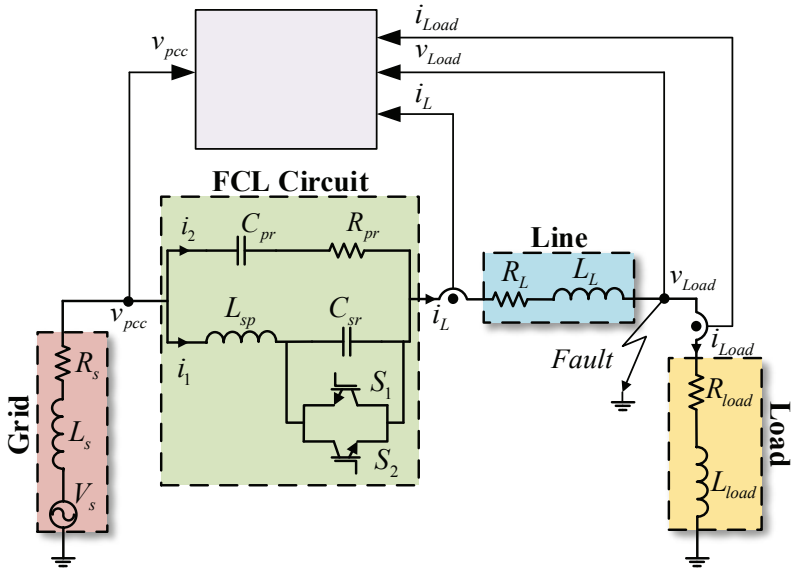

Figure 1. Topology of the system.

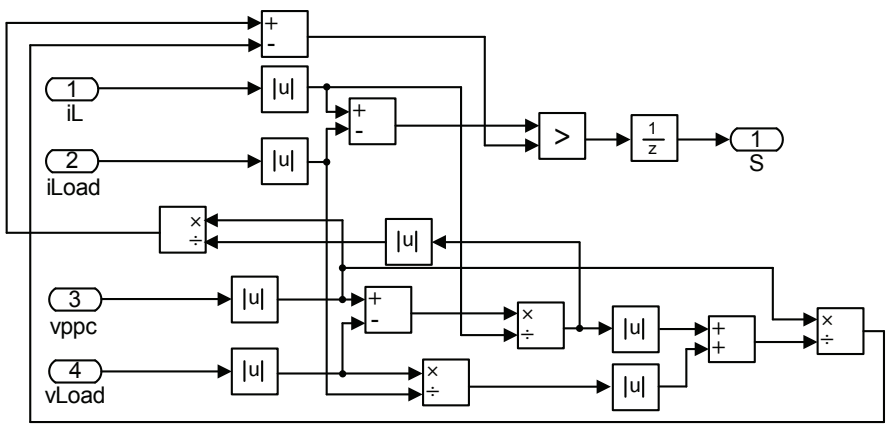

Figure 2. The proposed control algorithm.

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Algorithm 1:
1  Read iL, iLoad, vpcc, vLoad
2  Get absolute value of iL, iLoad, vpcc, vLoad
3  x=abs(vpcc)-abs(vLoad)
4  y=x/abs(iL)
5  z=abs(y)+abs(abs(vLoad)/abs(iLoad))
6  w=abs(vpcc)/z
7  a=abs(vpcc)/abs(y)
8  b= a-abs(w)
9  c=abs(iL)-abs(iLoad)
10 if c>b
11 S=1
12 Else
13 S=0
```

Figure 3. Pseudocode of the control algorithm.

to get their absolute values. PCC and load voltage that are transformed to absolute forms are utilized to calculate limiter and load impedance. The impedances are calculated by dividing voltages by currents. Instantaneous impedances of limiter and whole system are compared to identify the fault status. In a fault situation, this comparison has zero output and so it has a rather lower value than the difference of line and load currents. This condition provides to being turned on semiconductor switches and inserted high impedance of FCL to the system. In non-fault operation, its output keeps the switches at cut-off mode permanently. Thus, control algorithm produces the switching signal by continuously repeating of this process.

The Pseudocode of the control algorithm of the FCL circuit is seen in Figure 3. The anti-parallel connected IGBTs in the FCL circuit are switched depending on the control algorithm. It aims to detect the beginning moment of the fault rapidly, and so FCL begins to operate limiting the fault current. Additionally, it purposes to shorten the recovery time when the fault ends.

STUDY OF LABORATORY PROTOTYPE

The schematic of the prototype circuit is seen Figure 4. In the input of the system, a variable transformer is utilized, and a contactor is placed after the transformer to connect or disconnect the system to the grid. If any unexpected fault occurs in the system, protection algorithm disconnects the system by the contactor. On the point of common coupling (*PCC*), a LV 25-P voltage sensor is used to sense the *PCC* voltage (v_{pcc}). Another LV 25-P is utilized on the output of the system to measure the load voltage. Two LA 25-NP current sensors are utilized to sense the line and load current. Four sensors are used to sense the electrical signals. In the FCL circuit, two IXGH48N60C3 IGBTs are used to switch the C_{sr}. They are connected anti-parallel each other to pass the current for two ways. The IGBT has no internal anti-parallel diode, thus two ways current can be controlled. They are switched by TLP350 driver integrated circuit (IC). R_L and L_L components are used as line conducting while an inductor and a resistor are used as a load at the output.

The parameters of the components in the system are given in Table 1. In the application circuit, the components are connected to each other by aluminum sheets, and the resistance values of these sheets are modeled as resistance in the simulation to obtain more accurate results. The resistance value of aluminum sheets (R_{al}) that are utilized between the components are used as 0.26 Ω depending on the resistance measurement.

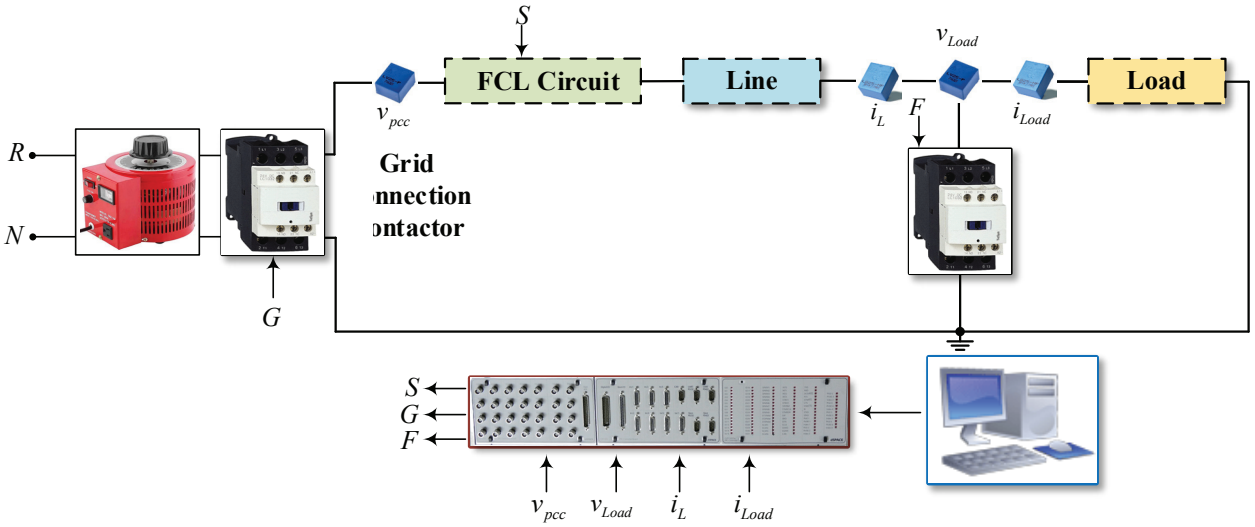

Figure 4. Schematic of prototype circuit.

Table 1. Parameters of the circuit components

Variable	Value
L_{sp}	101 mH, 3.5 A
L_L	10 mH, 3.5 A
L_{load}	100 mH, 5 A
R_{pr}	21 Ω, 1.5 kW
R_L	2 Ω, 500 W
R_{load}	50 Ω, 2500 W
R_{al}	0.26 Ω
C_{pr}	100 µF, 330 V
C_{sr}	100 µF, 480 V
S_1, S_2	IXGH48N60C3 600 V, 48 A
Current sensor	LA 25-NP
Voltage sensor	LV 25-P

The control signals of IGBTs are generated by a dSpace DS1103 controller card. The card is programmed by Simulink [20]. The Simulink blocks of the control algorithm are seen in Figure 5. In the algorithm, *OPERATION DURATION* block that is highlighted orange color determines the operation time. The system works for 4 seconds. In order to test the performance of FCL circuit, phase-to-ground fault is activated by *FAULT DURATION* block. The fault occurs for 130 ms from 3 to 3.13 seconds as seen from the red highlighted block. As the setup is a laboratory prototype, *CURRENT PROTECTION* is added into the control algorithm. The blue highlighted block stops the system by closing the grid contactor until the system is restarted if the line current reaches 15 A. The voltages and currents that are used in the algorithm are injected into the algorithm by *SENSOR OUTPUTS* block. It converts the analog signals to digital signals in the microprocessor. The *SENSOR GAINS* block includes gains that are used to convert the measured signals into real values because the measured signals are scaled between -10 and 10 by analog-to-digital converter (ADC). The blocks named DS1103BIT_OUT_GX have digital outputs. The outputs are connected to solid-state switches and contactors. The output signals of the sensors are transmitted to DS1103 through CLP1103 connector panel via ADC BNC connector.

Laboratory prototype of the developed system is seen in Figure 6. The components are connected each other by aluminum sheets. Because the circuit includes big and heavy components such as inductors and capacitors, this type of structure is preferred. The input voltage of the system is adjusted with variable transformer. The setup is first tried for lower input voltage levels. The experimental results have been taken for 220 V_{rms} phase voltage. The system is connected to the grid by grid contactor, and it is controlled with user through Controller Desk that is the software of DS1103. The input and output signals of the control algorithm are supplied by CLP1103. It has BNC connector for ADC channels. They are used for connection of measured voltage and current signals. The signals for contactors and switching devices are provided from the IO pins. As the switching signals are not produced with pulse width modulation, PWM module is not used. Another contactor used in the system is the fault contactor. It makes a short-circuit between phase and ground.

IXGH48N60C3 model IGBTs are used in the FCL, and TLP350 driver IC gives the PWM signal to the IGBT. The schematic of the driver is given in Figure 7. It has 2.5A maximum output current, and 2 mA maximum input current. Its supply voltage is between 15 V and 30 V. There is an isolation between input and output with light-emitting diode, and the output signal is the same with input signal [21]. The power of TLP350 is provided via linear power source

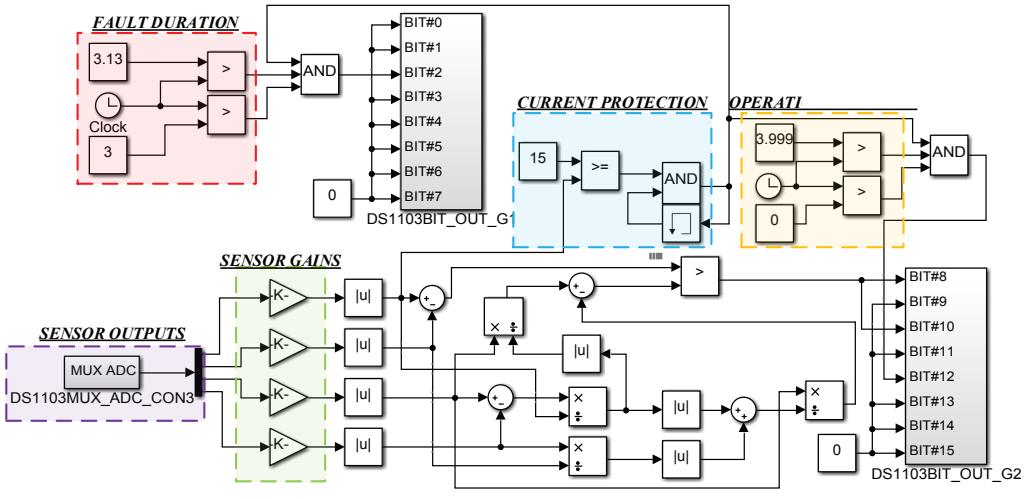

Figure 5. Simulink control algorithm of the prototype circuit for DS1103.

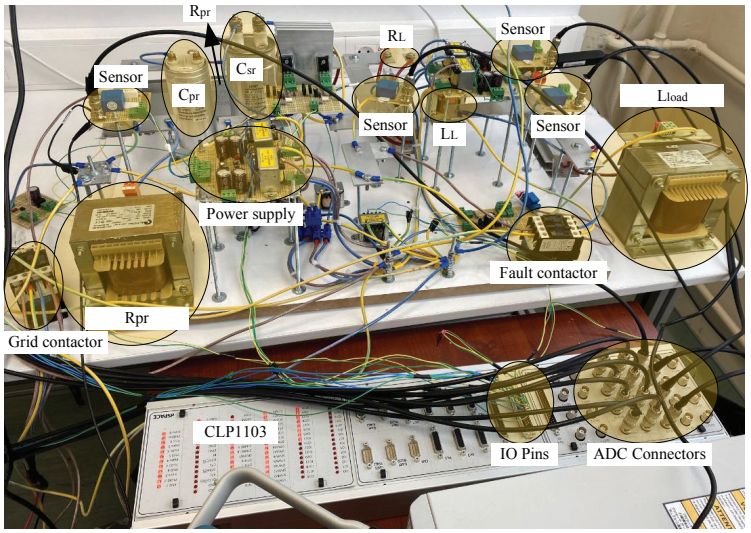

Figure 6. Laboratory prototype of the system .

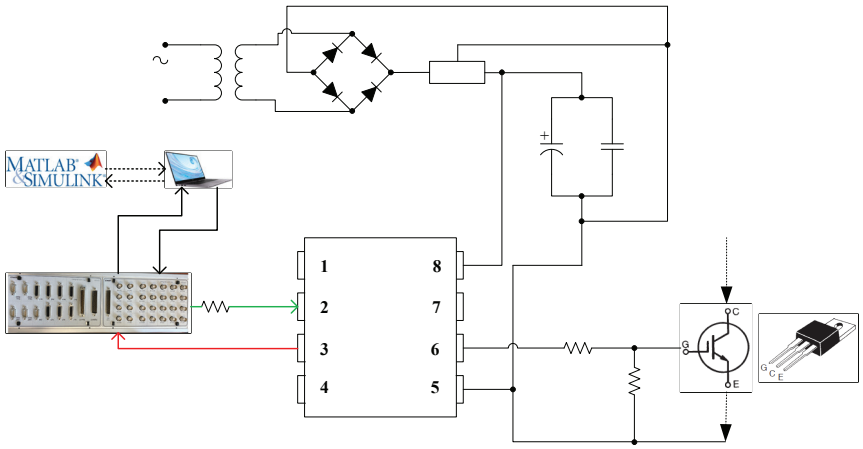

Figure 7. IGBT driver circuit.

made with 220 V / 15 V transformer, full-bridge rectifier and 7815 linear voltage regulator. The signal comes from DS1103 via CLP1103 connection box as seen in Figure 7. The output of TLP350 is a signal that is applied to IGBT.

There are two current transducers using the hall effect in the system as seen in Figure 4. The current is sensed by LA 25-NP current transducer. It has galvanic isolation between the primary and secondary circuit. It allows five different connection features to change turn ratio. Two types of connections for LA 25-NP that provide 2/1000 (left) and 5/1000 (right) turn ratio are seen in Figure 8, respectively. The output of the transducer is current, and it is converted to voltage signal by a resistor. The transducer that is configured with 2/1000 turn ratio converts 12 A to 24 mA at the output. The output current flows through the resistor. With using a 270 Ω resistor, the output voltage becomes 6.48 V. It can be calculated for other ratio connections [22]. The voltage signal is transmitted to ADC channel of control card through CLP1103.

The voltages in the system are sensed by LV 25-P voltage transducer that uses hall effect like LA 25-NP. It measures up to 500 V. Similar to the current transducer, the output of the voltage transducer is current. For the input current of 10 mA, the output current is 25 mA because it has 2500:1000 turn ratio. As seen in Figure 9, the output current is converted to voltage signal by a resistor, and the input voltage is converted to current by a resistor [23]. The nominal PCC voltage is 220 V, so the input current of voltage sensor is 6.67 mA because of 33 kΩ resistor. The output current is 16.67 mA by 2500:1000 turn ratio. The resistor of 330 Ω at the output provides 5.5 V by 16.67 mA current. Both transducers are supplied from +15/-15 V linear power supply that is given in Figure 10. Two linear voltage regulators, 7815 and 7915,

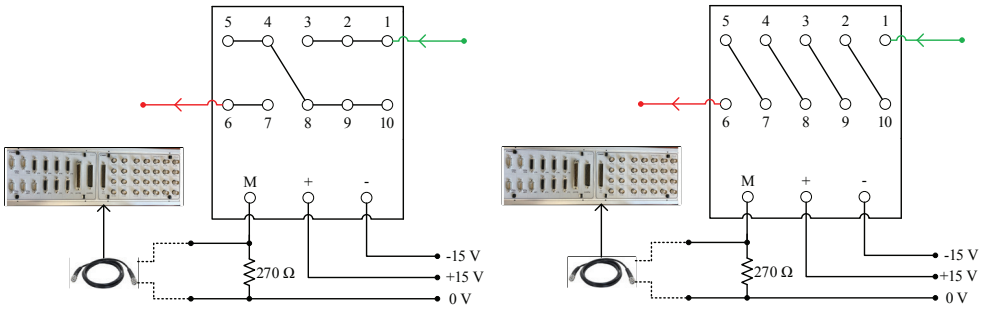

Figure 8. Schematic of the current sensor connection (left : 2/1000 turn ratio, right : 5/1000 turn ratio).

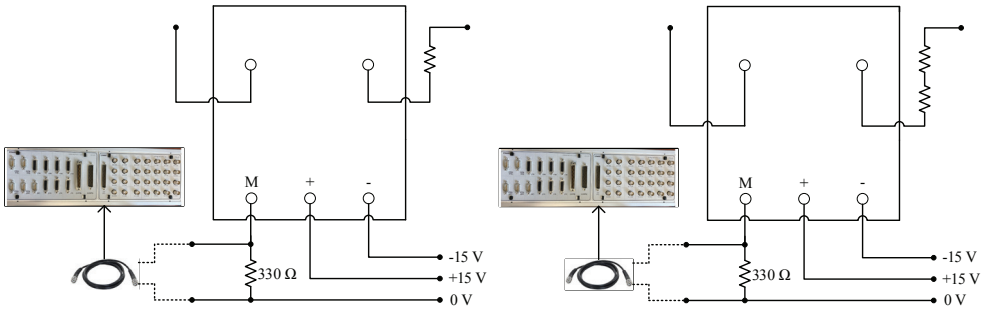

Figure 9. Schematic of the voltage sensor (LV 25-P) connection.

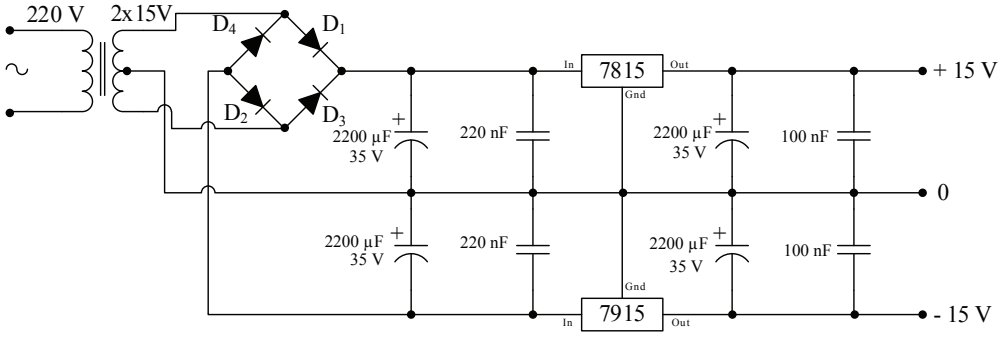

Figure 10. Power supply circuit for the current and voltage sensors.

are used in the supply with a transformer and a full bridge rectifier to provide positive and negative voltage, respectively. They have 1.5 A output current, and +15 V and -15 V output voltage, respectively [24,25]. The power supply feed the all current and voltage transducers.

COMPARISON OF SIMULATION AND EXPERIMENTAL RESULTS

The simulated system in the Matlab/Simulink is seen in Figure 11. In the simulation, a bidirectional switch is used instead of two IGBTS. V_{SA} is grid voltage, and R_{sA}, L_{sA} are internal resistance and inductance value of the grid, respectively. R_{sp} and R_{sr} are used to model internal resistance of L_{sp} and R_{sr}, respectively. L_L and R_L are inductance and resistor value of the line. The fault that is named phase-to-ground is made by a bidirectional switch at the output in parallel with the load. While the system operates in the normal operation, fault switch is turned ON with signal builder, named Fault Signal in the simulation circuit, and therefore fault current exits. The control algorithm senses the fault depending on the voltage and current measurements, and S signal for the

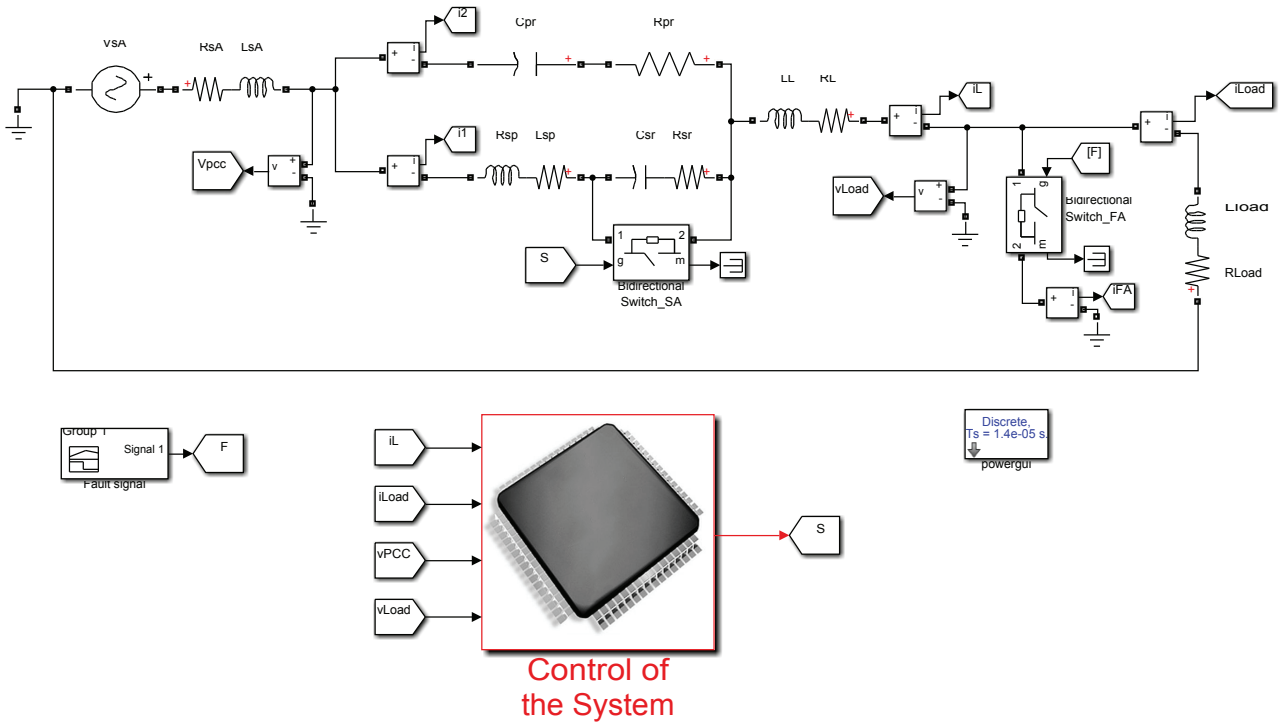

Figure 11. Simulink schematic of the system.

FCL switches is produced. As seen in Figure 3 and Figure 5, the voltages and currents from the points before and after FCL circuit are measured, and using the absolute values of the signals the impedances are calculated. Depending on the impedance difference between input point of FCL and load point, the fault situation is detected. The fault situation continues around 130 ms.

The line current without FCL is seen in Figure 12. The waveform is drawn from only simulation study because the maximum current in the experimental study is higher than laboratory current capacity. During the normal operation, maximum value of the line current is 4.6 A. The current starts increasing with the fault and reaches up to 58.5 A. In a fault, the current increases by approximately 12.6 times. When the fault disappears, the line current falls back to 4.6 A.

As the lower leg has a lower impedance, almost all part of the line current passes on it during the normal operation as seen in Figure 13 and Figure 14. When the fault occurs, impedance value of the lower leg increases because of switching in FCL, and two legs share the fault current inversely proportional to the impedance magnitudes. Maximum value of lower leg current i_1 is 11.5 A while the upper leg current value i_2 is 7 A.

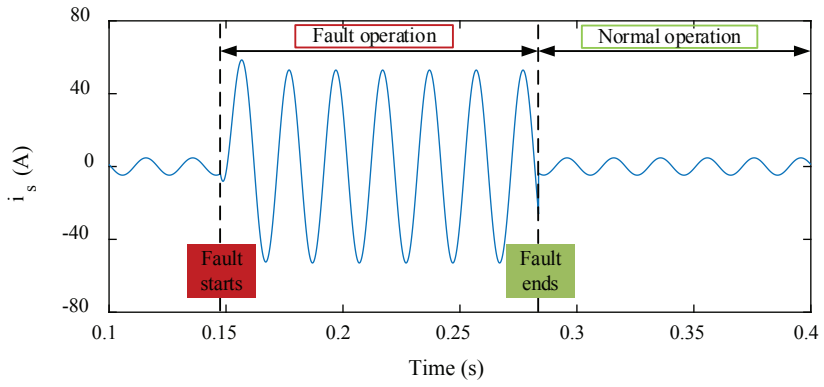

Figure 12. Line current in simulation study without FCL.

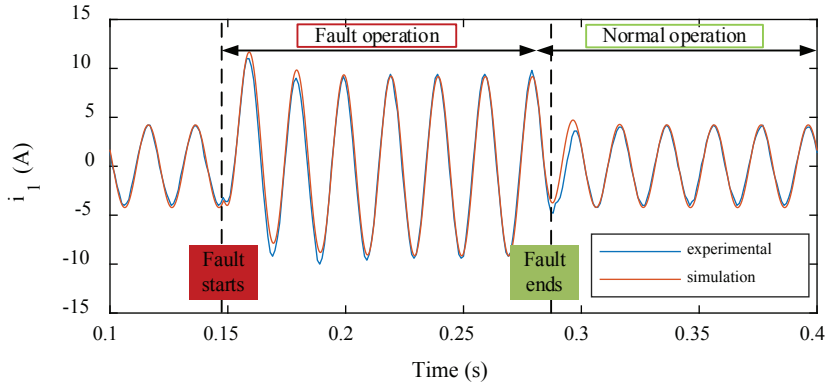

Figure 13. Lower leg current of FCL.

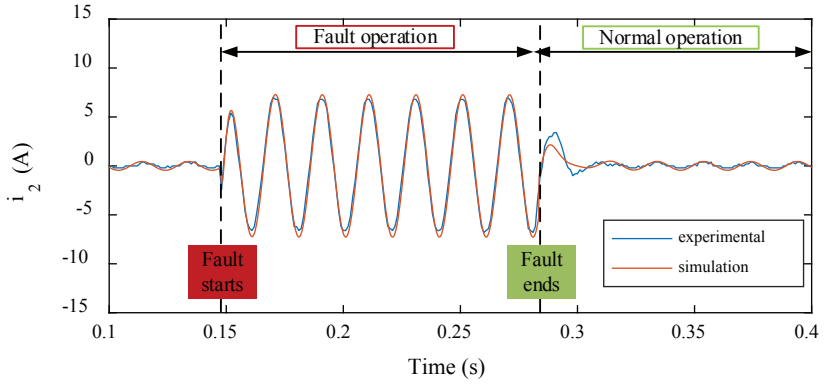

Figure 14. Upper leg current of FCL.

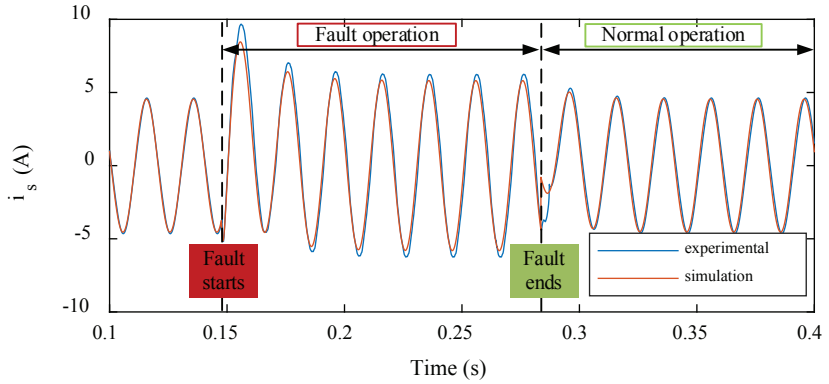

Figure 15. Line current in simulation and experimental study with FCL.

The line current is seen in Figure 15. As seen in the figure, the fault current is suppressed around 9 A. While the red waveforms show the simulation result, the blue waveform is for experimental. The fault duration, point of fault start and stop in the simulation and experimental study are the same. Therefore, two waveforms are being overlapped in the same figure to verify the simulation study. As seen in the figure, the waveforms are almost the same and verify each other.

The load current and voltage waveforms are given in Figure 16 and Figure 17, simultaneously. When the system works in normal operation, the load is fed from the grid. However, when the fault starts, the load voltage is

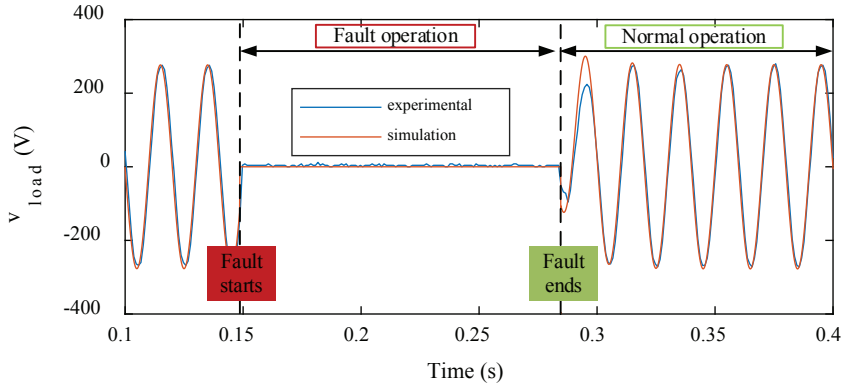

Figure 16. Load current.

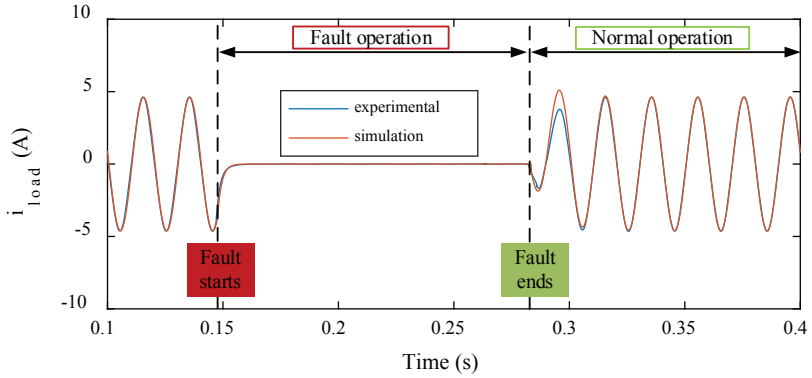

Figure 17. Load voltage.

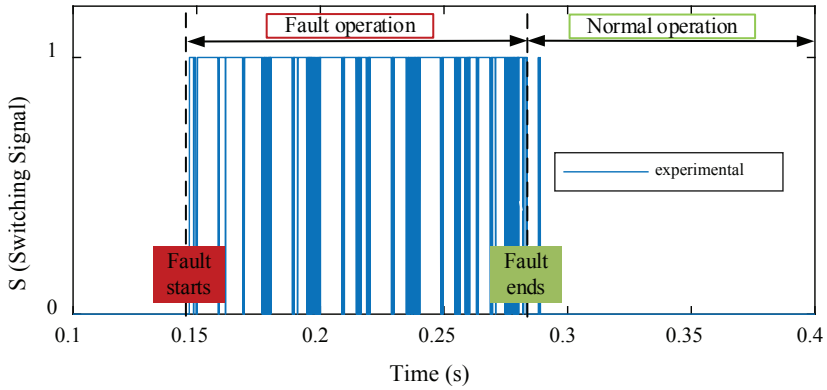

Figure 18. Switching signal of IGBTs in the FCL.

interrupted. While the fault continuous, the load cannot be fed from the grid.

The switching signal of the IGBTs in the FCL is seen in Figure 18. The signal changes based on the control algorithm during the fault situation as seen in the figure. When the fault does not exist, the signal becomes zero. The control algorithm senses the fault and generates switching signals. The signal waveform is for two IGBTs. The related IGBT is switched based on the direction of the current.

As seen in Figure 19, the current of IGBTs is alternative because the waveform is related with total current of two IGBTs. In the setup, the used two IGBTs have no

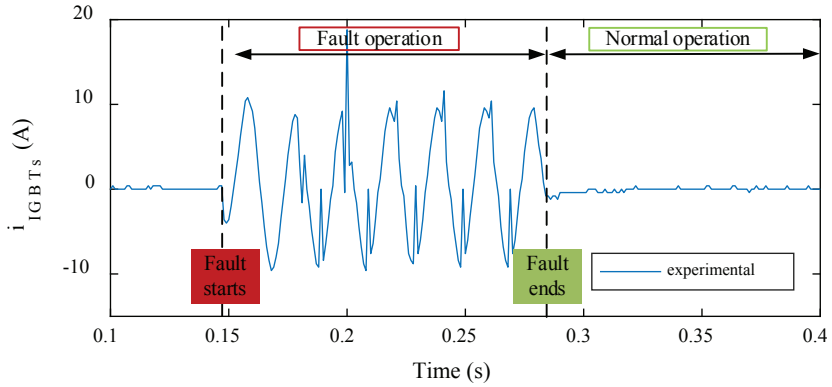

Figure 19. Current of parallel connected IGBTs.

anti-parallel diode. Therefore, there is no any uncontrolled current flow. Each IGBT controls the one direction flow of current. Because there is a high frequency switching during the fault, the IGBT current stays in the limit value for secure operation. In the fault situation, the maximum current value of IGBTs is 19 A.

RESULTS AND DISCUSSION

The working principle and effectiveness of the developed FCL circuit are presented with graphics, current-voltage waveforms and numerical data in the previous sections. The FCL circuit is developed as single-phase and designed to suppress phase-to-ground fault current. The developed FCL and control algorithm circuit decreases the fault current significantly comparing to current value of without FCL. The FCL circuit decreases the fault current of 58.5 A to 9 A with the rate of 85%. Its fault current limiting performance is considerably superior to other low-voltage solid-state FCL prototypes proposed in the literature. Bridge-type solid-state fault current limiter (BSSFCL) which is examined with the source voltage of 110 Vrms reduces the fault current from 22 A to 5 A by 77.3% [26]. Another solid-state FCL of 220 Vrms suppresses the fault current of 18 A in the case without FCL to 8 A at approximately the rate of 55% [27]. At the same voltage level, the fault current has been limited to 50% of the fault current of the no-limiter situation with the resonance type FCL [28].

Although the developed FCL circuit has higher fault current suppressing capability, the circuit should be designed with considering the capacitor discharging. The discharging current of capacitor that is parallel connected to switches could damage the switches depending on the charge value of the capacitor. Therefore, the values of circuit components should be selected considering of that. Also, the discharging current could be suppressed with additional algorithm added into control algorithm to avoid the switches to be damaged. The developed FCL is analyzed detailly in the simulation study, and the components are selected depending on the simulation results. So, the proposed circuit works without any problem of discharging current of capacitor.

CONCLUSION

In this study, the experimental details of a developed single-phase solid-state based fault-current-limiter circuit is given, and the results are compared with simulation results for the phase-to-ground fault. A low voltage and low power simulation of the system is performed in Matlab/Simulink environment. The FCL circuit has 480 V and 16 A capability. In order to verify the results obtained, the FCL effect is observed by applying 220 V input voltage in the laboratory environment. In the application circuit, the components are connected to each other by aluminum sheets, and the resistance values of these sheets are modeled as 0.26 Ω resistance in the simulation to obtain more accurate results. The control of the switches in the FCL circuit is done with the dSpace DS1103 control card. For the test of the system, the phase-to-ground fault is modeled by short-circuiting the load at the output with a contactor. The fault occurs for 130 ms in the system, and the control algorithm senses the fault and switches the solid-state switches. The FCL that shows low impedance in normal operation starts to show higher impedance with switching. Therefore, fault current is limited by FCL. Because the higher part of the current flows on the serial resonance lower leg in the normal operation, FCL does not cause higher voltage drop and power loss. The fault current reaches up to 58.5 A in case of FCL is not used, whereas the developed FCL suppresses the current to around 9 A. The value of maximum fault current decreases to 15% according to the non-FCL used situation. Thus, the circuit breakers are exposed to less current stress. The control algorithm achieves to detect the fault beginning time rapidly, therefore it becomes possible to limit the fault current to lower level. The algorithm uses the calculated impedances to detect the fault situation different from the other

studies that detect the fault depending on the current level. In addition, it recovers the FCL to series resonance topology in a short time. To determine the fault beginning and finish time fast provides higher power quality.

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AUTHORSHIP CONTRIBUTIONS

Authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

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