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Research Article

Investigation on the Effect of Parasitic Elements on PID Control of DC-DC Buck Converter

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ABSTRACT

DC-DC converter circuits are used in many electronic devices to adjust the voltage to a certain level such as Electric Vehicle. DC-DC Buck converters, which are the most used type of DC-DC converters, reduce the input voltage and keep the output voltage constant at a desired reference voltage value. In this study, the effect of parasitic elements in Buck DC-DC converters is examined on the PID controllers. Parasitic elements cause a non-linear effect on the Buck converter system model. Studies in the literature generally control the output voltage by designing controllers on the Buck converter model without parasitic elements. Alternatively, linear controllers such as PID are designed according to the linearizing model, taking into account the effect of parasitic elements. In addition, nonlinear controllers are designed on the full model with the effect of parasitic elements. In this study, the effect of parasitic elements on linear controllers, especially PID, is examined.

Keywords: DC-DC converter, Buck converter, Parasitic elements, PID controller

Parazitik Elemanların DC-DC Buck Dönüştürücünün PID Kontrolüne Etkisinin İncelenmesi

ÖZ

DC-DC dönüştürücü devreleri Elektrikli Araçlar gibi birçok elektronik cihazda gerilimi belirli düzeye ayarlamak için kullanılmaktadır. DC-DC dönüştürücülerin yaygın kullanılan türü olan Buck DC-DC dönüştürücüler giriş gerilimini düşürerek çıkış gerilimini istenen bir referans gerilim değerinde sabit tutar. Bu çalışmada, Buck DC-DC dönüştürücülerdeki parazitik elemanların PID kontrolcüler üzerindeki etkisi incelenmiştir. Parazitik elemanlar Buck dönüştürücü sistem modeli üzerinde lineer olmayan etkiye neden olmaktadır. Literatürde yapılan çalışmalar genellikle parazitik elemanlar olmaksızın Buck dönüştürücü modeli üzerinde kontrolcüler tasarlanarak çıkış gerilimi kontrol edilmektedir. Alternatif olarak, parazitik elemanların etkisi de dikkate alınan model doğrusallaştırılarak lineer kontrolcüler tasarlanmaktadır. Bunlara ek olarak, parazitik elemanların etkisiyle birlikte tam model üzerinde lineer olmayan kontrolcüler tasarlanmaktadır. Bu çalışmada ise parazitik elemanların özellikle PID gibi lineer kontrolcü üzerindeki etkisi incelenmiştir.

Anahtar Kelimeler: DC-DC dönüştürücü, Buck dönüştürücü, Parazit elemanlar, PID kontrolör

I. INTRODUCTION

DC-DC converters are widely used in electronic devices to regulate DC voltage. They are capable of converting voltage from one level to another. Their objective is to regulate and manage the transfer of electrical energy between input and output by adjusting voltages and currents to be compatible with loads. Switches, diodes, inductors, and capacitors play crucial roles as energy storage elements within converter circuits. Modern DC-DC converters are advanced power electronic devices that utilize highfrequency switching circuits with pulse width modulation (PWM) technique. These converters are utilized for numerous applications in industry and academia [1], [2], [3], [4], [5], [6], [7], [8], [9]. The extraordinary increase in their benefits is particularly obvious in sustainable energy systems such as wind turbines, photovoltaics, AC transmission and battery storage [10]. The growth of DC microgrids [4], [9], [11] is encouraging larger applications of DC-DC converters in next power systems. DC microgrids are becoming increasingly popular and a more suitable alternative to AC microgrids due to their simpler power converter stages, flexible control algorithms etc. However, DC microgrids can face instability issues due to non-linear loads like constant power loads (CPL), which have a higher negative impedance, leading to potential voltage collapse on the primary DC Bus. DC voltages produced by fuel cells, batteries or photovoltaic systems change in amplitude; input voltages of powerfactor adjustment applications change with sinusoidal grid voltages; and large-scale reconfiguration of battery packs causes voltage spikes [12], [13], [14]. Therefore, good control design requires adjusting the output voltage. DC-DC converters play a crucial role in Electric Vehicles, which are extensively utilized today, leading to ongoing research on different circuits and controls, as evidenced in the studies mentioned in [1], [15], [16], [17].

One type of commonly used of DC-DC converters are Buck (step down) converter. Buck converters utilize a straightforward yet highly efficient circuit configuration to reduce the input voltage to a lower output level. They are electronic circuits that play a significant role in electrical power systems and have a wide range of applications. Their application areas are in the various electronic devices such as cell phones, televisions, and computers. Also, they are widely used in solar energy systems, where they convert high-voltage DC power from solar panels to lower voltage levels suitable for use and integration with the electrical grid or battery banks such as DC microgrids [18], [19], [20], photovoltaic systems/solar panels [21], [22]. In addition, it is used for DC motor control such as [23], [24], [25]. Additionally, they are frequently found in the power systems of electric vehicle and hybrid vehicle, where they are employed to meet the power demands of onboard electronic systems and lighting by reducing the voltage from the battery [25], [26], [27], [28], [29]. Moreover, in the telecommunications industry, DC-DC Buck converters are often utilized to enhance energy efficiency and optimize power distribution [30]. Finally, they play a crucial role in power conversion and control in industrial equipment and automation systems. DC-DC Buck converters are regarded as essential components in various applications, contributing to energy efficiency, voltage regulation, and effective power distribution in modern electronic systems. Finally, they contribute significantly to power conversion and control, facilitating the efficient operation of many industrial systems.

The presence of parasitic elements, such as resistance, in DC-DC buck converters can have significant effects on their performance. These parasitic elements, often inherent in real-world components, can lead to power loss, reduced efficiency, and decreased voltage regulation. Studies have shown that even small amounts of resistance, particularly in high-power applications, can significantly sap the converter's ability to deliver power efficiently. Additionally, they can cause instability in the converter's dynamic response, impacting its ability to quickly adjust to changes in load or input voltage. Researchers have investigated methods to mitigate these effects, including careful component selection, layout optimization, and advanced control techniques. By addressing parasitic elements, engineers can improve the overall performance and reliability of DC-DC buck converters such as in [31], [32], [33], [34]. For example, in [35], the effect of parasitic resistances on the input resistance in Maximum Power Point Tracking (MPPT) systems of photovoltaic (PV) systems has been investigated. [31] introduces a new method utilizing Adaptive Backstepping for developing a current controller in buck-boost converters by including influence of parasitic elements. [36] discusses the fixed diode duty

cycle operation of Buck converter, considering the parasitic resistances. A simple circuit-level model is presented to explain how undesirable trigger signals occur at the input voltage of a MOSFET in a synchronous converter. [37]. It considers the parasitic inductances and capacitances of both the control and the synchronous MOSFETs, as well as the reverse recovery properties of the synchronous MOSFET's body diode. In [32], a new approach is proposed for the passivity-based nonlinear control design of the buck converter, where the design considers the full converter model, including the impacts of parasitic elements such as equivalent series resistance (ESR) of inductor, ESR of MOSFET. In [38], a nonlinear way/model is proposed to model Buck an Boost converters for both without parasitic elements and with parasitic elements. In [39], the effect of parasitic elements on the output voltages has been investigated. In [40], the effects of parasitic elements have been investigated on power loss in buck converter-based GaN. Finally, parasitic elements can significantly impact the performance of DC-DC buck converters. By understanding their effects and employing proper design techniques, such as minimizing parasitic resistance and inductance, optimizing layout, and selecting appropriate components, converter efficiency, stability, and transient response can be improved.

The aforementioned-works and other relevant studies in the literature are generally related to the effects of parasitic elements on the circuits. However, their effects on control design are not comprehensively examined. This paper presents a comprehensive analysis of control performance and control design challenges caused by parasitic elements in DC-DC Buck converters. As seen in [34], the Buck converter system becomes nonlinear although the values of parasitic elements are low. Therefore, the major problem is that parasitic elements cause nonlinearity due to switching duty ratio. Different controller or different modelling have been proposed to overcome the difficulties. For example, to develop the controller response, the inductor parasitic resistance is modelled for Boost converter in [41]. Additionally, a PID controller is employed to remove any steady-state error of the system. An adaptive nonlinear controller is developed for a DC-DC buck/boost converter, ensuring robustness and stability even with changes in converter load, fluctuations in input voltage, and uncertainties in parameters in [42]. On the other hand, the controller design endures the linearized model of the converter as in [43], where employing this method across a broad spectrum of input voltage fluctuations, load resistances, and desired voltage variations may lead to instability in the converter. Similarly, [44] use the linearized DC-DC boost converter model. Alternatively, nonlinear controllers such as model feedback linearisation, sliding mode, predictive control, fuzzy control are designed for the nonlinear converter model with parasitic elements such as [31], [33], [41], [45], [46], [47]. Therefore, the nonlinear controller design is usually needed if the model is not linearized. However, linear control such as PID is simpler and cheaper. Hence, it depends on linearizing the converter model with parasitic elements or without parasitic elements. As for the analysis in this paper, the effects of PID controllers on the full model containing parasitic elements are investigated.

II. BUCK CONVERTER MODEL

A. DC-DC BUCK CONVERTER CLASSIC/LINEAR MODEL (WITHOUT PARASITIC ELEMENTS))

Figure 1 shows the circuit model of DC-DC Buck converter without parasitic elements. Let's consider the on-state of the MOSFET. According to the equation $v_0 = v_C$, when Kirchhoff's voltage law is applied, Equation [\(1\)](#page-2-0) is obtained, and when it is rearranged, Equation [\(2\)](#page-2-1) is obtained.

$$
V_{in} = L\frac{di_L}{dt} + v_C \tag{1}
$$

$$
V_{in} - L\frac{di_L}{dt} - v_C = 0\tag{2}
$$

When Kirchhoff's current law is applied, Equation [\(3\)](#page-3-0) is obtained, and when it is rearranged, Equation [\(4\)](#page-3-1) is obtained.

Figure 1. Buck converter on-off state

$$
i_0 + i_c - i_L = 0 \tag{3}
$$

$$
\frac{v_C}{R} + C \frac{dv_C}{dt} - i_L = 0 \tag{4}
$$

When Equation [\(2\)](#page-2-1) and Equation [\(4\)](#page-3-1) are rearranged, Equatio[n \(5\)](#page-3-2) is obtained.

$$
\frac{di_L}{dt} = \frac{1}{L}(V_{in} - v_C)
$$

$$
\frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{v_C}{R}\right)
$$
 (5)

Using Equation [\(5\)](#page-3-2) and Equation $v_0 = v_C$, the state space matrices in Equation [\(6\)](#page-3-3) are obtained as in Equation [\(7\).](#page-3-4)

$$
\dot{x}(t) = Ax(t) + Bu(t)
$$

\n
$$
y(t) = Cx(t) + Du(t)
$$
\n(6)

 $[V_{in}]$ $\begin{bmatrix} 0 & 1 \end{bmatrix}$ $\begin{bmatrix} 0 & \frac{-1}{2} \\ 0 & \frac{-1}{2} \end{bmatrix}$ $\frac{L}{1}$ $\frac{1}{-1}$ $\left| \frac{I_L}{V_C} \right| + \left| \frac{L}{0} \right|$ *on on on* dI_L *L in* $\left[\begin{array}{ccc} 1 & 1 \\ - & \end{array}\right]$ $\left[\begin{array}{ccc} 1 & 1 \\ - & \end{array}\right]$ $\left[\begin{array}{ccc} 1 & 0 \\ 0 & \end{array}\right]$ *u* $\frac{dt}{dt}$ $\frac{c}{A_m}$ *Rc*_{*B_n*} *L* $C_{\scriptscriptstyle{cm}}$ $\begin{bmatrix} 0 & \mathbf{C} \\ \mathbf{C} & \mathbf{C} \end{bmatrix}$ *x* $\frac{d}{dt}$ $\begin{bmatrix} = \begin{bmatrix} 0 & \overline{L} \end{bmatrix} \begin{bmatrix} I_L \ \overline{L} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \ \overline{L} \end{bmatrix} \begin{bmatrix} V_L \ \overline{L} \end{bmatrix}$ $\left[\frac{dV_c}{dt}\right]$ $\left[\frac{1}{c}\right]$ $\left[\frac{-1}{RC}\right]$ $\left[\frac{V_c}{v_c}\right]$ *I y V L* $\left[\frac{dI_L}{dt}\right]_-\left[0 \quad \frac{-1}{L}\right] \left[I_L\right]_+\left[\frac{1}{L}\right]_{[V]}$ $\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ u \end{bmatrix}$ $\begin{bmatrix} A_{on} \ I_L \end{bmatrix}$ $=[0 \quad 1] \begin{bmatrix} I_L \\ V_C \end{bmatrix}$ (7)

Similarly, we get the state space equation in [\(8\).](#page-4-0)when we consider the off-state of the MOSFET in Figure 1.

$$
\begin{bmatrix}\n\frac{dI_L}{dt} \\
\frac{dV_C}{dt}\n\end{bmatrix} =\n\begin{bmatrix}\n0 & \frac{-1}{L} \\
\frac{1}{C} & \frac{-1}{RC}\n\end{bmatrix}\n\begin{bmatrix}\nI_L \\
V_C\n\end{bmatrix} +\n\begin{bmatrix}\n0 \\
0\n\end{bmatrix}\n\begin{bmatrix}\nV_m \\
u\n\end{bmatrix}
$$
\n
$$
y =\n\begin{bmatrix}\n0 & 1\n\end{bmatrix}\n\begin{bmatrix}\nI_L \\
V_C\n\end{bmatrix}
$$
\n(8)

Now let's derive the state space average model. Since the duty ratio (*d*) of the period is in conduction and the (1-*d*) ratio is in cutoff, the average model is obtained as in Equation [\(9\),](#page-4-1) where *d* is MOSFET switching duty ratio ranging between 0 and 1.

$$
A = d \times A_{on} + (1 - d) \times A_{off}
$$

\n
$$
B = d \times B_{on} + (1 - d) \times B_{off}
$$

\n
$$
C = d \times C_{on} + (1 - d) \times C_{off}
$$
\n(9)

If we apply the average model approach in Equation [\(9\),](#page-4-1) we get [\(10\)](#page-4-2) state space average model.

$$
\begin{bmatrix}\n\frac{dI_L}{dt} \\
\frac{dV_C}{dt}\n\end{bmatrix} =\n\begin{bmatrix}\n0 & \frac{-1}{L} \\
\frac{1}{C} & \frac{-1}{C_R}\n\end{bmatrix}\n\begin{bmatrix}\nI_L \\
V_C\n\end{bmatrix} +\n\begin{bmatrix}\nV_m \\
L \\
0\n\end{bmatrix}\n\begin{bmatrix}\nd \\
u\n\end{bmatrix}
$$
\n
$$
y =\n\begin{bmatrix}\n0 & 1\n\end{bmatrix}\n\begin{bmatrix}\nI_L \\
V_C\n\end{bmatrix}
$$
\n(10)

B. DC-DC BUCK CONVERTER FULL MODEL (WITH PARASITIC ELEMENTS)

In electrical circuits, a parasitic element is a circuit element (such as resistance, inductance or capacitance) that is present in an electrical component but occurs outside its intended purpose and is not desired. For example, a resistor may have undesirable parasitic capacitance at high frequencies beyond its specification. Figure 2 shows the converter circuit including parasitic elements (parasitic resistances). r_m , r_p r_l and r_c are the parasitic resistances of the MOSFET, diode, inductor, and capacitor, respectively. In addition, the diode forward voltage is V_D . It is supposed that the forward voltage is zero.

Figure 2. Buck converter circuit with parasitic resistances

Similar to the modelling steps in Section A can be applied for this circuit. After the steps, we get state system model is linearized.

Shimal to the modelling step in Section 11 can be defined for this circular. That are they, we get state space average model (11). (12) is obtained from full model (11) for
$$
r_m = r_D = 0
$$
. Therefore, the system model is linearized.

\n
$$
\left[\frac{dI_L}{dt}\right] = \left[\frac{-1}{L}\left(d\left(r_m - r_D\right) + r_D + r_L + \frac{r_C R}{\left(r_C + R\right)}\right) - \frac{-1}{L}\frac{R}{\left(r_C + R\right)}\right] \left[\frac{I_L}{C}\right] + \left[\frac{V_m}{L}\right] \left[d\right]
$$
\n
$$
y = \left[\frac{r_c R}{\left(r_c + R\right)} - \frac{R}{\left(r_c + R\right)}\right] \left[\frac{I_L}{V_C}\right]
$$
\n
$$
\left[\frac{dI_L}{dt}\right] = \left[\frac{-1}{L}\left(r_L + \frac{r_C R}{\left(r_C + R\right)}\right) - \frac{-1}{L}\frac{R}{\left(r_C + R\right)}\right] \left[\frac{I_L}{V_C}\right] + \left[\frac{V_m}{L}\right] \left[d\right]
$$
\n
$$
\frac{dV_C}{dt} = \left[\frac{1}{r_c + R}, \frac{R}{\left(r_c + R\right)}\right] \left[\frac{I_L}{C}\right] - \frac{1}{c}\frac{1}{\left(r_c + R\right)}\right] \left[\frac{I_L}{V_C}\right] + \left[\frac{V_m}{L}\right] \left[d\right]
$$
\n
$$
y = \left[\frac{r_c R}{\left(r_c + R\right)} - \frac{R}{\left(r_c + R\right)}\right] \left[\frac{I_L}{V_C}\right]
$$
\n(12)

III. SIMULATION RESULTS

Accordingly, we compare between [\(10\),](#page-4-2) [\(11\)](#page-5-0) and [\(12\)](#page-5-1) which are without parasitic elements, full model with parasitic elements and with partial parasitic elements $(r_c$ and r_L). Hence, we present the results of open loop parasite elements and with partial parasite elements v_c and r_L). Thence, we present the results of open hopp
model according to Parameters 1 and Parameters 2 in Table 1. Figure 3 represents that the output voltages of ording to Parameters 1
erter for *d*=0.2. Figure 4
o Parameters 1.
= $\frac{V_o}{d} = \frac{3.507 \times 1}{s^2 + 152s + 2.3}$

Buck converter for *d*=0.2. Figure 4 shows that the output voltages for *d*=0.5. The transfer functions are as in (13)
according to Parameters 1.

$$
G_{ideal/classic} = \frac{V_o}{d} = \frac{3.507 \times 10^8}{s^2 + 152s + 2.338 \times 10^7} (from Eq. 10)
$$

$$
G_{(r_m=r_d=0)} = \frac{V_o}{d} = \frac{1614 \text{ s} + 3.505 \times 10^8}{s^2 + 951.8s + 2.347 \times 10^7} (from Eq. 12)
$$
(13)
$$
G_{(d=0.5)} = \frac{V_o}{d} = \frac{1614s + 3.505 \times 10^8}{s^2 + 9221s + 2.473 \times 10^7}, G_{(d=0.2)} = \frac{V_o}{d} = \frac{1614s + 3.505 \times 10^8}{s^2 + 4952s + 2.408 \times 10^7} (from Eq. 11)
$$

From Figure 3 and 4, as *d* decreases, the difference between linearized models and the full model with parasitic elements increases. Therefore, it can be deduced that the difference between models increases as the difference between output voltage and input voltage increases. From state space form, the pole-zero map is obtained as in Figure 5, where the poles vary significantly. Especially for Parameters 1, the poles vary significantly more.

Figure 3. Output voltages for d=0.2 (a) Parameters 1 and (b) Parameters 2

Figure 4. Output voltages for d=0.5 (a) Parameters 1 and (b) Parameters 2

Figure 5. Pole-zero map for (a) Parameters 1 and (b) Parameters 2

Today, classic, and modern control systems are widely used in the literature. Among the classic control techniques, we can say that the PID control technique is the most widely used in industry. The reasons for this can be listed as its simplicity, low cost, not requiring high processing capacity, and easy implementation. However, this control technique is ineffective in systems that require high performance such as nonlinear systems, systems with a large parameter change range, or systems with sudden disturbances. PID control is a feedback control technique. Although PID control can yield better results, PI is not preferred in practice since the derivative effect can introduce noise. However, the derivative can be derived from integrator with filter N. The PID control system is presented in Figure 6. The mathematical equation of the PID controller is as follows. Where *e* is the error signal, and *u* is the control input signal.

$$
u(t) = K_p e(t) + K_i \int e(t) + K_D \frac{de(t)}{dt}
$$

$$
U(s) = \left(K_p + \frac{K_i}{s} + K_p s\right) E(s) \rightarrow U(s) = \left(K_p + \frac{K_i}{s} + K_D \frac{N}{1 + N \frac{1}{s}}\right) E(s)
$$

$$
\xrightarrow{r(t)} \underbrace{\sum_{t \in \mathcal{L}} e(t)}_{t \in \mathcal{L}} \underbrace{\left(\sum_{t \in \mathcal{L}} e(t)\right)}_{t \in \mathcal{L}}
$$

Figure 6. PID Control block diagram

In PI/PID control design, finding the optimum values of *P*, *I* and *D* parameters is important for control success. Different methods have been proposed in the literature for this purpose. Some of them are Ziegler-Nichols, Cohen and Coon method, Tyreus-Luyben, IMC (Internal Model Control), C-H-R (Chien, Hrones, Reswick) method, Fertik method [48], [49], [50]. Some optimization methods are also utilized [50]. Since the focus of this study is not on PID design, the PID parameters are obtained by using the "PID Tuner" tool in MATLAB Simulink. The block diagram created for this is shown in Figure 7. Clicking on the PID block opens the PID block parameters screen in Figure 7. When the "Tune" button is pressed here, the "PID Tuner" tool screen appears.

Accordingly, the parameters are arranged and adjusted according to behaviour due to input saturation
after PID is designed by the tool. According to this, the PID control is designed for Parameters 1 and
Parameters 2 as f Parameters 2 as follows.

Accordingly, the parameters are arranged and adjusted according to behaviour due to input saturation after PID is designed by the tool. According to this, the PID control is designed for Parameters 1 and Parameters 2 as follows.

\n
$$
U(s) = \left(5 + \frac{700}{s} + 0.001 \frac{34926000}{1 + 34926000} \right) E(s), \quad U(s) = \left(1 + \frac{280}{s} + 0.00018 \frac{12585586}{1 + 12585586} \right) E(s)
$$

Figure 7. "PID Tuner" Tool Screen

Let's compare the performance of the PI controller without and with the inclusion of parasitic elements. Figure 8 shows the output voltages for a reference of 5V. The simulation results demonstrate that the designed PID control in regard to ideal/classic model in Equation [\(10\)](#page-4-2) is successful for the nonlinear/full model. Hence, ideal/classic model in [\(10\)](#page-4-2) can be used for the linear controller design like PID design. However, PID is of short-time steady state error for Parameters 2.

Figure 8. The output voltages for(a) Parameters 1 and (b) Parameters 2

We can remark on the simulation results from different perspectives as follows.

Remark 1: However, the effect of *d* in [\(11\)](#page-5-0) should be analyzed for frequency, just as analysis is made in time domain. Therefore, bode analysis can be made to *d*. In addition, if a specific topic will not be addressed such as disturbance rejection or observer, linearized models can be utilized for PID controller design.

Remark 2: The simulation tests are conducted for only two different parameters. So, it should not be ignored that the designed PID may not be successful according to ideal/classic model in [\(10\)](#page-4-2) when the effects of *d* in [\(11\)](#page-5-0) are much more to the poles/zeros. This entirely depends on the values of parameters. For instance, if the input voltage of V_{in} in [\(11\)](#page-5-0) is quite bigger than the output voltage V_0 , *d* is more effective to the poles/zeros. Hence, the PID may not succeed.

Remark 3: In general, it can be interpreted that linear controller design, like PID, according to the linearized model, can be used under certain conditions. In addition, it should be applied to the full model to test its performance after PID design according to the linearized model. Moreover, the more suitable control techniques should be focused on for topics such as disturbance rejection, disturbance observer, and sensorless control.

Remark 4: The model considered in this study is valid for low and medium frequency. In this study, PWM is tried at medium frequencies such as 150-200 kHz and similar results are obtained. Since capacitance and inductance effects may also be involved at high frequencies, they need to be examined separately.

IV. CONCLUSION

This study examines the PID control design performance for a simple buck converter. For this purpose, the analysis is performed both on the effect of parasitic elements and the ideal/classical model where parasitic elements are neglected. The findings indicate that, under certain conditions, PID and similar low-order linear controllers designed according to the linearized model can be implemented to the full/non-linear model containing parasitic elements. Simulation results reveal that PID performance may be weakened in circuits where the difference between input and output voltage is large, and the values of the circuit parameters increase the effect of *d*. In general, it can be interpreted that linear controller designs such as PID based on linearized models can often be

implemented under certain conditions. However, it is imperative to verify their performance on the fully nonlinear model after PID design using the linearized model. Additionally, emphasis should be placed on investigating more appropriate control techniques to overcome challenges such as rejection of disturbances, use of disturbance observers, and implementation of sensorless control. Consequently, it can be concluded that designing PID control and similar low-order linear controllers based on linear Buck models depends on design priorities and effect of Buck converter parameters on duty cycle *d*.

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