GU J Sci 30(4): 283-294 (2017)

Gazi University

Journal of Science

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Two Novel Subthreshold Logic Families for Area and Ultra Low-Energy Efficient Applications: DTGDI & SBBGDI

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Article Info

Received: 09/06/2017
Accepted: 18/08/2017

Keywords

Area
DTGDI
EDP
SBBGDI
Subthreshold
Ultra low-energy

Abstract

Two novel area and ultra low-energy efficient subthreshold logic families: Dynamic Threshold Gate Diffusion Input (DTGDI) and Swapped Body Bias Gate Diffusion Input (SBBGDI) are introduced. These logic families examine the effectiveness of GDI based circuits over the Conventional CMOS (C-CMOS) logic circuits using subthreshold optimal area overhead free body biasing schemes. The basic logic gates OR, AND and XOR are designed using the proposed DTGDI and SBBGDI logic. To analyze the performance, a full adder cell is implemented. The simulations are performed in Cadence 45nm technology with 0.2V supply voltage. The simulation results show that the proposed DTGDI full adder circuit with layout area of only 6.891μm^2 offers more than 41% savings in energy ,78% savings in EDP than the Conventional CMOS (C-CMOS) and more than 12% energy savings, 27% savings in EDP than the GDI. Whereas, the SBBGDI full adder circuit with layout area of only 5.654 μm^2 offers more than 47% savings in energy ,90% savings in EDP than the C-CMOS and more than 24% energy savings, 67% savings in EDP than the GDI.

1. INTRODUCTION

Recent trends in applications like low-power Digital Signal Processors (DSP), micro sensor networks, Radio Frequency Identification (RFID) and many others which take the advantage of low energy operation, demands the need for subthreshold circuits. The circuits operating in the subthreshold regime uses a supply voltage less than the threshold voltage of the transistors. The subthreshold current of an MOS transistor is given in equation 1 [1].

$$I_{sub} = I_0 e^{(V_{GS}-V_T)/nV_{th}} \quad (1)$$

Where I_0 is the drain current when $V_{gs}=V_T$ and is given by

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) V_{th}^2 \quad (2)$$

The parameters V_T is the threshold voltage, V_{gs} is the gate to source voltage, V_{th} is the thermal voltage (kT/q), W/L is the effective channel width to the length ratio, μ_0 is the zero bias mobility and n is the subthreshold slope factor ($n=1+C_d/C_{ox}$) where C_d and C_{ox} are the depletion and oxide capacitances of the MOS transistor respectively.

However, subthreshold computing is a very effective approach in reducing energy consumption but at the expense of performance degradation, more leakage and high sensitive to process variations. Body biasing is one of the popular solution to address these issues, where the transistor threshold voltage can be varied

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with respect to the applied body biasing voltage based on the performance requirements. This effect of variations in V_{th} due to body bias is known as body effect. The basic equation which models the impact of body bias on V_T is given in equation 3 [1].

$$V_T = V_{T0} + \gamma(\sqrt{2\varphi_B - V_{BB}} - \sqrt{2\varphi_B}) \quad (3)$$

Where the parameters V_{T0} is the threshold voltage with zero body bias, γ is the body effect coefficient, $ø_B$ is the flatband voltage and V_{BB} is the body bias voltage. The body bias voltage (V_{BB}) is the potential between body terminal and source terminal of the transistor. From equation 3, it can be noticed that if V_{BB} is positive, V_T will increase and vice-versa.

Many body biasing approaches for the design of ultra-low voltage circuits have been reported earlier in the literature [2-6], each of them having its own trade-offs in terms of area, delay, power and process complexity. Adaptive body biasing and Variable threshold schemes [4,5] were proposed to mitigate Process and temperature variations. But these schemes make the design complex and also increase the area of the chip due to the use of additional stabilization circuitry. Forward Body Biasing (FBB) and Reverse Body Biasing (RBB) are the most conventional body biasing schemes, where forward biasing the body to source junction improves the performance and reverse biasing the body to source junction reduces the leakage [3]. Both the FBB and RBB, apply a constant biasing voltage to the body to source junctions of the device. Since this biasing voltage is independent of the supply voltage, these schemes also incur the area penalty. In [2], a Dynamic Threshold MOS (DTMOS) scheme was introduced, where body terminal of the MOSFET is connected to the gate input. This scheme reduces the leakage by raising the V_T of the transistor when the gate voltage V_{gs} is low and improves the speed by lowering the V_T when Vg is high. In [6], Dynamic Threshold Pass Transistor (DTPT) logic scheme was proposed, which uses auxiliary devices to improve the current drive of the device. This scheme is more energy efficient, but it also requires more area due to the additional auxiliary transistors. Swapped Body Bias (SBB) scheme for low voltage high speed CMOS circuits was proposed in [7]. In this, the body connections of the PMOS and NMOS transistors are swapped each other to provide forward bias equal to the supply voltage, to both the PMOS and NMOS devices.

Gate Diffusion Input (GDI) [8] is one of the most energy efficient logic family, where complex digital circuits can be realized with less transistor count compared to the C-CMOS [9-11] and pass transistor [11,12] logic's. Note that, the GDI cell which is compatible with standard CMOS process [13] is used in this work. Since the GDI cell will not provide full swing output for some input combinations, the functionality of the circuits may fail when multiple GDI gates are cascaded. This issue may become even worse in sub-threshold computing. To overcome this, additional buffer stages are required. This, in turn, adds more area on the chip and also increases power consumption. Hence there is a need of new energy efficient and area overhead free logic families. The logic families DTGDI and SBBGDI proposed in this paper reduces the voltage swing issue of the GDI based circuits in the subthreshold region and provide a new pathway for area and energy efficient subthreshold digital design.

The rest of this paper is organized as follows. Two new subthreshold logic families DTGDI and SBBGDI are introduced in section-2.The simulation results obtained from the basic logic gates OR, AND, and XOR have also been presented in this section-2. Section-3 evaluates the performance of the proposed logic families with the help of an energy efficient full adder design. The simulation results with comparative analysis have also been presented in section-3 and some conclusions are summarized in section-4.

2. PROPOSED LOGIC FAMILIES: DTGDI & SBBGDI

GDI is one of the familiar logic family which allows realization of a wide range of complex logic functions with only two transistors [8,13]. Figure 1 clearly depicts the differences between the basic CMOS and GDI cell structures, with and without body biasing. However, GDI structure resembles the standard CMOS inverter but the key difference is that the GDI cell consists of three inputs (G, P, and N).

Different boolean logic functions can be realized using the GDI cell by simply changing the inputs. Table 1 shows the logic table for implementing various boolean functions using GDI and table 2 shows the transistor count comparison between the GDI and conventional CMOS implementations of different boolean functions. F1 and F2 are the two universal logic functions offered by GDI which can be used to realize other complex functions more efficiently than the universal NAND and NOR logic gates.

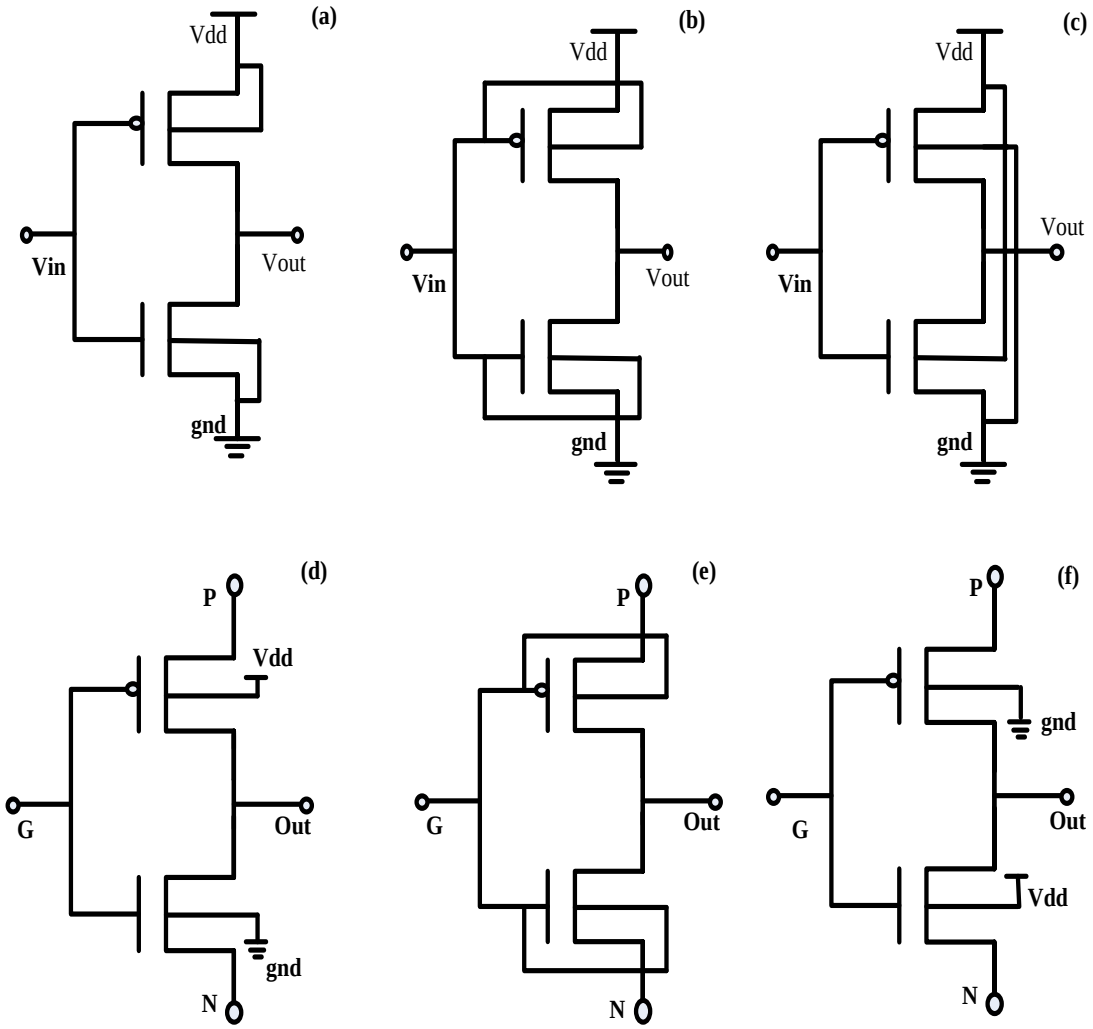


Figure 1. *Basic subthreshold logic structures;a) C-CMOS inverter b) DT-CMOS inverter c) SBB-CMOS inverter d) GDI cell e) DTGDI cell f) SBBGDI cell.*

The operation of GDI cell is similar to the Pass Transistor Logic (PTL) [11], but the key difference is that the top-down logic design complexity in providing universal cell library is more with PTL, whereas the GDI logic family provides simple top-down logic design using a small cell library. Quantitative expressions of GDI logic circuits have been presented in [8]. GDI logic enjoys significant energy savings with less transistor count but lags in providing full swing output due to the threshold voltage drops. In the subthreshold region of operation, this output swing issue may become even more serious and also the functionality of the circuit may fail.

From the brief overview of the popular body biasing schemes presented in section 1, it is evident that SBB and DTMOS are the two area overhead free and high performance body biasing schemes optimal for subthreshold design. DTGDI and SBBGDI logic families are the enhanced versions of GDI logic family, which are incorporated with DTMOS and SBB schemes respectively to improve the energy efficiency and output swing of GDI logic.

***Table 1**. Implementation of various boolean functions using GDI cell*

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A} + B$	F2
'0'	'1'	A	$\overline{A}$	NOT
B	'0'	A	AB	AND
'1'	B	A	A+B	OR
C	B	A	$\overline{A}B + AB$	MUX

***Table 2.** Transistor count comparison*

Function	No.of transistors required	
	CMOS	GDI
F1	6	2
F2	6	2
NOT	2	2
AND	6	2
OR	6	2
XOR	12	4
MUX	12	2

***Table 3.** Comparison of different subthreshold logic structures for implementing AND, OR and XOR logic functions*

Design	Logic	Power(pW)	Delay(μs)	Energy(aJ)	EDP(yJs)
AND	C-CMOS	0.781	0.642	0.502	0.322
	DT-CMOS	1.07	0.464	0.496	0.230
	SBB-CMOS	1.539	0.284	0.438	0.124
	GDI	0.065	0.372	0.024	0.008
	DTGDI	0.132	0.048	0.006	0.0003
	SBBGDI	0.149	0.028	0.004	0.0001
OR	C-CMOS	0.843	0.541	0.456	0.246
	DT-CMOS	1.094	0.389	0.425	0.165
	SBB-CMOS	1.643	0.225	0.369	0.083
	GDI	0.071	0.232	0.016	0.003
	DTGDI	0.158	0.039	0.006	0.0002
	SBBGDI	0.167	0.02	0.003	0.00006
XOR	C-CMOS	1.673	0.535	0.896	0.480
	DT-CMOS	2.664	0.333	0.887	0.295
	SBB-CMOS	3.157	0.244	0.772	0.189
	GDI	0.5845	0.232	0.135	0.031
	DTGDI	0.826	0.121	0.099	0.012
	SBBGDI	1.021	0.092	0.093	0.008

The DTGDI cell is created by replacing the transistors in the GDI cell with DTMOS devices shown in figure 1(e). In this, the threshold voltage (V_T) of the transistor is dynamically varied with the gate voltage (V_g) which improves the speed by lowering the V_T (when $V_g=V_{BB}=V_{dd}$) and reduces the leakage by raising the V_T (When $V_g=V_{BB}=0$). The SBBGDI cell shown in the figure 1(f) is created by swapping the body terminals of the transistors (PMOS body to gnd instead of V_{dd} and NMOS body to V_{dd} instead of gnd) to provide constant forward body bias (equal to V_{dd}) for all the devices. This constant forward bias

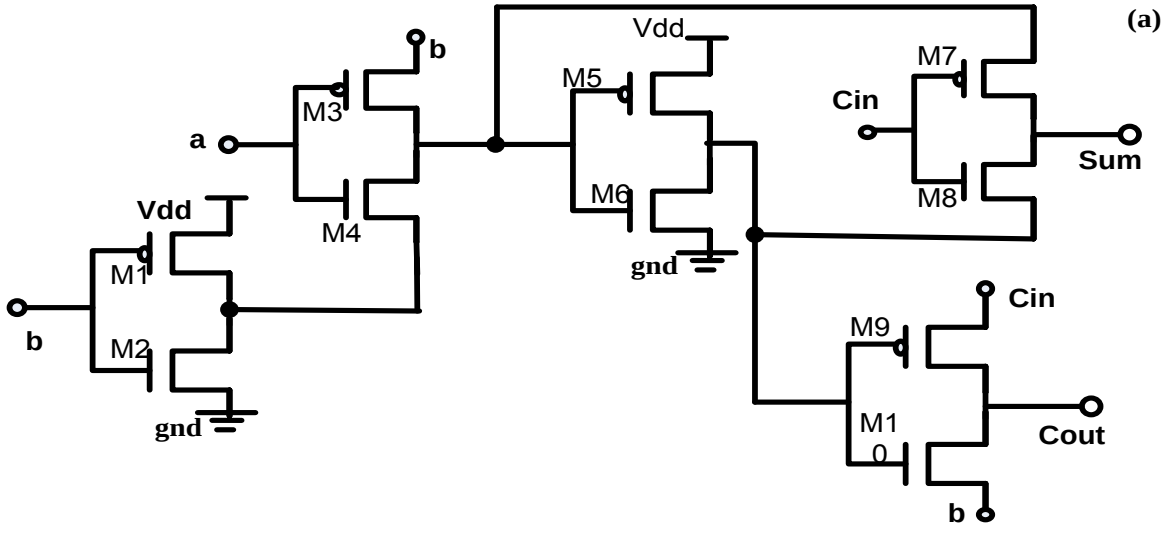
decreases the channel depletion region, which lowers the V_T. As a result of lowering the V_T with a strong dependency on V_{BB}, significantly improves the speed of the design.

The basic logic gates NOT, AND, OR, XOR is designed first to verify the functionality of the proposed DTGDI and SBBGDI logic families. Later the designs are extended to 1-bit full adder circuit, to evaluate the performance of the proposed logic families. The transistors are sized for minimum energy consumption at V_{dd}=0.2V with 20 KHz operating frequency. All the simulations are performed in cadence 45nm technology. The simulation results of the DTGDI and SBBGDI logic gates in comparison with different logic families are shown in the table 3. It can be noticed that energy consumption of the proposed logic circuits is significantly reduced when compared with the other logic designs. It should be noted that the power calculations presented in this paper is the average of the total power consumed.

3. PROPOSED LOGIC FAMILIES: DTGDI & SBBGDI

3.1. Full Adder Designs

To validate the performance of the proposed DTGDI and SBBGDI logic families, full adder cell is implemented. In [14] a novel area and energy efficient full adder circuit with only 10 transistors is designed using GDI logic as shown in figure 2(a). The same full adder structure is chosen to evaluate the performance of the proposed logic families in the subthreshold region. As GDI cell suffers from output swing problem, the design shown in figure 2(a) also suffers from the same. This problem will severely degrade the performance in the subthreshold region. So, we modified the original design (figure 2(a)) to subthreshold optimal design as shown in figure 2(b). The structure of both the full adder cell looks same but in the modified full adder design the critical path transistors cells which results in threshold drop are replaced with low V_T cells to improve the output swing and performance in the subthreshold region. The comparisons and variations of power, delay, Energy and EDP for original design versus modified design is shown in table 4 and figure 3 respectively. It can be observed that, with the use of low V_T devices in the critical paths, the modified design provides 78% more performance than the original design at the cost of 56% increase in power consumption. However, we can use high V_T devices in the non-critical paths of the design, but in the subthreshold operation with GDI logic which produces threshold drops, the use of high V_T devices results in more performance loss and sometimes leads to functionality failure. As the overall energy consumption and EDP of the modified design is reduced by more than 40% and 90% than the original design respectively, here the conflict with the power consumption can be neglected.



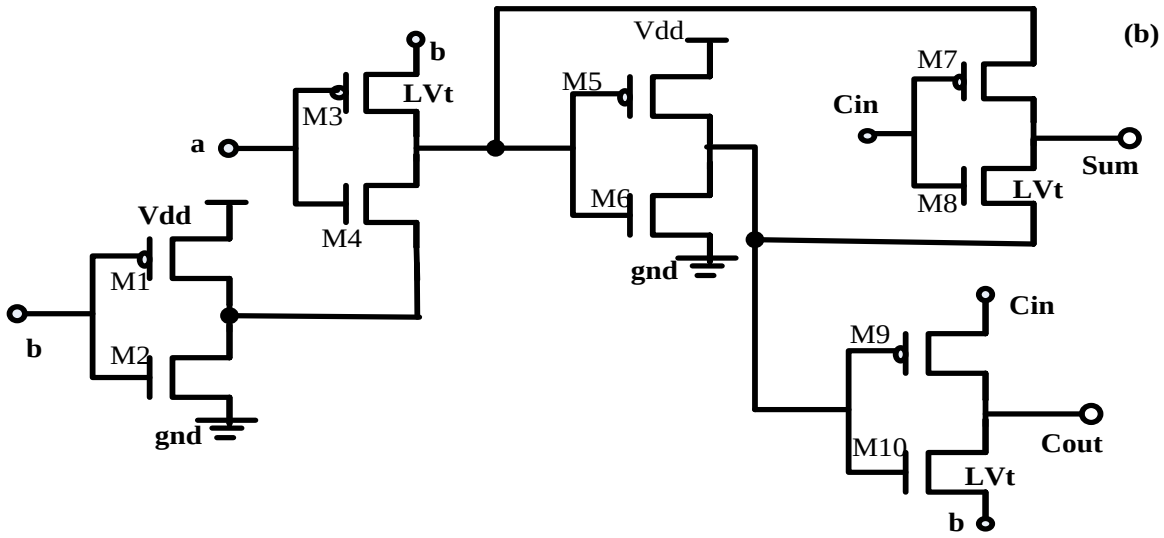


Figure 2. *GDI based 1-bit full adder circuits; a) Originally proposed GDI based full adder circuit b) Modified full adder circuit for improved swing and performance in subthreshold region*

Table 4. *Comparison of power, delay, energy and EDP metrics for originally proposed and modified GDI based full adder designs with V_{dd}=0.2V*

Design	Power (pW)	Delay (µs)	Energy (aJ)	EDP (yJs)
Original GDI	1.665	3.3	5.494	18.131
Modified GDI	3.797	0.7	2.657	1.86

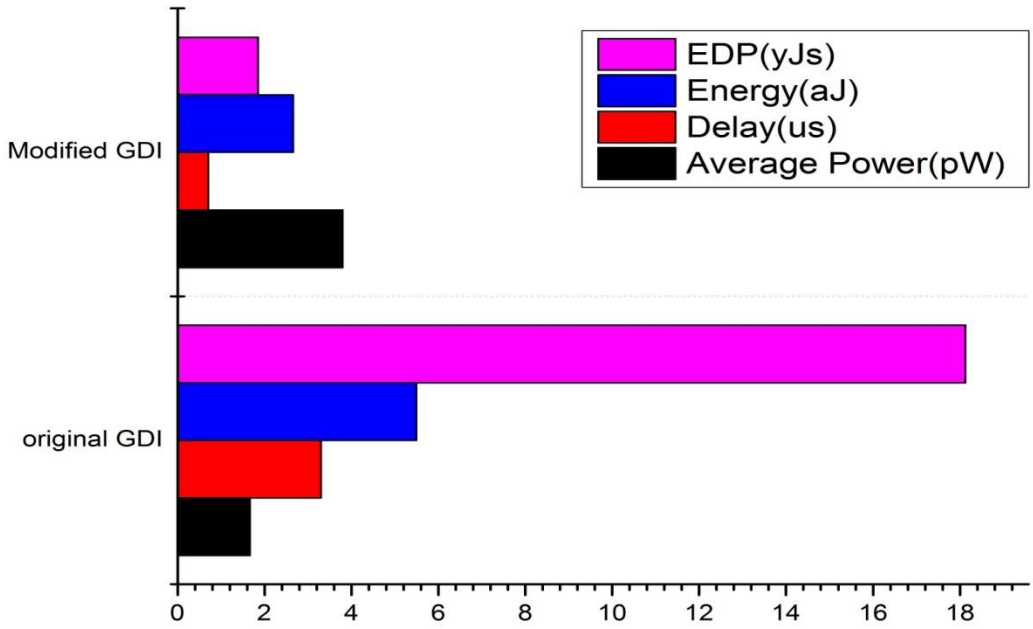


Figure 3. *Power, delay, energy and EDP variations for originally proposed and modified GDI based full adder designs with V_{dd}=0.2V*

As the modified design provides better performance with minimum energy consumption, the Dynamic Threshold MOS (DTMOS) and Swapped Body Bias (SBB) schemes are applied to the modified subthreshold energy efficient full adder circuit design (figure 2(b)) to further improve the performance of the design using the new DTGDI and SBBGDI logic families respectively. Figure 4 shows the time evolution of the carry output signal (C_{out}) for the original GDI full adder design versus modified GDI full adder design, DTGDI and SBBGDI full adders with respect to the input signals (a,b and C_{in}). It clearly depicts that the modified design provides significant improvements in the output swing and performance. Also, the proposed DTGDI and SBBGDI full adder circuits show further improvement in the performance than the modified design.

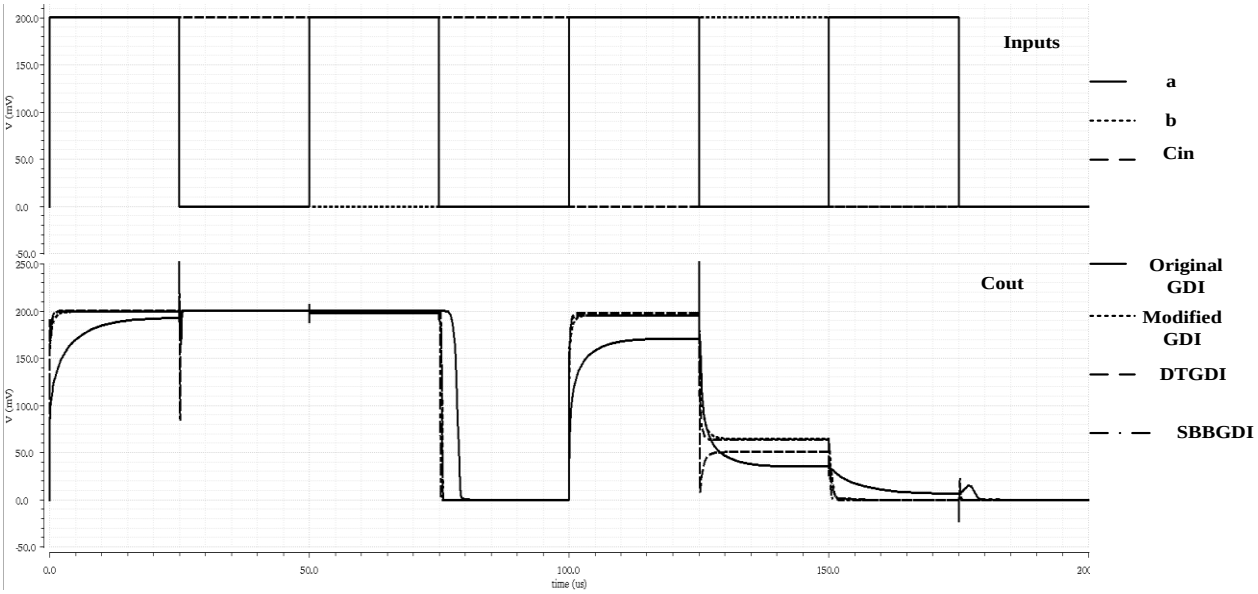


Figure 4. *Time evolution of output carry signal (Cout) for different GDI based full adder circuits*

3.1. Results and Comparitive Discussions

In this section, the results obtained from the simulation of full adder circuits designed using the proposed logic families DTGDI and SBBGDI are evaluated in comparison with the conventional C-CMOS, DT-CMOS, SBB-CMOS and GDI full adder circuit designs. To compare in common environment, all the full adder circuits are simulated using Cadence 45nm technology with a supply voltage of 0.2V and operating frequency of 20KHz.The values of Power, delay, Energy, and EDP of full adder circuits using different subthreshold logic families and the proposed logic families are presented in the table 5 for comparisons. For fair comparisons, the modified GDI based full adder circuit in figure 2(b) is chosen to represent GDI logic family. The transistors sizing has been made, such that minimum energy consumption is achieved.

With an aim to improve the performance characteristics of digital circuits in subthreshold region, the Energy Delay Product(EDP) and the Energy consumption, that is, the Power-Delay-Product (PDP) has been optimized with the proposed DTGDI and SBBGDI full adder designs. The comparison plots for EDP and energy metric of different full adders is shown in figure 5. The comparisons depict that the full adders designed using the proposed DTGDI and SBBGDI logic families outperform the C-CMOS, DT-CMOS, SBB-CMOS and GDI logic families in terms of energy and EDP metrics. The Energy and EDP savings obtained by the proposed designs with respect to the other designs is shown in figure 6. This is achieved by reducing the delay of the circuit. This delay in the proposed circuits is reduced mainly because of improved output swing using modified GDI adder circuit and by employing the Dynamic threshold (in DTGDI) and swapped body bias (in SBBGDI) schemes. The SBBGDI design shows better performance improvement when compared with the DTGDI. This is due to the constant forward bias application of SBB scheme.

Table. 5 *Simulation results for full adder cells using different subthreshold logic families in 45nm technology*

Designs	Average Power (pW)	Delay(μs)	PDP(aJ)	EDP (yJs)
C-CMOS	2.568	1.55	3.98	6.169
DT-CMOS	3.6	1.08	3.888	4.199
SBB-CMOS	4.785	0.69	3.301	2.278
GDI	3.797	0.7	2.657	1.86
DTGDI	4.02	0.58	2.331	1.352
SBBGDI	7.2	0.29	2.088	0.605

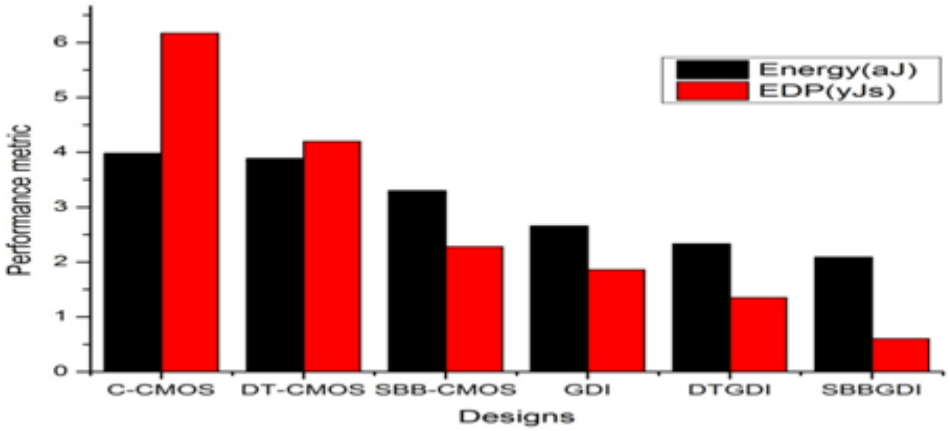


Figure 5. *Energy and EDP variations for full adder designs using different subthreshold logic families*

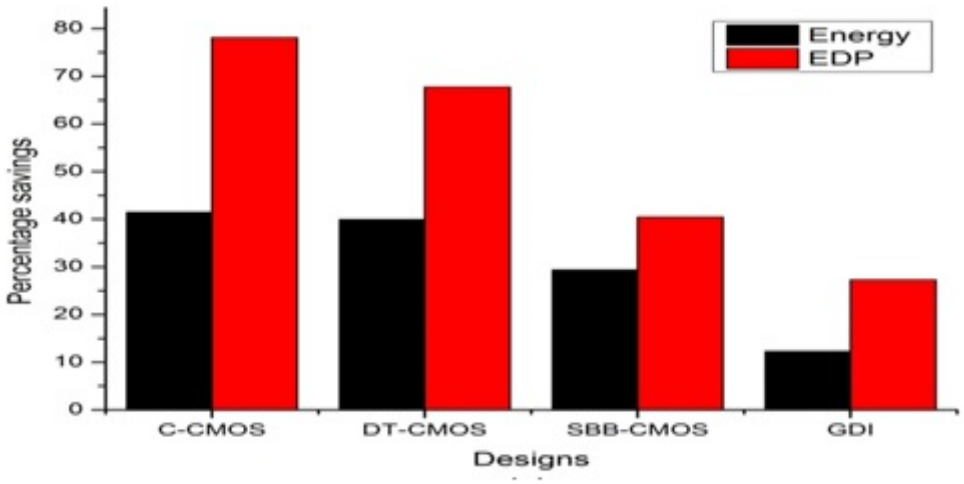


Figure 6. *PDP and EDP percentage savings of the proposed full adder designs*

Area of the proposed GDI based full adder circuits is calculated and is 4.982 μm^2, 6.891 μm^2 and 5.654 μm^2 for the GDI, DTGDI, and SBBGDI respectively. The layout designs of the proposed GDI based full adder circuits is shown in figure 7. It is found that the proposed GDI based full adder circuits achieved more than 67% area savings than the conventional CMOS adder design. Post layout simulations have also been performed and it is found that there is a negligible (less than 0.4% variation) effect of parasitic elements on the delay characteristics.

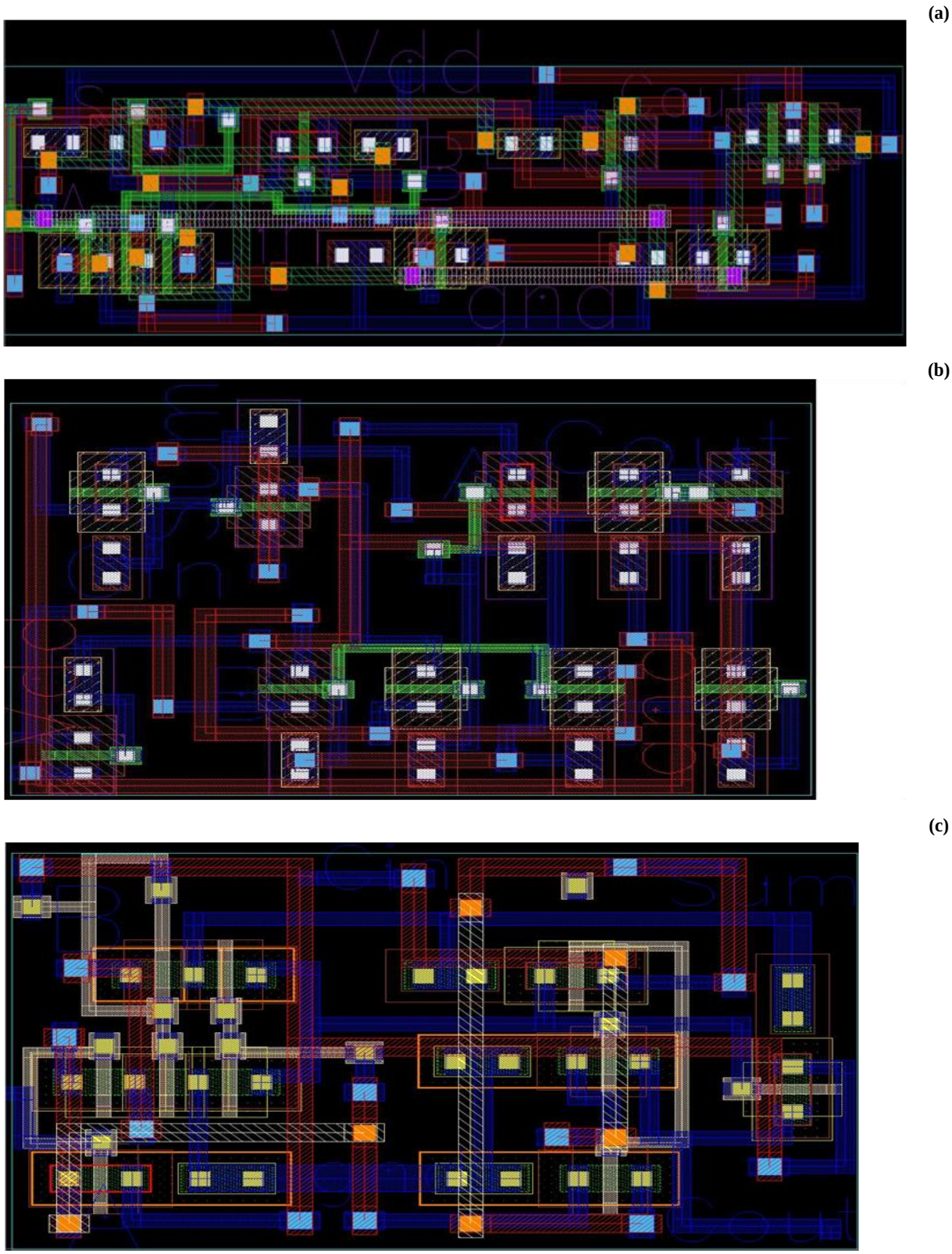
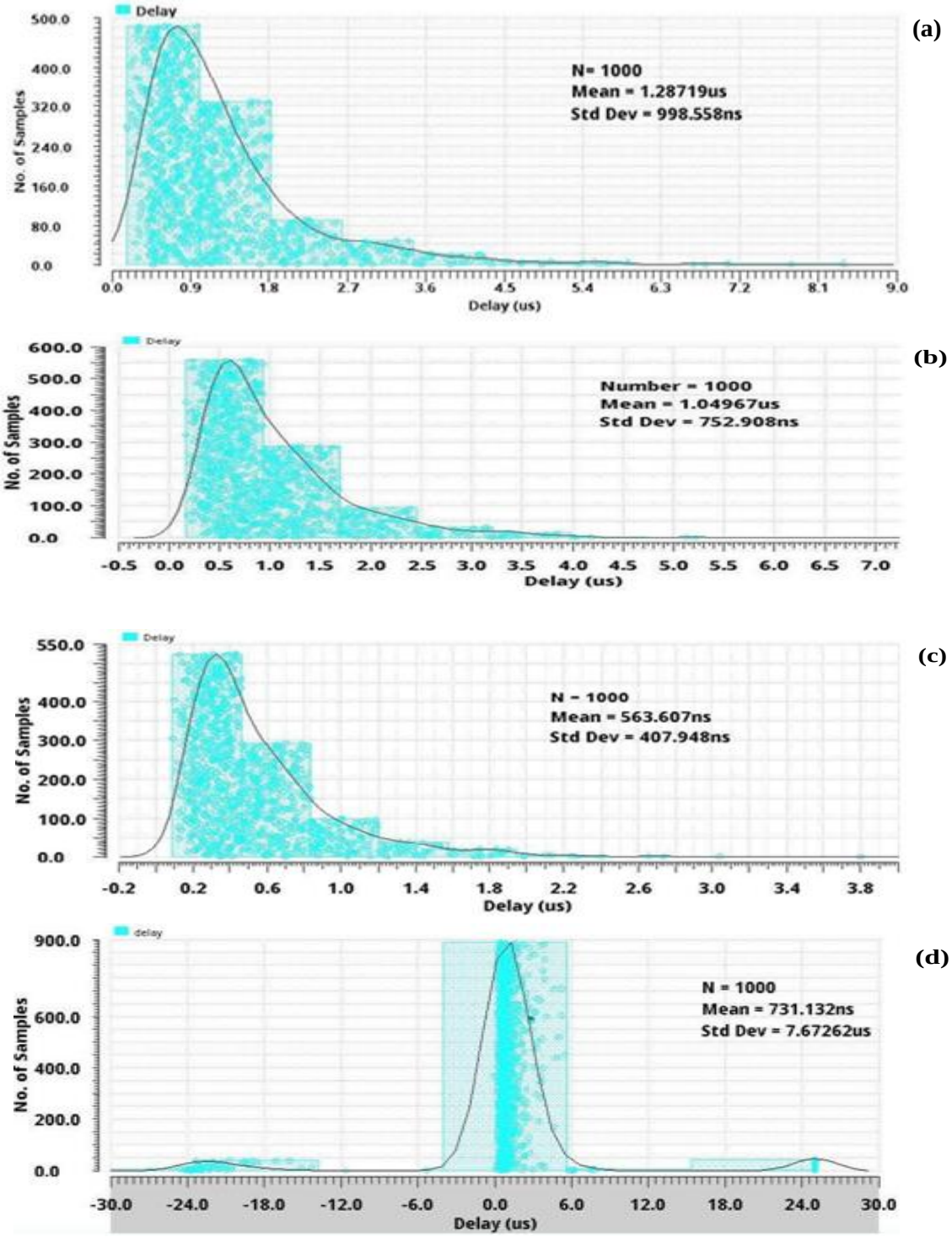


Figure 7. *Layout designs of GDI based 1-bit full adder circuits; a) GDI b)DTGDI c)SBBGDI*

In order to study the effect of local and global process variations on the delay of a critical path for the proposed full adder designs, Monte-Carlo simulations with 1000 samples for V_{DD} = 0.2V and T= 27^0C have been performed at TT process corner. Both the intradie and interdie fluctuations were considered for evaluating the robustness of the designs. The results are shown in the figure 8. As expected, the mean (μ)

value of the GDI based proposed designs is minimum when compared with the CMOS configurations, where DTGDI (σ =5.369) design have shown better immunity to process variations than the GDI design (σ =7.67) and the proposed SBBGDI design (σ =7.948).



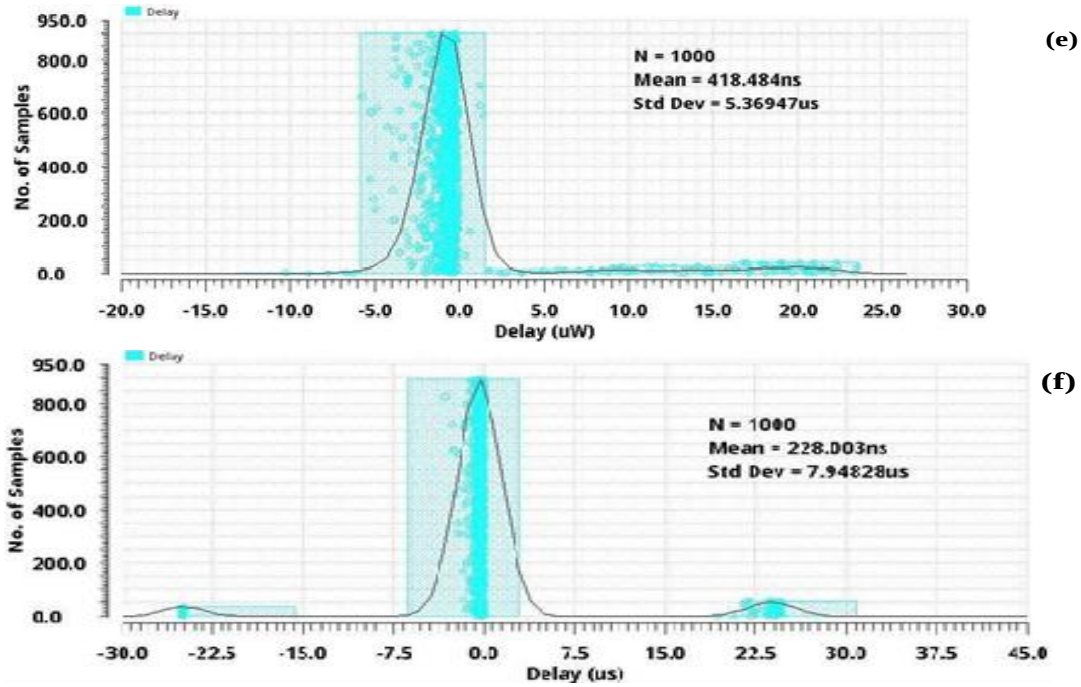


Figure 8. *Delay distribution of full adders derived by Monte-Carlo simulations; a) C-CMOS b) DT-CMOS c) SBB-CMOS d) GDI e) DTGDI f) SBBGDI*

4. CONCLUSIONS

GDI is one of the familiar logic family which allows realization of a wide range of complex logic In the recent years, GDI logic circuits are becoming more popular for area and energy efficient applications. However, it is challenging to operate the GDI circuits in subthreshold region for achieving ultra-low energy efficiency, where the degradation in the logic swing and speed are the major concerns. In this work, we proposed two new GDI logic families DTGDI and SBBGDI for improved logic swing and energy efficiency in the subthreshold region. The performance of these logic families is evaluated by designing a 1-bit full adder circuit using cadence 45nm technology with a supply voltage of 0.2V. The obtained results from the post layout simulations have shown significant improvements in terms of energy and EDP. The proposed DTGDI full adder circuit with layout area of only 6.891 μm^2 offers more than 12% energy savings and 27% savings in EDP when compared with its counter parts. Whereas, the SBBGDI full adder circuit with layout area of only 5.654 μm^2 offers more than 24% energy savings, 67% savings in EDP. Monte-Carlo simulations for 1000 samples reveal that the proposed designs are robust against local and global process variations with 100% yield.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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