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Effects of Frequency and Bias Voltage on Dielectric Properties and Electric Modulus of Au/$Bi_4Ti_3O_{12}$/n-Si (MFS) Capacitors

Araştırma Makalesi / Research Article

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ABSRACT

In this work, a metal-ferroelectric-semiconductor (MFS) type capacitor was fabricated and admittance measurements were held in a wide frequency range of 1 kHz-5 MHz at room temperature for the investigation of frequency and voltage dependence of complex dielectric constant, complex electric modulus and electrical conductivity of the MFS capacitor. Bismuth titanate ($Bi_4Ti_3O_{12}$) with high dielectric constant was used as interfacial ferroelectric material and the structure of MFS capacitor was obtained as Au/$Bi_4Ti_3O_{12}$/n-Si. Experimental results showed that dielectric, modulus and conductivity parameters are strong functions of frequency and voltage especially in depletion and accumulation regions due to the existence of surface states (N_{ss}), series resistance (R_s), interfacial polarization and interfacial layer. It was found that R_s of the structure and interfacial ferroelectric layer are efective in accumulation region whereas surface states (N_{ss}) and interfacial polarization are efective in depletion region. Also the changes in dielectric, modulus and conductivity parameters become considerably high particularly at low frequencies due to high values of R_s and N_{ss}. The observed anomalous peak in voltage dependent plots of capacitance and dielectric constant was atributed to the particular density distribution of N_{ss}, R_s and minority carrier injection. Moreover, the value of conductivity at low and intermediate frequencies is almost independent of frequency thus low frequency data was used to extract d.c. conductivity. This work showed that the use of high-dielectric $Bi_4Ti_3O_{12}$ as ferroelectric interfacial layer in a MFS capacitor is preferable due to high values of its dielectric constant compared with traditional insulator layer materials such as SiO_2 and SnO_2. Therefore, a MFS capacitor with $Bi_4Ti_3O_{12}$ interfacial layer can store more energy thanks to its high dielectric constant.

Keywords: MFS capacitors, frequency and voltage dependence, surface states and interfacial polarization, dielectric properties and electrical modulus.

1. INTRODUCTION

Electrical and dielectric properties of metal-semiconductor (MS) type structures with an insulator, polymer and ferroelectric interlayers are usually different from the ideal case of conventional MS structures especially due to barrier inhomogeneity and variations in the energy dependent surface states (N_{ss}) and concentration of doping atoms as a result of growing interlayer. Therefore, there has been a great effort for enhancing the performance metal-semiconductor (MS) structures by using interfacial materials with high dielectric constant such as TiO_2 [1-3] $Bi_3Ti_4O_{12}$ (BTO) [4,5], $BaTiO_3$ [6], (graphene-oxide-doped PrBaCoO nanoceramics) [7], (7% graphene doped-PVA) [8] and (Al_2O_3/Ga_2O_3(Gd_2O_3)) [9]. Among these various interlayer materials, ferroelectrics come forward since not only it provides high dielectric constant but also it is suitable for photodiode and non-volatile memory applications [10]. These device applications mostly utilize metal-ferroelectric-semiconductor (MFS) structures therefore the study of metal-ferroelectric-semiconductor (MFS) structures is important. During admittance measurements, MFS structures behave like a series combination of typical parallel plate capacitors in the high frequency limit. Therefore, charge storage ability of the capacitor also depends on the dielectric constant of the ferroelectric material. Therefore, the capacitance is given by $\varepsilon'\varepsilon_o A/d$ where ε' is dielectric constant, ε_o is permittivity of vacuum, A is capacitor area and d is the thickness of interfacial layer. Modifying the capacitance through changing the values of A and d is limited due to high space coverage and operating voltage in electronic devices [9,11], on the other hand charge storage ability of the capacitor is enhanced by using materials with high dielectric constant. It must also be noted that surface states (N_{ss}) with energies that correspond to forbidden band gap are formed in a way that they are in equilibrium with the semiconductor [12-15]. Nevertheless, the effect of N_{ss} is minimized by performing the admittance measurements at high frequencies.

When the thickness of interfacial ferroelectric layer is small, the device behaves like a typical Schottky barrier diode which could be utilized as photodiode, solar cell, and alike. However, when the thickness is sufficiently large, it becomes difficult for the charges on metal and semiconductor to exchange, hence the charge storage feature of the MFS structure comes forward, and therefore MFS structure basically behaves like a MFS capacitor which could be utilized in ferroelectric field effect transistors [16-19]. Like the other kinds of MS structures with various interlayer materials, the

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performance and reliability of a MFS structure are dependent of various factors/parameters such as the interfacial layer thickness, its homogeneity and dielectric constant, the process of surface preparation or fabrication procesess, doping concentration of donor or acceptor atoms (N_D or N_A), barrier formation at M/S interface and its homogeneity, density of N_{ss} or dislocations at interlayer/semiconductor interface, series resistance (R_s) of device, as well as measurement conditions such frequency of a.c. signal, applied bias voltage and device temperature [20-24].

The aim of this study is to investigate the effects of frequency and applied bias voltage on the dielectric properties, electric modulus and electrical conductivity of Au/$Bi_4Ti_3O_{12}$/n-Si (MFS) capacitors. For this purpose, admittance measurements were carried out in wide frequency (1 kHz-5 MHz) and bias voltage (±4V) ranges at room temperature. Obtained capacitance (C) and conductance (G) data were utilized for calculating dielectric, electric modulus and electrical conductivity parameters. Dependence of these parameters on frequency and bias voltage was clear. The bias voltage dependence was explained by the effects of R_s, N_{ss} and interfacial BTO layer whereas the frequency dependence was explained by Maxwell-Wagner polarization.

2. EXPERIMENTAL DETAILS

Au/$Bi_4Ti_3O_{12}$/n-Si (MFS) capacitor was fabricated using phosphor doped single crystal Si wafer with diameter of 3 inches, orientation of (111) and thickness of ~300 μm. Before the fabrication, n-Si wafer was cleaned in a mixture of a peroxide-ammoniac solution and then in H_2O+HCl solution for 10 min and then it was thoroughly rinsed in deionized-water with 18 MΩ cm resistivity in an using an ultrasonic bath for 15 minutes. After the cleaning process, the wafer was immediately taken into thermal evaporator in which highly pure (99.999%) Au metal was evaporated onto the whole back side of n-Si wafer at 10^{-6} Torr. Thus, 200 nm gold layer was grown on the wafer. However it needed to be annealed at 450 °C for 5 min in N_2 atmosphere to get an ohmic contact with low resistivity by sintering the Au layer. After the formation of ohmic contact, $Bi_4Ti_3O_{12}$ ferroelectric interfacial layer was deposited on the front side of n-Si wafer by RF magnetron sputtering using a hot compacting of $Bi_4Ti_3O_{12}$ powder of a stoichiometric composition as a target material. The mixture of argon (Ar) and oxygen (O_2) was used as working medium and the substrate was kept at 650 °C. Thickness of the deposited BTO layer was measured with Veeco Dektak 6 M thickness profilometer as 540 nm. Finally, circle-shaped pure Au (99.999%) front contacts with diameter of 1 mm were deposited through same thermal evaporation system and conditions. Thus, 200 nm gold layer was grown on BTO layer so that the fabrication of MFS capacitor is completed. In order to perform admittance measurements, the fabricated Au/$Bi_4Ti_3O_{12}$/n-Si (MFS) capacitor was mounted on a copper holder with the help of silver dag and later the electrical contact with one of the front contacts was ensured by the use of thin silver coated Cu wires with the help of silver paste. C-V-f and G/ω-V-f data was obtained by using a HP4192A LF impedance analyzer between –4 V and +4 V at room temperature. During the measurements, the MFS capacitor was applied with a small a.c. test signal of 40 mV_{rms} in a wide frequency range of 1 kHz and 5 MHz. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. RESULT AND DISCUSSION

Admittance spectroscopy has proven to be an efficient tool for characterizing electrical parameters such as traps, series resistance, doping concentration, barrier height, depletion width and dielectric parameters of Schottky barrier diodes (SBDs) and capacitors of the similar heterostructure. For this purpose, admittance measurements were held in a wide frequency and/or temperature range. Figure 1 (a) and (b) show C-V and G/ω-V plots of Au/$Bi_4Ti_3O_{12}$/n-Si capacitor, respectively.

These plots clearly exhibit inversion, depletion and accumulation regions just like a typical SBD. There is a peak behavior just after the depletion region for C-V curves at low frequencies and then the capacitance value drops rapidly particularly for the data measured at 1 kHz. Such peak behavior is common for the structures that has interfacial layer of insulator type. On the other hand, the decrease after the peak is stronger at low frequencies because of R_s of the capacitor. Another reason of peak

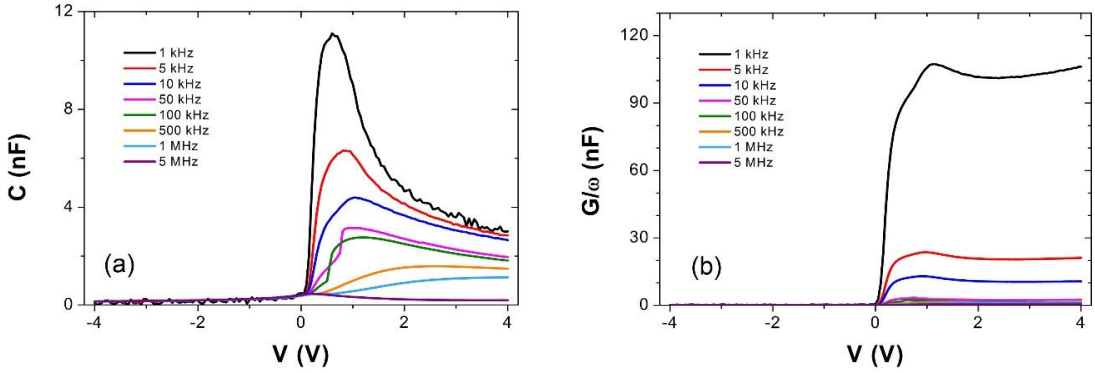

Figure 1. (a) C-V and (b) G/ω-V plots of the MFS capacitor at different frequencies.

behavior at low frequencies is due to the effect of N_{ss} because excess capacitance and conductance is yielded for admittance data measured at low frequencies. This effect also shows itself in G/ω-V plots such that higher conductance values are obtained at low frequencies due to the contribution of excess conductance formed by N_{ss}. The effects of R_s and N_{ss} on capacitance and conductance is important since dielectric parameters are calculated using the measured capacitance and conductance values. This is also because the applied bias on the semiconductor device is shared by R_s, N_{ss} and interfacial layer. However, while the value of R_s on the C-V and G/w-V is effective only the accumulation region, surface states (N_{ss}) are effective both in inversion and depletion regions. When the life time of surface states is lower than the period (T), the charges at surface states can easily follow the external ac signal and yield an excess capacitance and conductance to their measured value. Therefore, this effect becomes more effective in the low and intermediate frequency regions (T=1/f) and at enough high frequencies (f≥500 kHz) the effect of N_{ss} can be neglegted low. Because, the life time of surface states (τ) at high frequencies becomes higher than T. Nicollian and Brew suggested that real part of impedance in the high accumulation region yields R_s, thus R_s values were calculated using the equation below [21];

$$R_s = \frac{G}{G^2 + \omega^2 C^2}$$

In addition, Fonash's method [25] was utilized for the calculation of N_{ss} values which can be calculated by the following equation;

$$\alpha = \frac{qdN_{ss}}{\varepsilon_i}$$

where ε_i is dielectric constant of insulating BTO layer, q is electronic charge, d is the thickness of insulating BTO layer and α is a parameter given by $(1-c_2)/c_2$ where c_2 corresponds to the ratio of experimental value of doping concentration to its theoretical value ($7{,}837 \times 10^{16}$ cm^{-3}) such that the experimental value can be extracted from the slope of C^{-2}-V curves [4]. Figure 2 shows frequency dependence of N_{ss} and R_s of $Au/Bi_4Ti_3O_{12}/n\text{-}Si$ capacitor. As previously discussed, N_{ss} values decrease with increasing frequency. As the frequency of a.c. signal is increased, period of the signal gets smaller and after some point it becomes smaller than the time constant of interface states. Therefore, interface states cannot follow the a.c. signal and contribution of excess capacitance is minimized. R_s values also decrease with increasing frequency in consistency with the increasing conductance values with increasing frequency.

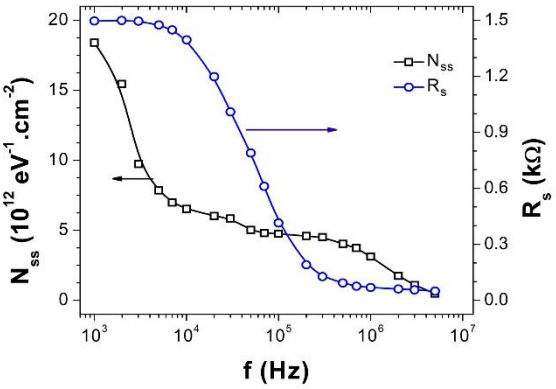

Figure 2. Frequency dependence of N_{ss} and R_s of the MFS capacitor.

It is well known that permittivity (ε*) consists of real and imaginary parts such that it is equal to ε'-iε" where ε' is a measure of the capacitor's ability to store charge and ε" is associated with the energy dissipation, and they are referred as dielectric constant and dielectric loss, respectively. These parameters are calculated on the basis that fabricated MFS device is literally a combination of parallel plate capacitor, thus dielectric constant and dielectric loss are obtained by using the following equations [1,2,3,5,7,8];

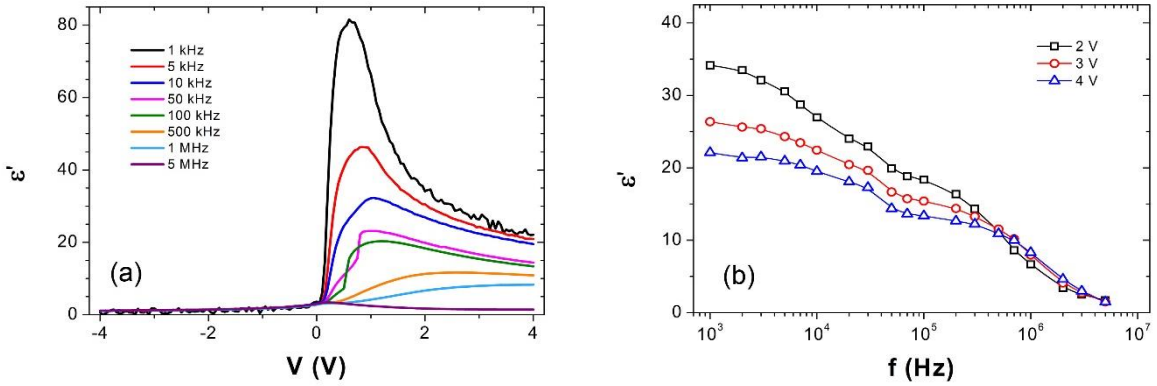

Figure 3. (a) ε'-V and (b) ε'-f plots of the MFS capacitor.

$$\varepsilon' = \frac{C}{C_o}$$

$$\varepsilon'' = \frac{G}{\omega C_o}$$

Here C_o is the capacitance of empty capacitor and equals to $\varepsilon_o A/d$ where ε_o is permittivity of vacuum (8.85×10^{-14} F/cm) and A is the area of front contact. Bias voltage and

frequency dependent plots of dielectric constant of $Au/Bi_4Ti_3O_{12}/n$-Si (MFS) capacitor is given in Figure 3 (a) and (b) respectively. Similarly, bias voltage and frequency dependent plots of dielectric loss of the MFS capacitor are given in Figure 4 (a) and (b), respectively.

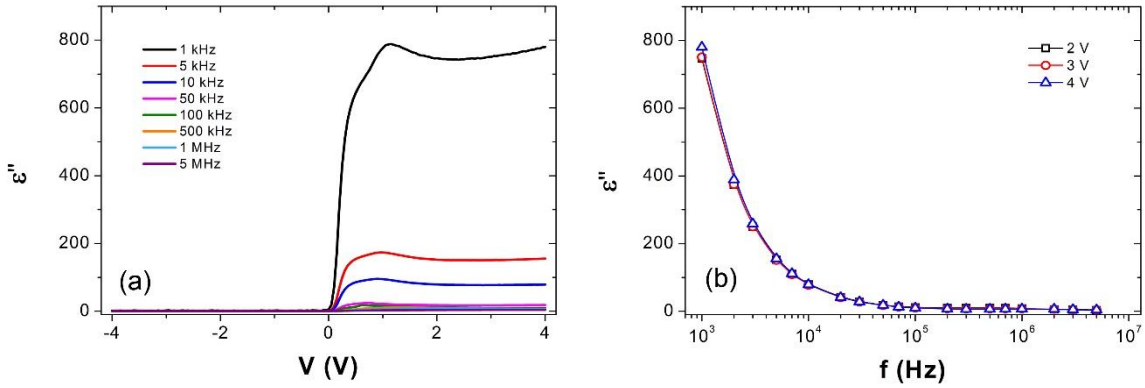

Figure 4. (a) ε"-V and (b) ε"-f plots of the MFS capacitor.

Voltage dependence of these dielectric parameters resembles to that of admittance data. Therefore similar peak behavior is observed at low frequencies due to high values of R_s and N_{ss}. In Figure 3 (b) and Figure 4 (b), it is clear that ε' and ε" decrease with increasing frequency. ε' also shows strength of polarization in the studied material. It is well known that polarization is comprised of interfacial polarization, dipolar polarization, ionic polarization and electronic polarization. Last three polarization types exist in the whole frequency range of a.c. signal of applied to the MFS capacitor. However, contribution of interfacial polarization, which is also called as Maxwell-Wagner polarization, to total polarization disappears as the frequency goes up to MHz level. Therefore, we observe a gradual decrease in ε' values with increasing frequency. On the other hand, there is a rapid decrease for ε" values with no sign of relaxation. Nevertheless, it might be masked due to conductivity of the MFS capacitor, hence dielectric properties of $Au/Bi_4Ti_3O_{12}/n$-Si (MFS) capacitor are further explored using electric modulus (M*) approach. The relation between permittivity and electric modulus is that the latter is reciprocal of the former, i.e. $M^*=1/\varepsilon^*$ [1,2,3,5,7,8], therefore real and imaginary parts of electric modulus are calculated using the following equation;

$$M^* = M' + iM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + i\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2}$$

Figure 5 (a) and (b) show bias voltage and frequency dependent plots of M', and same plots of M" are shown in Figure 6 (a) and (b), respectively. The reciprocal behavior of modulus plots is particularly clear for the frequency dependent plots. The increase in there parameters with increasing frequency is already expected for this reason. Besides, M"-f plots reveal peaks as can be seen in inset of Figure 6 (b). Such peak behavior of M" data is associated with the relaxation of the sample. Therefore, it can be said that relaxation frequency of the sample is around 70 kHz.

When the MFS capacitor is applied with a.c. signal, its electrical conductivity is referred as a.c. conductivity (σ_{ac}). The values of σ_{ac} were calculated using the equation $\sigma_{ac}= \omega\varepsilon''\varepsilon_o$ [1,2,3,5,7,8] and its bias voltage dependence is given in Figure 7 (a). The MFS capacitor yields much larger conductivity values in the forward bias region compared to reverse bias region because the MFS

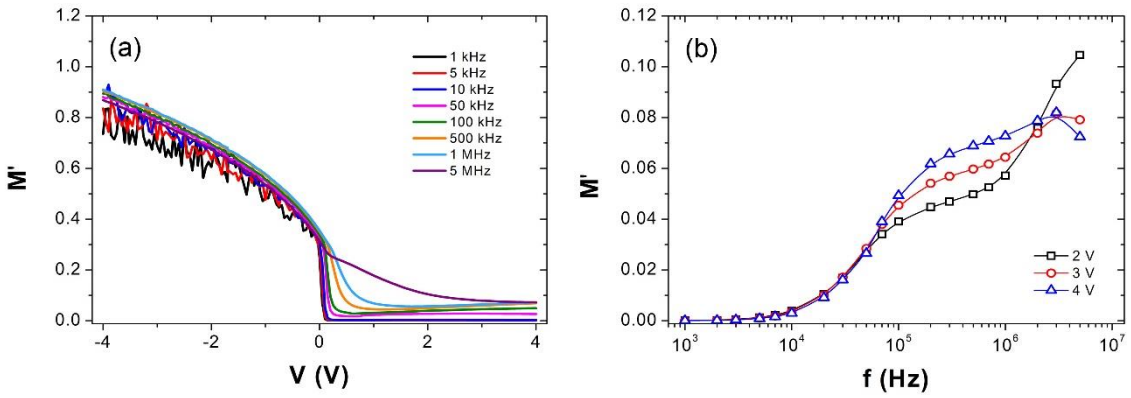

Figure 5. (a) M'-V and (b) M'-f plots of the MFS capacitor.

capacitor is in the form of a Schottky barrier diode. Figure 7 (b) shows frequency dependence of σ_{ac}.

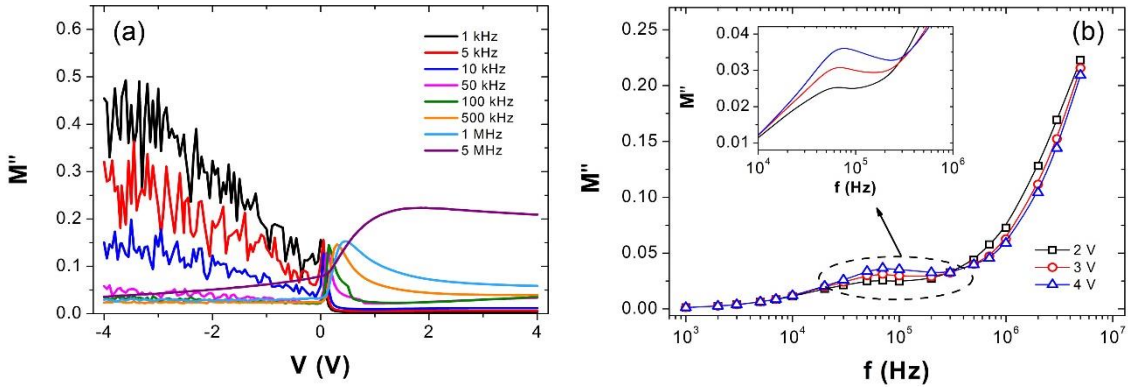

Figure 6. (a) M"-V and (b) M"-f plots of the MFS capacitor.

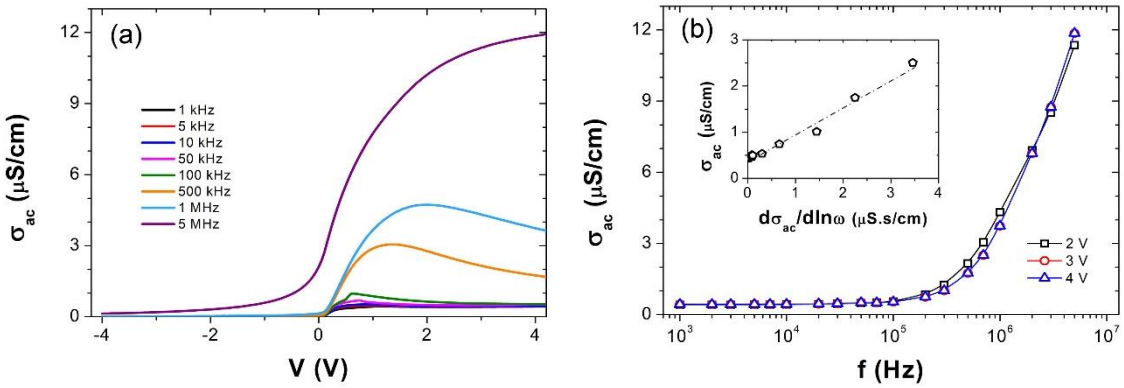

Figure 7. (a) σ_{ac}-V and (b) σ_{ac}-f plots of the MFS capacitor. The inset shows the $\sigma_{ac} - d\sigma_{ac}/d\ln\omega$ plot.

It is seen that σ_{ac}-f plots increase gradually up to 0.1 MHz, then they increase rapidly. The increase in σ_{ac} with increasing frequency leads to an increase in eddy current and this is consistent with the decreasing strength of series resistance with frequency (Figure 2). σ_{ac} is a combination of capacitor's d.c. conductivity (σ_{dc}) and conductivity contribution due to a.c. signal, and its frequency dependence is expressed by the following equation [1,2,3,5,7,8];

$$\sigma_{ac} = \sigma_{dc} + A\omega^{s}$$

where A is a constant and s is a parameter that shows the strength of frequency dependence. Another expression of frequency dependence of σ_{ac} is as below [5];

$$\sigma_{ac} = \sigma_{dc} + \frac{1}{s}\frac{d\sigma_{ac}}{d\ln\omega}$$

Inset of Figure 7 (b) shows σ_{ac}–$d\sigma_{ac}/d\ln\omega$ plot whose y-intercept corresponds to σ_{dc}. Thus, σ_{dc} of the MFS capacitor was extracted as $4.1\text{x}10^{-7}$ S/cm. This value might look small, however it is reasonable considering the thickness of BTO interlayer.

4. CONCLUSION

The fabricated Au/$Bi_4Ti_3O_{12}$/n-Si MFS capacitor yielded high values of capacitance and conductance particularly at low frequencies. This was explained by the excess capacitance and conductance due to interface states. Interface states and series resistance were the reasons of peak behavior in C-V and G/ω-V plots. When these two parameters were calculated, it was seen that they decrease with increasing frequency. Similar effect was also seen in dielectric constant and dielectric loss such that they decrease as the frequency is increased because interface states can no longer follow a.c. signal since lifetime of traps is larger than inverse of angular frequency. Dielectric constant at 1 kHz is around 20s in the high accumulation region. Modulus formalism was utilized to explore relaxation behavior of the capacitor and it was found that relaxation occurs around ~70 kHz. Moreover, investigation of a.c. conductivity in the low frequency region revealed a d.c. conductivity value of $4.1\text{x}10^{-7}$ S/cm. Overall, the usage of BTO interfacial layer is preferable due to high value of dielectric constant because it allows storing more energy and enchance capacitor's ability.

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