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A MULTI-INPUT MULTI-OUTPUT ENERGY HARVESTING ARCHITECTURE FOR MICROBIAL FUEL CELL

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ABSTRACT

This paper presents an energy harvesting architecture that accommodates two microbial energy sources and delivers power supply synchronously to two loads. The proposed architecture enables the maximum power extraction from the first energy source, whereas the second source is disabled. However, once the first energy source is impaired (i.e., not working), the second energy source becomes the primary energy source in the architecture, and the first energy source is decoupled from the system. The measurement result of the proposed architecture, implemented with the off-the-shelf components and tested with two emulated MFCs, demonstrates a peak efficiency of 56.51%, which is the highest end-to-end efficiency among prior work. The proposed architecture can operate from a minimum input voltage of 0.3 V and simultaneously regulate two outputs to constant voltages of nearly 3.7 V and 5 V.

Keywords: Burst mode, Energy combiner, Energy harvesting, Energy scavenging, Microbial fuel cell, Multiple input, Multiple loads, Underwater electronic devices, Wireless sensor networks

1 INTRODUCTION

Microbial fuel cells (MFCs) are considered an emerging alternative energy source for underwater electronic devices (e.g., hydrophones) [1], [2]. MFCs have a significant potential to deploy in deep oceans, seas, lakes, and rivers in the harsh aquatic environment [2]-[5]. MFCs generate energy from biodegradable substrates through the metabolic activities of microorganisms in marine sediment [6]. Typically, MFCs contain two electrodes: an anode

buried in sediment and a cathode floating in water. Microbial activity in the marine sediment causes a potential difference between electrodes. Thus, MFCs generate electrical energy.

MFCs are generally not sufficient to directly drive electronic devices (e.g., sensors) since the voltage and power generated by MFCs are inherently at low levels [1]-[18]. Thus, an energy harvesting system that boosts the low voltage is needed along with a temporary storage element (e.g., supercapacitor) for accumulating the harvested energy over time to intermittently transfer to the load (i.e., burst mode operation). This type of load can be classified as a heavy load, which requires more power than the generated power by the energy source.

However, the energy available from a single microbial fuel cell might not be secured to power the load due to the issue of bioturbation by diverse aquatic organisms [3], [7], [11], [18]-[20]. In other words, the anode of the MFC can be impaired by either burrowing organism [7] or incomplete installation [5], [17], thereby allowing dissolved oxygen in water to contact the anode that becomes the cathode. Thus, the potential difference across the electrodes is eliminated, and the MFC becomes short-circuited without producing any useful voltage and power at the output. In order to increase the reliability of the microbial energy source, it is possible to construct the energy harvesting system with multiple MFCs [14], [17], [18], [20].

Prior work in multi-input energy harvesting systems for MFCs has involved combining the outputs of the individual power converters for each MFC to a common output capacitor and transferring its power to the load [13], [14], [17], [20]. However, these works have a large area overhead, resulting in complexity and large power losses. As a result, they have low overall efficiencies (e.g., $\leq 32.8\%$). To further improve the complexity and efficiency, adding the output voltages of the MFCs through switches to supply a single inductor power converter is proposed in prior work [18]. However, the work utilizes all MFCs at the same time; thus, all MFCs are not isolated from each other. Also, the MFC with the highest output voltage constrains the contributions from other MFCs. Thus, all MFCs do not exploit their best efficiencies, thereby degrading the overall efficiency. Also, these works do not consider the regulation of multiple output loads. Thus, there is a need for a more efficient architecture for multi-input energy harvesting systems with multi-output regulation.

This paper presents an energy harvesting architecture. The architecture handles energy from two emulated MFCs and provides efficient regulation of two output loads. One MFC is allowed merely to support the loads by the architecture, but the other MFC stays at the idle mode (i.e., not utilized). This leads to full isolation among MFCs. As a result, the overall

efficiency degradation is reduced or eliminated in the system. Once the first MFC is impaired, the architecture allows the second MFC to supply the loads. Thus, the energy path to the loads is maintained with the spare MFC, i.e., MFC 2. The architecture can start the operation from the minimum input voltage of 0.3 V and regulate two outputs to voltage levels of roughly 3.7 V and 5 V. The architecture implemented with discrete components, accomplishes a peak efficiency of 56.51%. As compared to prior multiple MFC works, the architecture achieves the highest end-to-end efficiency, supports multiple loads with regulated voltages, and secures full isolation between sources.

2 THE PROPOSED ARCHITECTURE

Figure 1 shows the top-level architecture of the proposed architecture, which consists of four power switches, a low voltage step-up converter (e.g., $V_{in} \geq 0.3$ V), a high voltage boost converter (e.g., $V_{dc} \leq 3.7$ V), and a temporary storage element (e.g., C_{STOR}=235 mF). The architecture does not require any precharge voltage to start the system operation; thus, the voltage in all capacitors is initially equal to zero.

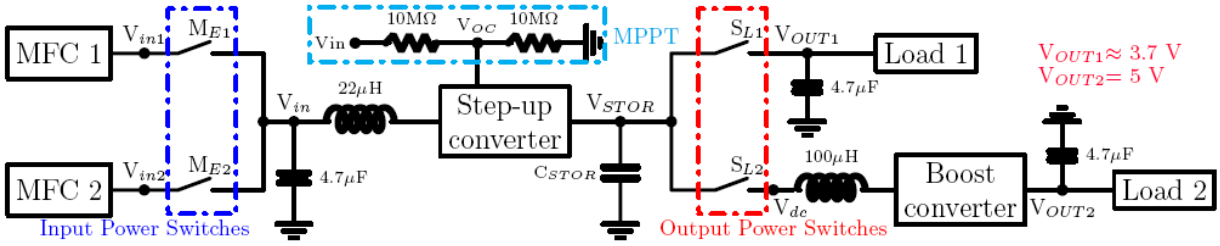

Figure 1. Block diagram of the proposed architecture.

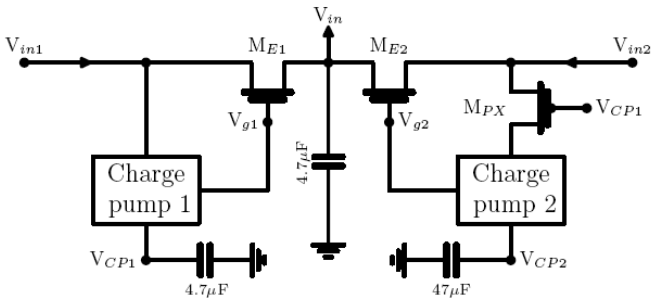

Figure 2. The input detecting circuit (IDC).

Two MFCs are enabled to provide voltage to their outputs (V_{in1}-V_{in2}), but input power switches (M_{E1}-M_{E2}) block these voltages to supply the V_{in} node. In order to allow the available power from the MFCs to transfer to the step-up converter, an input detecting circuit (IDC) is needed, as shown in Figure 2. The MFCs provide a power supply to charge pumps to charge

capacitors at the V_{CP1} and V_{CP2} nodes from 0 V. Once the V_{CP1} node reaches 0.4 V, the M_{PX} PMOS transistor turns off, which was on. Thus, the charge pump 2 is decoupled from the output of the MFC 2, V_{in2}, and the capacitor at the V_{CP2} node stops charging. As a result, the voltage at the V_{in2} node becomes the open-circuit voltage of the MFC 2. However, the MFC 1 keeps supplying the charge pump 1 to charge. Once the voltage at the V_{CP1} node reaches 2 V, the charge pump internally connects the V_{CP1} node to the V_{g1} node, which is the gate of the M_{E1} NMOS transistor. Consequently, the M_{E1} transistor turns on, and the energy available from the MFC 1 is transferred to the V_{in} node, which is isolated from the MFC 2. With the IDC, the energy sources are fully isolated from each other.

However, once the MFC 1 is impaired, the output V_{in1} drops to zero or an insufficient voltage level. Thus, the charge pump 1 stops to charge the capacitor at the V_{CP1}, and the capacitor voltage is not delivered internally to the V_{g1} node. As a result, the M_{E1} transistor shuts off, and the energy transfer from the MFC 1 to the step-up converter is cut-off. Meantime, due to the small value of the capacitor at the V_{CP1} node, the energy at the capacitor is consumed internally; consequently, it drops to nearly zero. This causes the M_{PX} transistor to switch on, and the MFC 2 starts to supply the charge pump 2. Once the capacitor at the V_{CP2} node charges to 2 V, the energy at the capacitor releases to the gate of the M_{E2} transistor. As a result, the transistor turns on, and the MFC 2 starts to provide a power supply to the converter. This is precisely what the IDC detects: the MFC 2 as the energy source once the MFC 1 is not functional to supply the converter.

The step-up converter receives power supply from the IDC output V_{in} to up-convert to higher voltage levels to charge a supercapacitor at the V_{STOR} node. When the V_{STOR} reaches 1.8 V, the converter internally enables the maximum power point tracking (MPPT), which drives the maximum power available from the MFC. The V_{OC} pin of the converter is placed at the output of the voltage divider of the V_{in} node in order to achieve the MPPT. After this voltage level (e.g., 1.8 V), the supercapacitor keeps charging at a faster rate. Once the V_{STOR} arrives at nearly 3.7 V, which is the maximum voltage level for the supercapacitor to charge in this study, the accumulated energy should be released to two output loads. Thus, there is a need for a circuit between the loads and the supercapacitor to manage the charge transfer.

Figure 3 shows the circuit used for controlling the outputs. Before the accumulated energy at the supercapacitor is transferred to the loads, the Nx transistor shuts on. This is because resistors of 1 and 6.7 MΩ placed between the V_{STOR} and V_{GL} nodes behave as a linear element to supply current to the gates of the S_{L1}, $S_{L2,}$ and Nx transistors. Thus, the diode between

the V_{x1} and the V_{x2} nodes is bypassed. The voltage at the V_{STOR} node goes across four diodes to charge the capacitor of 4.7 µF at the V_{cntrl} node. A comparator circuit is an interface between the V_{cntrl} and OUT nodes. The comparator circuit compares internally a divided version of the V_{cntrl} node with the internally generated reference voltage (V_{ref}).

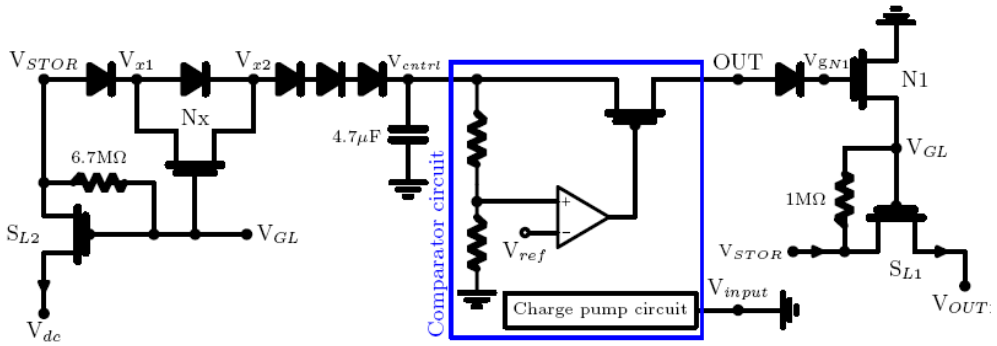

Figure 3. Output control circuit (OCC).

Once the V_{STOR} node is charged to nearly 3.7 V which drops over diodes to charge the capacitor at the V_{cntrl} node to 2 V, the comparator energizes the gate of the PMOS transistor. As a result, the PMOS switches on, which was cut-off, and the V_{cntrl} node is at the same potential as the OUT node. The OUT voltage goes across the diode to supply the gate of the N1 transistor (Vg_{N1}). In consequence, the N1 turns on, and the V_{GL} node drops to zero. Thus, the S_{L1}, $S_{L2,}$ and Nx transistors turn on, on, and off, respectively. The stored energy is transferred to Load 1 and the V_{dc} node, and the diode between the V_{x1} and V_{x2} nodes becomes conducting. The load 1 receives a power supply with a voltage level of approximately 3.7 V.

Due to shutting off the Nx transistor, the voltage at the V_{cntrl} node undergoes a decrease with the amount equal to the voltage drop across the corresponding diode, and the V_{cntrl} voltage drops from 2 V to 1.5 V. Both load 1 and load 2 receive power supply from the supercapacitor. Thus, the supercapacitor starts discharging, and the capacitor at the V_{cntrl} node discharges as well. Once the V_{cntrl} voltage reduces to 1.44 V, the comparator circuit internally shuts off the internal PMOS. This step leads to the isolation between the V_{cntrl} and OUT nodes. As a result, the OUT voltage drops to zero, and the N1 transistor switches off, and the V_{GL} voltage shifts from 0V to nearly V_{STOR} voltage. This causes the S_{L1}, $S_{L2,}$ and Nx transistors turns off, off and on, respectively. Therefore, the supercapacitor is disconnected from the loads and starts charging back to 3.7 V again. The same operation process will occur over time for the loads operating in burst mode. This is precisely what the control circuit carries out.

Once the supercapacitor transfers the energy to loads, the load 1 is at the voltage level of 3.7 V while load 2 is at 5 V. For load 1, there is no need for another stage to boost the voltage since the V_{OUT1} node is at the same potential as the V_{STOR} node. However, load 2 requires a second converter placed between the S_{L2} transistor and the V_{OUT2} node to step up the voltage from 3.7 V to 5 V. The output voltage levels of the proposed architecture can be adjusted by adding/subtracting more diodes to the output control circuit or rearranging the boost converter. Table 1 tabulates off-the-shelf components used in the architecture.

Table 1. List of discrete components used to construct the architecture.

Component	Name	Specifications
Input detecting circuit		
Charge pump	S-8880A20	min. input voltage=0.3 V
M_{E1} & M_{E2} NMOS	BSH103	$V_{GS(th)}$=0.4 V
M_{PX} PMOS	SI-3499DV	$V_{GS(th)}$=-0.35 V
Outputs control circuit		
Comparator circuit	S-8880A20	Input connected to gnd
N_X & N1 NMOS	SI-3460BDV	$V_{GS(th)}$=0.45 V
S_{L1} & S_{L2} PMOS	SI-3499DV	$V_{GS(th)}$=-0.35 V
Diodes	1N4007	Drop voltage
Converters		
Step-up converter	BQ25505	min. input voltage=0.1 V
Boost converter	L6920DB	min. input voltage=0.8 V
Supercapacitor	235mF	ESR=8Ω

3 MEASUREMENT RESULTS

The proposed architecture is implemented using off-the-shelf components. The experimental setup of the architecture is shown in Figure 4. The architecture harvests energy from two MFCs while regulating two different output voltage levels, which are nearly 3.7 V and 5 V. MFC can be electrically modelled as a voltage source in series with a resistance [12]. Voltage sources with series resistors are used to model the MFC 1 and MFC 2 for testing. The MFC 1 is emulated as a voltage source of 0.8 V in series with a resistor of 0.1 kΩ, and the MFC 2 is modeled as a 0.7 V input voltage in series with a 0.2 kΩ internal resistor.

Figure 5 shows the operation of the architecture from the initial time to several cycles. Two functional MFCs provide power supply to the architecture; however, the architecture receives energy from MFC 1, but MFC 2 is not allowed to support the architecture, and it becomes an open-circuit. The supercapacitor voltage (V_{STOR}) begins to rise from 0 V. Once the

V_{STOR} exceeds 1.8 V, the step-up converter triggers the MPPT accomplished by regulating the converter input as half of the open-circuit voltage of MFC 1. After that, it is obviously seen that the supercapacitor has charged at a faster rate than before. Once the V_{STOR} voltage gets to 3.7 V, both the S_{L1} and S_{L2} turn on, and both loads, thus, start receiving power supply. Once the MFC 1 is impaired ($V_{in1} \approx 0$), the backup source (i.e., the MFC 2) should deliver energy to the architecture to maintain the load operations. It can be seen from Figure 4 that the MFC 2 does not start immediately providing power to the architecture. This is because the voltage of the capacitor at the V_{CP1} in the IDC does not drop instantly to below the threshold voltage of the M_{PX} PMOS transistor. Once the V_{CP1} drops to the below the transistor threshold voltage, the transistor switches on and, consequently, the MFC 2 is allowed to supply the circuit. Thus, the voltage of the MFC 2 V_{in2} shifts from the open-circuit voltage to nearly half of the open-circuit voltage of the MFC 2, which is equal to the voltage at the V_{in}.

Figure 6 shows voltage waveforms at the V_{in1}, V_{in2}, V_{CP1}, and V_{CP2} nodes in Figure 2. Once the impairment occurs at MFC 1, the input voltage V_{in1} begins reducing to zero due to shutting off the M_{E1} transistor. Also, the charge pump 1 does not charge up, and the capacitor voltage V_{CP1} starts todrop. Once the capacitor voltage reaches roughly 0.35 V, the M_{PX} transistor turns on and the MFC 2 starts the operation of the charge pump 2 to charge the capacitor at the V_{CP2} node. As the V_{CP2} reaches 2 V, the M_{E2} transistor turns on, and MFC 2 is connected to the step-up converter. These results demonstrate that the energy path to the architecture is secured with the backup source (i.e., the MFC 2).

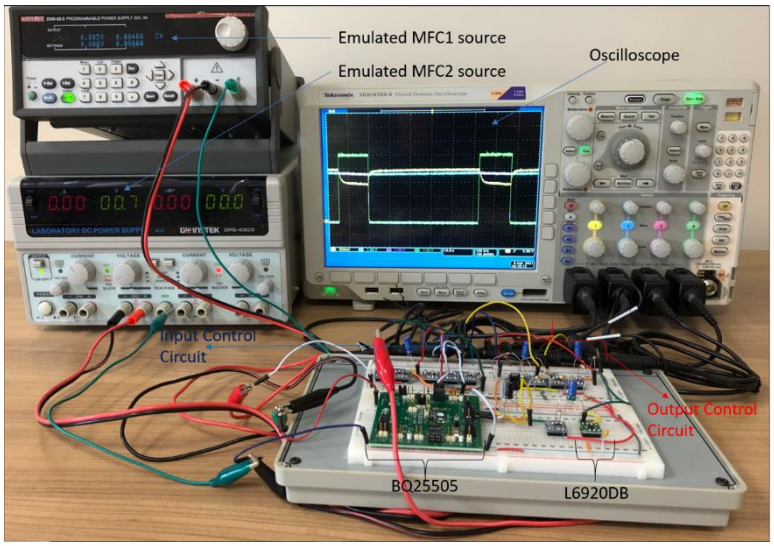

Figure 4. Experimental setup of the proposed architecture.

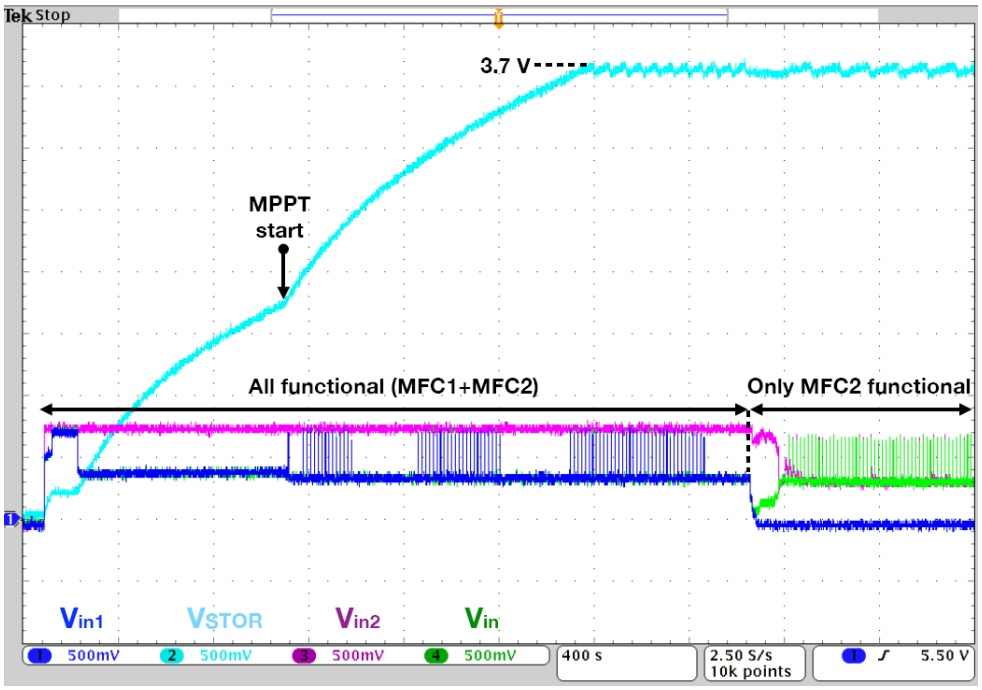

Figure 5. The operation from the initial time without impaired MFCs and once MFC 1 is impaired.

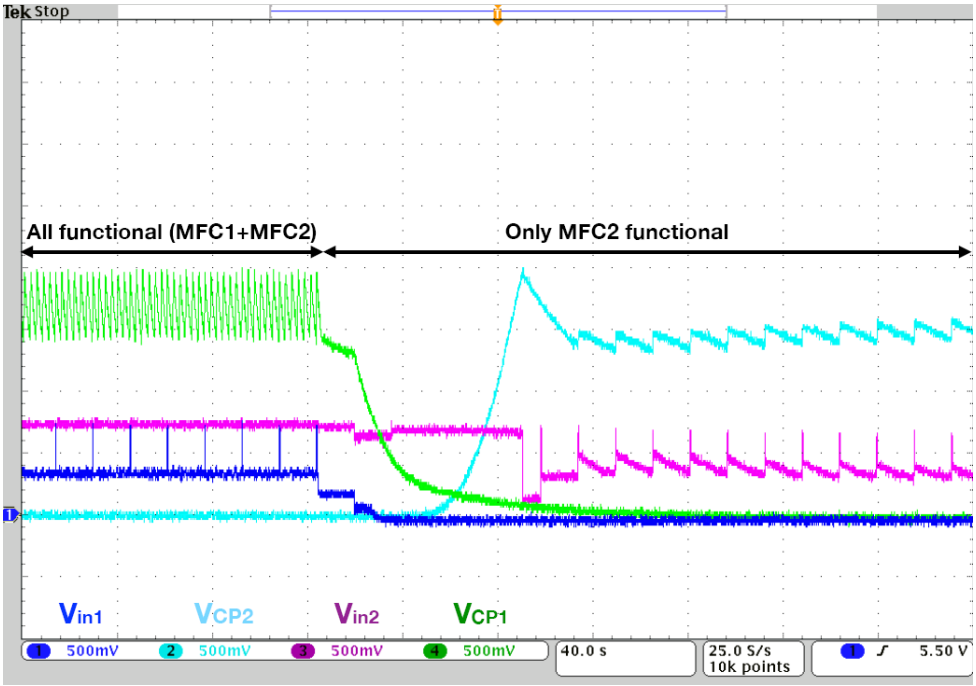

Figure 6. Voltage waveforms at the V_{in1}, V_{in2}, V_{CP1}, V_{CP2} nodes for the IDC once MFC 1 is impaired.

In order to verify the operation of the boost converter, voltage waveforms at the V_{dc}, V_{cntrl}, V_{GL}, and V_{OUT2} are monitored, as illustrated in Figure 7. Before the V_{cntrl} voltage arrives at 2 V, the voltages of the input (V_{dc}) and output of the boost converter are equal to zero. This is because output power switches (S_{L1}-S_{L2}) are kept being in off status by the resistors located

between the V_{STOR} and V_{GL} nodes. The resistors act as a short-circuit to energize the common gate of the transistors V_{GL} that is almost at the same potential as the V_{STOR} node. Once the V_{cntrl} voltage charges to 2 V, the common gate voltage V_{GL} drops to zero. Therefore, the S_{L2} transistor turns on, and consequently, the boost converter is bridged to the supercapacitor. Voltages of the input (V_{dc}) and output of the boost converter (V_{OUT2}) are 3.7 V and 5 V, respectively. Because of the heavy load, the supercapacitor at the V_{STOR} and the capacitor at the V_{cntrl} start discharging. Once the V_{cntrl} voltage drops to 1.44 V, the S_{L2} shuts off, and thus, the supercapacitor is disconnected from the boost converter. The V_{dc} and V_{OUT2} voltages drop to zero while the V_{GL} voltage increases from 0 V to the V_{STOR} voltage. The V_{cntrl} voltage starts rising up again, and the same process will be repeated over time.

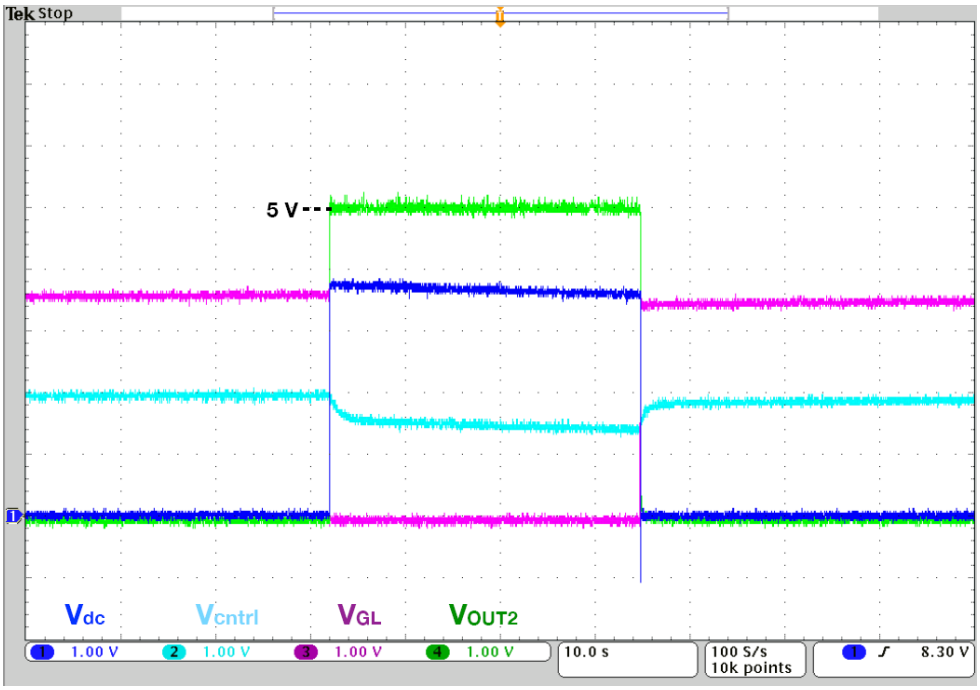

Figure 7. Voltage waveforms at the V_{cntrl}, V_{dc}, V_{GL}, V_{OUT2} nodes under a heavy load at the load 2.

Figure 8 indicates measured voltage waveforms for the proposed architecture operating in burst mode with various output power levels. The measured waveforms demonstrate that the architecture regulates two outputs at voltage levels of nearly 3.7 and 5 V.

Finally, the end-to-end efficiency of the proposed architecture that accommodates two loads operating in burst mode was measured. The efficiency is expressed as

$$\eta_{end} = \frac{\sum P_{load}}{P_{max}} \times \frac{t_{on}}{(t_{on} + t_{off})} = \frac{P_{out1} + P_{out2}}{P_{max}} \times \frac{t_{on}}{(t_{on} + t_{off})} \quad (1)$$

where t_{ON} is the time duration for both active loads. t_{ON} times for both loads are the same. (t_{ON}+t_{OFF}) is the time between two power cycles received by the loads. P_{max} is the maximum power available from the functional MFC. Efficiency measurements indicated a peak efficiency of 56.51% with two outputs at V_{OUT1}= 3.7 V and V_{OUT1}= 5 V.

Table 2 shows the performance summary and comparison to prior work. The architecture is the first to regulate multiple outputs with multiple MFCs. Also, the architecture accomplishes the highest efficiency among prior art multi-input MFCs.

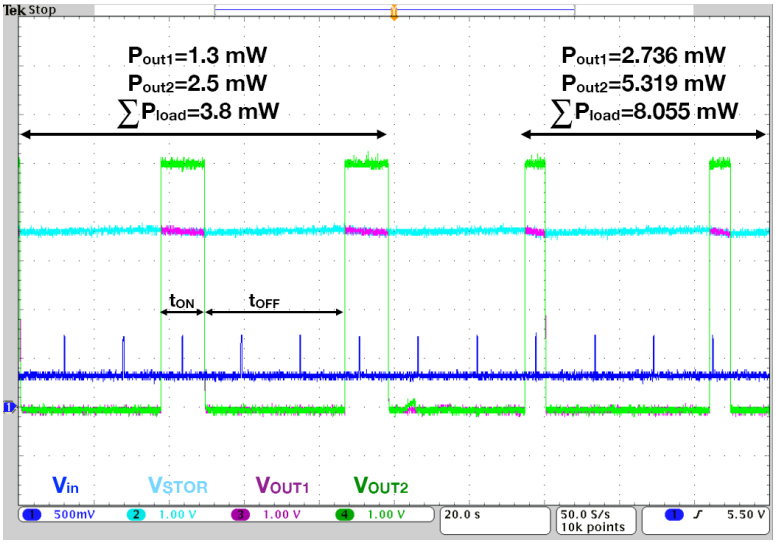

Figure 8. Measured voltage waveforms under varying heavy loads.

Table 2. Performance comparison of the proposed architecture to prior work for multiple MFCs.

Parameters	[14]	[17]	[18]	[20]	This work
Technology	Discrete	Discrete	Discrete	Discrete	Discrete
No of inputs	2	4	2	2	2
No of outputs	1	1	1	1	2
Architecture	2-stage 2-transfs+1-ind	1-stage 8-inds⋆	2-stage 2-inds	2-stage 2-caps§+1-ind	2-stage± 2-inds±
Output voltage (V)	5	0.4-1.6‡	3.3	3.3	3.7 & 5
Efficiency	26%† @Vin=0.44 V	32.8%†	42.16%	NA	56.51

⋆ 4-inductors used for startup circuit. § First-stage includes two charge pumps. ± Second load needs an addition boost converter. ‡ Not regulated. † Not end-to-end efficiency.

4 CONCLUSION

This article presented an energy harvesting architecture for multiple MFCs, implemented using off-the-shelf components. The architecture receives the energy from two MFCs while regulating two independent different power rails. The architecture decoupled one of the MFCs from the output load contribution by putting in the position of the backup in order to employ it once the other active MFC is impaired. The architecture used a second boost converter to regulate the second output to a higher voltage level (e.g., 5 V) than the first output (e.g., 3.7 V). The architecture achieves the peak efficiency of 56.51% due to the full isolation between MFCs, the optimum maximum power extraction from the energy source, and one converter at the load side. Measurement exhibited that the architecture achieves the highest peak efficiency with multiple outputs as compared to prior work.

Statement of Research and Publication Ethics

The study is complied with research and publication ethics.

Artificial Intelligence (AI) Contribution Statement

This manuscript was entirely written, edited, analyzed, and prepared without the assistance of any artificial intelligence (AI) tools. All content, including text, data analysis, and figures, was solely generated by the author.

REFERENCES

[1] U. Karra, E. Muto, R. Umaz, M. Kölln, C. Santoro, L. Wang, and B. Li, "Performance evaluation of activated carbon-based electrodes with novel power management system for long-term benthic microbial fuel cells," *Int. J. Hydrogen Energy*, vol. 39, no. 36, pp. 21847–21856, 2014.

[2] A. Meehan, H. Gao, and Z. Lewandowski, "Energy harvesting with microbial fuel cell and power management system," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 176–181, Jan. 2011.

[3] R. Umaz and L. Wang, "Integrated power converter design for bioturbation resilience in multi-anode microbial fuel cells," *IET Circuits, Devices Syst.*, vol. 13, no. 8, pp. 1142–1151, 2019.

[4] C. Donovan, A. Dewan, H. Peng, D. Heo, and H. Beyenal, "Power management system for a 2.5 W remote sensor powered by a sediment microbial fuel cell," *J. Power Sources*, vol. 196, no. 3, pp. 1171–1177, 2011.

[5] I. Lee *et al.*, "System-on-mud: Ultra-low power oceanic sensing platform powered by small-scale benthic microbial fuel cells," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 4, pp. 1126–1135, Apr. 2015.

[6] B. Logan, *Microbial Fuel Cells*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2008.

[7] R. Umaz, C. Garrett, F. Qian, B. Li, and L. Wang, "A power management system for multianode benthic microbial fuel cells," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3562–3570, May 2017.

[8] E. Dallago, A. Lazzarini Barnabei, A. Liberale, G. Torelli, and G. Venchi, "A 300-mV low-power management system for energy harvesting applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2273–2281, Mar. 2016.

[9] G. Huang, R. Umaz, U. Karra, B. Li, and L. Wang, "A biomass-based marine sediment energy harvesting system," in *Proc. Int. Symp. Low Power Electron. Design (ISLPED)*, Sept. 2013, pp. 359–364.

[10] P. K. Wu, J. C. Biffinger, L. A. Fitzgerald, and B. R. Ringeisen, "A low power DC/DC booster circuit design for microbial fuel cell," *Process Biochem.*, vol. 47, no. 11, pp. 1620–1626, 2012.

[11] F. Qian, R. Umaz, Y. Gong, B. Li, and L. Wang, "Design of a shared stage charge pump circuit for multi-anode microbial fuel cells," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 213–216.

[12] J. D. Park and Z. Ren, "Hysteresis-controller-based energy harvesting scheme for microbial fuel cells with parallel operation capability," *IEEE Trans. Energy Convers.*, vol. 27, no. 3, pp. 715–724, Sept. 2012.

[13] R. Umaz and L. Wang, "An energy combiner design for multiple microbial energy harvesting sources," in *Proc. Great Lakes Symp. VLSI*, May 2017, pp. 443–446.

[14] J.-D. Park and S. Lee, "Single-transistor sub-1-V self-startup voltage boost energy harvesting system for microbial fuel cells," *J. Power Sources*, vol. 418, pp. 90–97, 2019.

[15] S. Carreon-Bautista, C. Erbay, A. Han, and E. Sanchez-Sinencio, "An inductorless DC-DC converter for an energy aware power management unit aimed at microbial fuel cell arrays," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 1109–1121, Dec. 2015.

[16] R. Umaz, "A power management system for microbial fuel cells with 53.02% peak end-to-end efficiency," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 67, no. 11, pp. 2592–2596, Nov. 2020.

[17] N. Tang, W. Hong, T. Ewing, H. Beyenal, J. H. Kim, and D. Heo, "A self-sustainable power management system for reliable power scaling up of sediment microbial fuel cells," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4626–4632, Sept. 2015.

[18] R. Umaz, "A single inductor self-startup energy combiner circuit with bioturbation resilience in multiple microbial fuel cells," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 67, no. 12, pp. 3227–3231, Dec. 2020.

[19] U. Karra, G. Huang, R. Umaz, C. Tenaglier, L. Wang, and B. Li, "Stability characterization and modeling of robust distributed benthic microbial fuel cell (DBMFC) system," *Bioresour. Technol.*, vol. 144, pp. 477–484, 2013.

[20] R. Umaz and Y. Sahin, "An architecture for two ambient energy sources," in *Proc. Int. Conf. Power Electron. Appl. (ICPEA)*, 2019, pp. 1–6.