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Performance Evaluation of Various Multicarrier Pulse Width Modulation Techniques for Seven-level Packed U-Cell Multilevel Inverter with a Novel Switching Generating Method

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Highlights

- Analysis and comparison of multicarrier PWM methods for a PUC-MLI were conducted.
- Conduction and switching losses were separately analyzed to evaluate semiconductor losses.
- A novel switching generation method for conventional PWM was proposed for PUC-MLI operation.
- Numerical studies were performed on a single-phase 324 kVA seven-level PUC-MLI.

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Abstract

In this paper, a novel switching generation method is presented that adapts conventional pulse width modulation (PWM) methods to the packed U-cell multilevel inverter topology. The proposed solution involves designing a combinational logic circuit constructed using minterms. By selecting and summing appropriate minterms, the resulting output signal is used to drive the power semiconductors. Additionally, various multicarrier PWM methods are analyzed and compared based on performance metrics such as output current harmonics, DC bus utilization, and semiconductor losses. Numerical studies are conducted in MATLAB on a single-phase 324 kVA, seven-level PUC-MLI using an improved semiconductor loss estimation approach that employs higher-order loss curves for both IGBT and diode, derived from the manufacturer's data sheet. When compared to level-shifted PWM, phase-shifted PWM (PS-PWM) consistently achieves lower current THD, even at low carrier frequencies, and always maintaints THD within the limits of the IEEE-519 power quality standard. It is also shown that the PS-PWM method results in approximately 3.3 times higher semiconductor losses on average than level-shifted PWM methods. Across all PWM methods, the carrier frequency has a negligible effect on the fundamental component of the output voltage, which remains below 1V. Furthermore, when comparing the PS-PWM method as a whole to level-shifted PWM methods, DC voltage variations of up to 0.5% are observed at the output for a given modulation index. The simulation results indicate that while level-shifted PWM methods generate lower semiconductor losses, the phase-shifted PWM option provides better power quality.

1. INTRODUCTION

A multilevel inverter (MLI) combines power electronic switches, circuit elements, and one or more DC sources to generate a stepped voltage waveform at its output. An MLI can serve as an alternative to two- or three-level inverters when an increase in the operating voltage or current is required. Although, classical two-level inverters are simple to implement and control, their output waveforms are distorted, reducing power quality and increasing filter size and cost. Moreover, the high switching frequency in these inverters further limits operational efficiency. MLIs are well suited for applications in renewable energy integration [1,2], AC drives [3,4], and power quality devices [5-7]. Over the past few decades, numerous MLI topologies have been developed using various switching strategies at various power levels [8-10]. MLIs have attraction significant attention due to their merits over two- or three-level inverters, such as reduced harmonic content, lower switching frequency and voltage stress on switches, and improved electromagnetic interference. MLIs are usually preferred because their output more closely resembles a sine waveform as the number of levels increases, enabling high-quality output and smaller filter design. Among the fundamental MLI configurations are the neutral point clamped (NPC), flying capacitor (FC), and cascaded

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H-bridge (CHB) topologies. However, the control scheme and the circuit design become more complex as the voltage levels at the output increases in these topologies. In addition, voltage balancing is another issue in NPC and FC topologies. Although the CHB topology is a better choice for generating a large number of stepped voltage levels, it is less economically attractive because it relies on multiple isolated DC sources. Various configurations composed of fundamental units have been posited in the literature to address the deficiencies inherent in the aforementioned MLI topologies. Among MLI topologies, the packed U-cell (PUC)-based MLI (PUC-MLI) is a competing inverter, which merges the benefits of both FC and CHB topologies [11-13]. Operating with asymmetrical DC voltages, the PUC-MLI topology has received great attention in recent years, and its performance has been validated in numerous applications, such as photovoltaic integration [14-19], wind energy systems [20], active filter [21,22], static VAR compensator [23], UPQC [24], and dynamic voltage restorer [25]. PUC-MLI can generate the same number of output voltage levels with a reduced semiconductor count compared to conventional NPC, FC, and CHB topologies. Several PUC-MLI papers have been published in the literature, with output voltage levels ranging between 5 and 31 [26]. Furthermore, it also offers bidirectional power flow and is suitable for both stand-alone [20,26,27] and grid-connected applications [15-17,28]. Although other DC sources can be capacitors, only a single DC source is needed to generate the multilevel voltage waveform. This feature enhances practical applicability and reduces design cost. However, regulating the capacitor voltage in each PUC to the desired value remains challenging because it requires modifications to the main current control loop, thereby increasing control complexity [29]. In [30], a set of logic-based equations have been proposed to balance the floating capacitor voltage in a seven-level PUC-MLI (PUC7-MLI). The approach is robust under dynamic load and variable power factor conditions. In [31], a hysteresis bandwidth technique is applied in conjunction with sliding mode control to regulate the capacitor voltage and the grid current of a grid-connected PUC7-MLI. The experiment designed in [32] demonstrates that the average energy exchange between the capacitors and the rest of the PUC7-MLI is zero to balance the capacitor voltages without closed-loop control. Furthermore, in [33], a voltage balancing method based on the charging and discharging of the capacitor at switching frequency of the phase shifted-pulse width modulation (PS-PWM) technique is proposed to reduce the capacitor size in a PUC5 converter. Multicarrier PWM methods find extensive applications in the control of MLIs in medium and high voltage/power scenarios owing to their straightforward implementation and operational simplicity [34]. Various multicarrier PWM methods exist, including PS-PWM, phase disposition PWM (PD-PWM), phase opposition disposition PWM (POD-PWM), and alternate phase opposition disposition PWM (APOD-PWM). The power quality, DC bus utilization, and the loss performance analysis of these gating techniques have been extensively studied for various MLI types in the current state-of-the-art [35-37]. However, such comparisons for PUC-MLI are scarce [38]. In this regard, this study addresses a detailed comparison of the aforementioned multicarrier PWM methods on a PUC7-MLI, employing important performance metrics such as total harmonic distortion (THD), DC bus utilization, conductor and switching losses, and average switching count under varying carrier frequencies and modulation index conditions. Secondly, an improved approach for estimating conduction and switching losses of the semiconductors is suggested. Finally, a novel switching generation method is suggested which translates the gating signals of a conventional multicarrier PWM method into the gating signals for PUC-MLIs. The highlights of this study are,

- To the best knowledge of the author, a comprehensive comparison including DC bus utilization, semiconductor losses (with separate analysis of conduction and switching losses), and THD content for various multicarrier PWM methods on PUC-MLIs has been conducted for the first time.
- Third-degree loss curves for the IGBT and a fourth-degree loss curve for the diode have been derived from the manufacturer data sheet, surpassing the conventional second-degree representation found in the literature [39], potentially contributing to the field and are made available for researchers' use.
- A novel method based on designing a combination logic circuit that utilizes the concept of the sum of minterms has been put forward to map the gating signals of the conventional multicarrier PWM technique for PUC-MLIs.

The rest of the paper is organized as follows: Section 2 briefly portrays the topological configuration of the PUC7-MLI and its operating states; Section 3 explains the details of the switching generation method proposed in this study; Section 4 demonstrates the semiconductor loss calculation method; Section 5 explains how the ratings of the PUC-MLI are determined; Section 6 illustrates the numerical results for the evaluation of the different performance metrics of the various PWM methods; and Section 7 concludes the study.

2. THE PUC TOPOLOGY

The basic circuit diagram of a single-phase PUC-MLI consists of a single U-cell, four power semiconductor switches, and two DC sources, as depicted in Figure 1. Note that an auxiliary capacitor can be replaced instead of one of the DC sources. A U-cell refers to a module that includes two power semiconductor switches (along with their antiparallel diodes) and either a flying or clamping capacitor. Because commercial IGBTs often lack reverse blocking capability, they are typical paired with an antiparallel diode. Figure 1 also illustrates the possible operating modes of the PUC-MLI by depicting the various switching states of the IGBTs. The design offers high flexibility in multilevel voltage synthesis, enabling the number of U-cells to be increased to achieve a greater number of voltage levels at the output terminals.

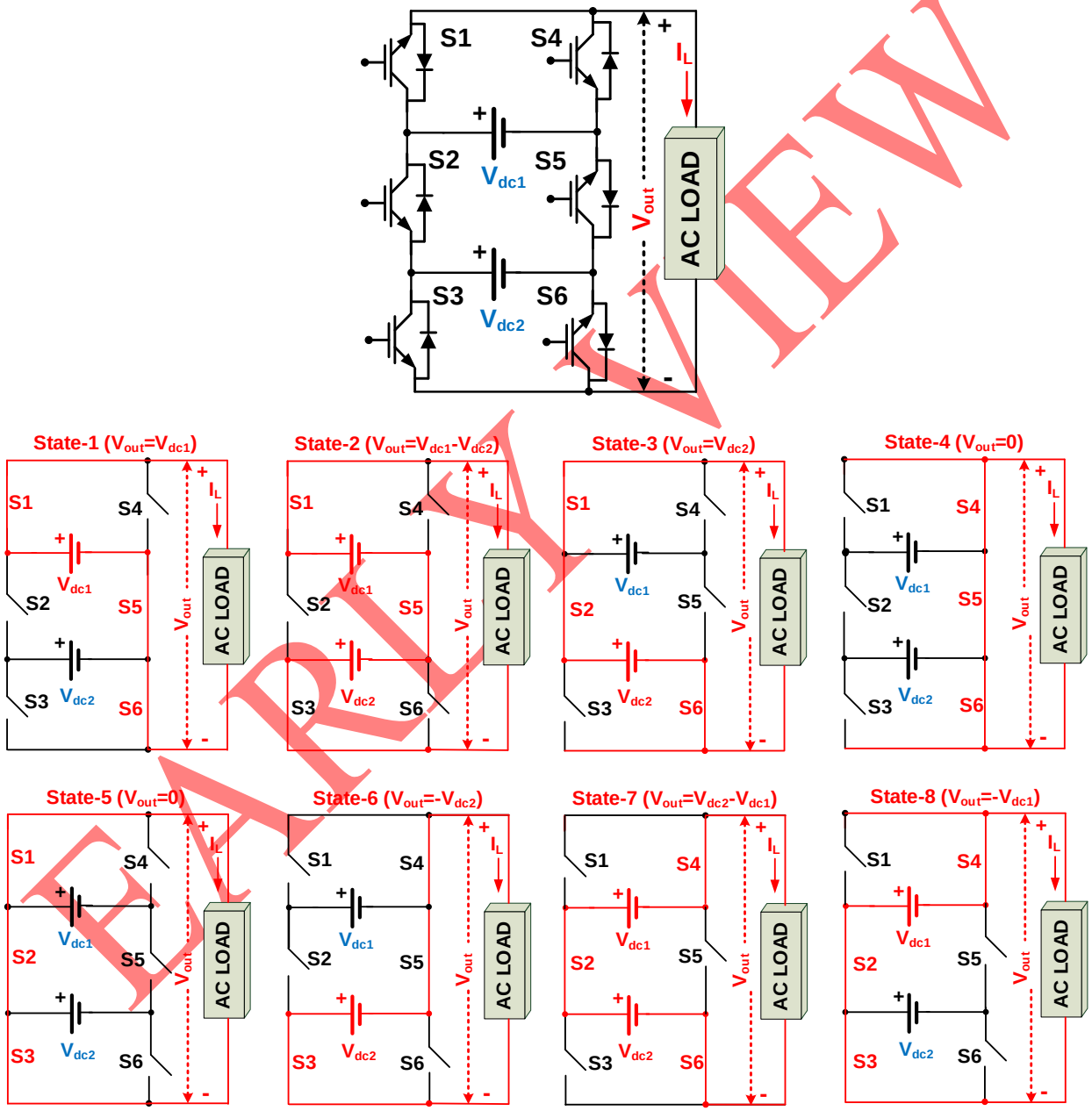


Figure 1. *The fundamental power circuit of PUC-MLI and its operating modes*

In the circuit, five or seven voltage levels can be generated without altering the power stage by setting the ratio of the two DC voltages V_{dc1}/V_{dc2}. For instance, setting $V_{dc1}/V_{dc2} = 2$ yields five voltage levels, whereas $V_{dc1}/V_{dc2} = 3$ produces seven voltage levels at the inverter's output. In this regard, the individual

output voltage of PUC-MLI for each state in both five- and seven-level operations is given in Table 1. For the purpose of this study, an additional DC source V_{dc2} is employed instead of the auxiliary capacitor in the PUC topology. By this way, the capacitor voltage control and balance are not needed. Table 2 compares the component counts employed in different MLI topologies for single-phase operation. An examination of these metrics reveals that the PUC topology generally requires fewer components, and this advantage becomes more significant as the number of output voltage levels increases.

Table 1. *The individual output voltage of PUC-MLI at each state for five- and seven-level operations*

Five-level operation $(\boldsymbol{V_{dc1} = 2E, V_{dc2} = E})$		**Seven-level operation** $(\boldsymbol{V_{dc1} = 3E, V_{dc2} = E})$	
State	$\boldsymbol{V_{out}}$	**State**	
1	$V_{out} = V_{dc1} = 2E$	**1**	$V_{out} = V_{dc1} = 3E$
2	$V_{out} = V_{dc1} - V_{dc2} = E$	**2**	$V_{out} = V_{dc1} - V_{dc2} = 2E$
3	$V_{out} = V_{dc2} = E$	**3**	$V_{out} = V_{dc2} = E$
4	$V_{out} = 0$	**4**	$V_{out} = 0$
5	$V_{out} = 0$	**5**	$V_{out} = 0$
6	$V_{out} = -V_{dc2} = -E$	**6**	$V_{out} = -V_{dc2} = -E$
7	$V_{out} = V_{dc2} - V_{dc1} = -E$	**7**	$V_{out} = V_{dc2} - V_{dc1} = -2E$
8	$V_{out} = -V_{dc1} = -2E$	**8**	$V_{out} = -V_{dc1} = -3E$

Table 2. *A comparison of the component counts used in different single-phase MLIs voltage of PUC-MLI at each state for five- and seven-level operations*

Single-phase MLI type ***L*****=level count**	**Power semiconductor switch count**	**Diode count**	**Capacitor count**	**DC source count**
NPC	$2(L-1)$	$(L-1)(L-2)$	$L-1$	1
FC	$2(L-1)$	0	$0.5(L^2-L)$	1
CHB	$2(L-1)$	0	0	$0.5(L-1)$
PUC-MLI ($L = 3,5$)	$L+1$	0	1	1
PUC-MLI ($L \geq 7$)	$L-1$	0	$0.5(L-5)$	1

On the other hand, Figure 2 provides a rough comparison of the cost of a 250kW single-phase inverter constructed using various MLI topologies, evaluated as a function of the number of voltage levels. It is evident that the PUC-MLI has the lowest device cost among all other MLIs, particularly at higher voltage levels. This is primarily due to that the PUC topology has the advantage of reduced component when generating the same multilevel voltage waveform when compared to NPC, FC, and CHB topologies. There might be different DC sources to be utilized in an MLI, including rectifier, renewable energy, and battery systems. Thereby, the cost of the DC source is excluded from this comparison due to its inherent versatility.

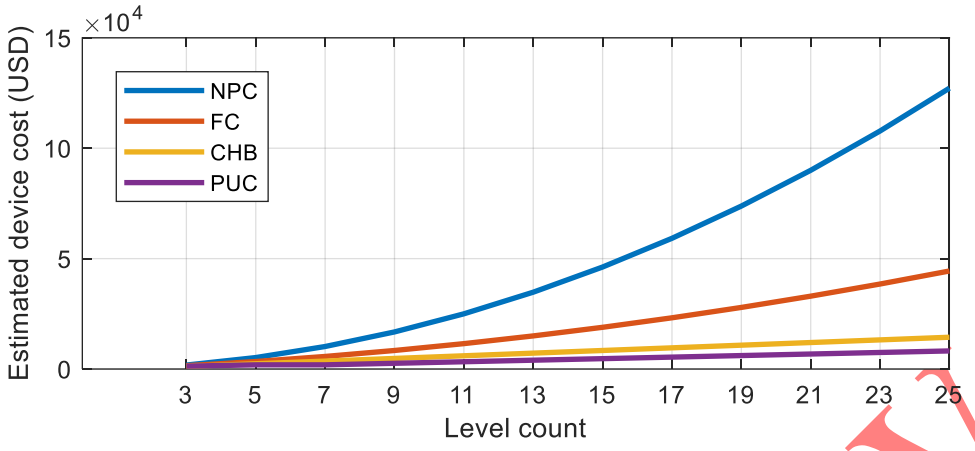
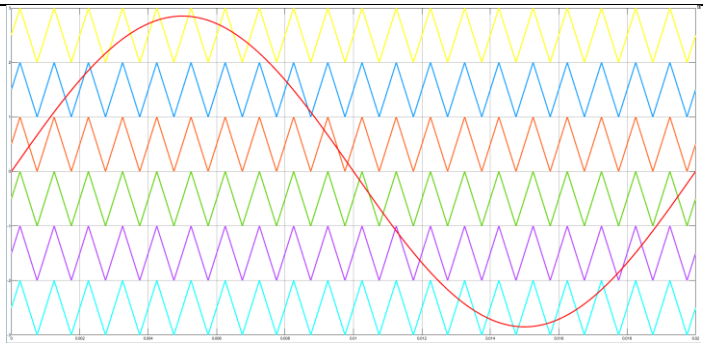


Figure 2. *Estimated device cost of a single-phase 250 kW inverter constructed by different MLI topologies with respect to the voltage level count*

3. NOVEL SWITCHING GENERATION FOR PUC-MLIs

There are numerous modulation methods available for controlling power semiconductor switches in MLIs, including space vector PWM, selective harmonic elimination (SHE), and multicarrier PWM. Although SHE can eliminate specific harmonics from the output waveform, determining the optimal switching angles to cancel out targeted harmonics is not easy for real applications, especially when a high number of output levels is involved, since many nonlinear equations should be solved iteratively. Similarly, designing space vector PWM is complicated by its computational complexity, particularly for high-level voltage operations. Hence, in this study, commonly used multicarrier PWM methods, namely, PS-PWM, PD-PWM, POD-PWM, and APOD-PWM are adapted for PUC-MLI operation because of their well-acceptance in the literature for their effectiveness in removing harmonics and simpler control compared to other switching methods. The multicarrier PWM method employs multiple high-frequency sawtooth or triangular carriers to modulate the output waveform. These carriers are typically compared to a modulating signal, such as a sinusoidal reference at the fundamental frequency. To generate m-voltage levels at the inverter output, $m-1$ carriers are required. Figure 3 shows the reference and carrier arrangements for the aforementioned multicarrier PWM methods with a sinusoidal modulating signal for seven-level inverter operation.

PWM method	**Carrier arrangements (7-level inverter operation)** fundamental frequency, $f_{fund} = 50\ Hz$ modulation index, $m_{ind} = 0.95$ carrier frequency, $f_c = 1\ kHz$
In **PD-PWM**, all carriers exhibit identical phase relationships above and below the zero-reference line.	

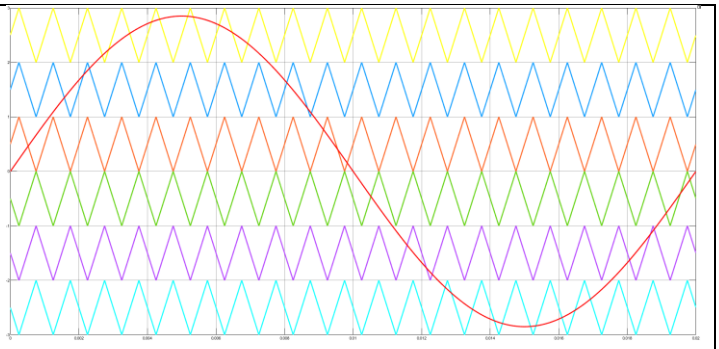
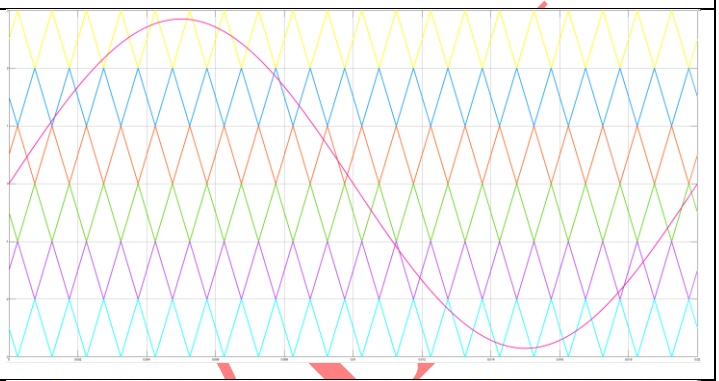
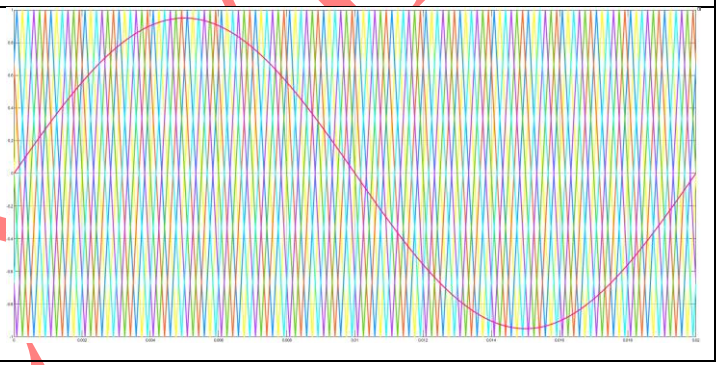
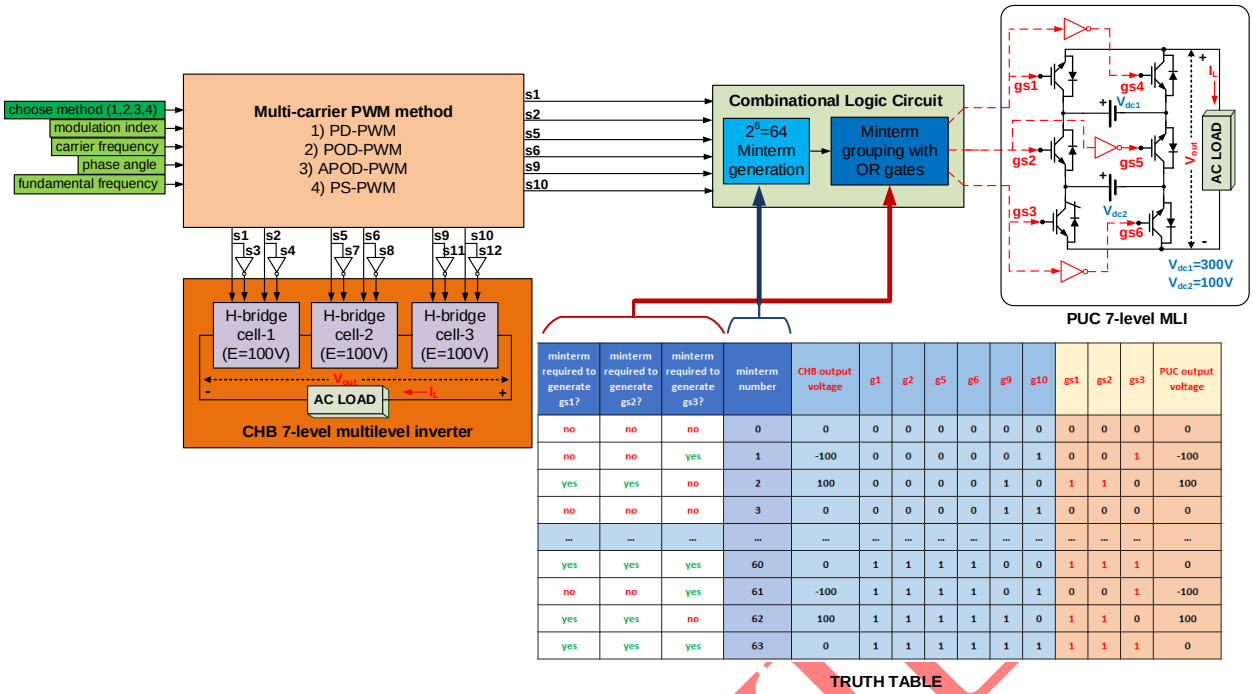
In **POD-PWM**, the carriers above the sinusoidal reference point are 180° out of phase with those below the zero-reference line.	
Each triangular carrier is phased shifted by 180° form its adjacent carrier in **APOD-PWM**.	
PS-PWM involves shifting the phase of each carrier signal by $360^{\circ}/(m-1)$ degrees, where m is the voltage-level at the inverter output.	

Figure 3. *The reference and carrier arrangements for various multicarrier PWM methods*

The aforementioned multicarrier PWM methods have originally been designed for conventional inverters, such as, NPC, FC, and CHB MLI. Due to differences in switching states, operating modes, and switch count, multicarrier PWM methods cannot be directly applied to the PUC-MLI. Accordingly, in this study, a novel method is proposed through a combinational logic circuit with six Boolean inputs and three Boolean outputs. To implement the proposed method, a truth table is first constructed to identify the switching states of a CHB inverter that produces an equivalent number of voltage levels. This truth table shows the values of the CHB inverter's output voltage according to the ON/OFF states of the semiconductors. For a 7-level CHB inverter, we need 3 H-bridge modules and 6 switches in total, with 2 switches for each module. As shown in Figure 4, for these 6 switch states (s1, s2, s5, s6, s9, s10), the output voltage of the CHB inverter will take three different values (0, -E, E). Since there are $2^6 = 64$ possible switch combinations, the operation of the 7-level CHB inverter can be expressed using 64 minterms, each representing a unique combination of these six switch states (s1, s2, s5, s6, s9, s10). A minterm is a term used in digital logic circuits and plays an important role in their design and optimization. Logic circuits are generally composed of components that process a set of inputs to obtain a specific output. A minterm represents the situation where the output of the circuit is "1" for every possible combination of inputs, expressed as an AND (conjunction) statement. A minterm includes either the truth or false (1 or 0) of each input. In other words, a minterm is only true for a specific input combination once. In the second stage of the method, the possible output voltage of the PUC-MLI (0, -E, E) are listed according to the ON/OFF states of the semiconductors in PUC-MLI.



minterm required to generate gs1?	minterm required to generate gs2?	minterm required to generate gs3?	minterm number	CHB output voltage	g1	g2	g5	g6	g9	g10	gs1	gs2	gs3	PUC output voltage
no	no	no	0	0	0	0	0	0	0	0	0	0	0	0
no	no	yes	1	-100	0	0	0	0	0	1	0	0	1	-100
yes	yes	no	2	100	0	0	0	0	1	0	1	1	0	100
no	no	no	3	0	0	0	0	0	1	1	0	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
yes	yes	yes	60	0	1	1	1	1	0	0	1	1	1	0
no	no	yes	61	-100	1	1	1	1	0	1	0	0	1	-100
yes	yes	no	62	100	1	1	1	1	1	0	1	1	0	100
yes	yes	yes	63	0	1	1	1	1	1	1	1	1	1	0

TRUTH TABLE

Figure 4. *The switching signal generation of the PUC7-MLI*

Since the 7-level PUC topology requires 6 switches, and since each pair of switches operates complementarily, the output voltage values of the 7-level PUC inverter can be determined by three distinct switching states. These states and their corresponding switch combinations are highlighted in orange in Figure 4. In the next stage of the method, the switch combinations that produce the same voltage as the CHB inverter and the PUC-MLI are matched. For example, to produce an output of -100 V on the CHB inverter, the required switch configuration is (0, 0, 0, 0, 0, 1). To achieve the same output voltage in the PUC-MLI output, the required switch combination will be (0, 0, 1). In this context, the input signals for the designed logic circuit are taken from the switching states of the CHB inverter, while its outputs represent the switching states of the PUC-MLI. Since the (0, 0, 0, 0, 0, 1) switch combination is referred to as minterm1, it will be used to make gs3=1. To generate minterm-1, the inverted switching signals ($g_1'.g_2'.g_5'.g_6'.g_9'.g_{10}$) should be multiplied or (AND-gated). This situation is shown in red with 1 in Figure 4. In this way, all 64 rows are checked, and it is determined which minterms make the PUC inverter's switching value 1. Since the table for 64 rows would be very large, only some of the rows are shown in Figure 4. In the final stage of the method, the columns created for gs1, gs2, and gs3 are examined separately, and for each switching state, the required minterms are identified. Here, gs1, gs2, gs3 can be considered as a separate combinational logic function, and the minterms needed for each of them are connected using OR gates or addition (+) operations. This is shown in the equations below with the SUM operation. Since the equations would be very long, only some of the minterms are provided. As demonstrated, the implementation of the proposed method is straightforward and simple, making programming and practical application both easy. Moreover, its implementation is well-suited for simulation and experimental studies. This method can theoretically be applied to any voltage level in a PUC-MLI. For reference, the required number of minterms according to the number of voltage levels are listed in Table 3.

$$gs1(g1, g2, \dots, g6) = \sum minterm(2,8,10,11, \dots 59,60,62,63) \quad (1)$$
$$gs2(g1, g2, \dots, g6) = \sum minterm(2,8,11,14, \dots 21,23,29,53) \quad (2)$$
$$gs3(g1, g2, \dots, g6) = \sum minterm(33,36,39,45, \dots 49,52,55,61) \quad (3)$$

Table 3. *Total required minterm counts for different voltage levels*

PUC-MLI voltage-level count	PUC-MLI semiconductor count	Input count for logic circuit	Output count for logic circuit	Total minterm count
5	4	4	2	16
7	6	6	3	64
9	8	8	4	256
11	10	10	5	1024

4. SEMICONDUCTOR LOSS CALCULATION

The power dissipation cause by internal gate resistance due to the superimposed measurement voltage remains the lower milliwatt range. In contrast, during regular chip operation, conduction and switching losses occur in the several-watt range. Consequently, the impact of self-heating effect resulting from the superimposed measurement voltage can be disregarded [40]. Additionally, as the diode turns on extremely quickly at zero voltage, the energy required to turn it on can be neglected. Thus, only the diode reverse recovery energy loss during turning off is taken into account. In this study, the snubber elements have been chosen too large (1 MΩ) compared to the on-state resistance values of both the IGBT and the diode. Consequently, the losses associated with snubber circuit for each semiconductor are also neglected. As a result, only the conduction and switching losses of the IGBT and the reverse parallel-connected diode are analyzed. In this study, 1700V-600A dual IGBT module (FF600R17ME4) from Infineon is used [41]. The rated collector-emitter voltage of this IGBT is $V_{CES} = 1200\ V$, it has a nominal continuous collector current rating of $I_C = 600\ A$ and a repetitive peak collector current of $I_{CRM} = 1200\ A$.

4.1. Conduction Loss Calculation of IGBT and Diode

To calculate the conduction losses of the semiconductors, the on-state resistance and forward voltage drop of the IGBT and the diode should be determined. To estimate the on-state resistance of the IGBT, the $I_C - V_{CE}$ curves given at different temperatures can be used [41]. For IGBT, the linearized function of I_C with respect to V_{CE} at temperature of 125 ℃ under the condition, $I_C > 200A$, is expressed as,

$$I_C = 465.9V_{CE} - 482.5. \tag{4}$$

From (4), the forward voltage drop of the IGBT is calculated by finding the value of V_{CE} when $I_C = 0$, i.e., $V_{CE0} = 482.5/465.9 = 1.0376\ V$. On the other hand, the reciprocal of the line slope shown in Figure 5 (a) gives the on-state resistance of the IGBT, $R_{ON} = 0.0021462986\ \Omega$. Similarly, for the diode, the linearized function of I_F with respect to forward voltage drop V_F at temperature of 125 ℃ under the condition, $I_F > 200A$, is obtained by linearizing the $I_F - V_F$ curve in [41],

$$I_F = 825.9V_F - 967.1\ . \tag{5}$$

From (5), the forward voltage drop of the diode is calculated by finding the value of V_D when $I_F = 0$, i.e., $V_{D0} = 967.1/825.9 = 1.1710\ V$. The reciprocal of the line slope shown in Figure 5 (b) gives the on-state resistance of the diode, such as $R_{ON} = 0.001210755\Omega$.

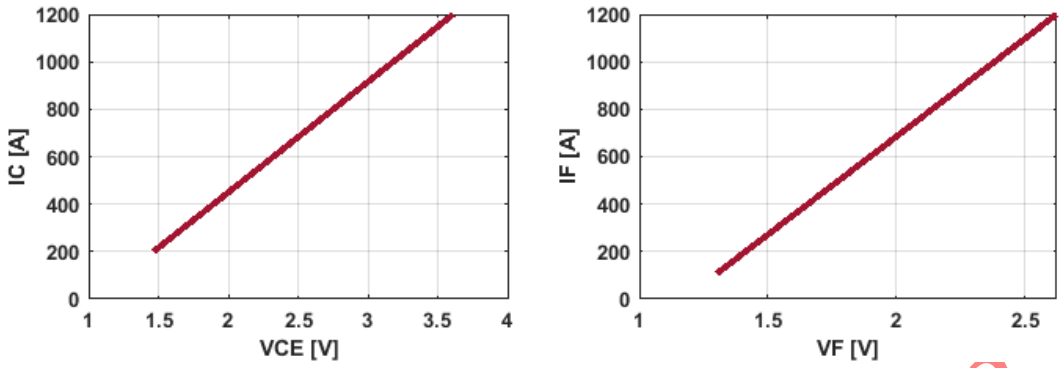
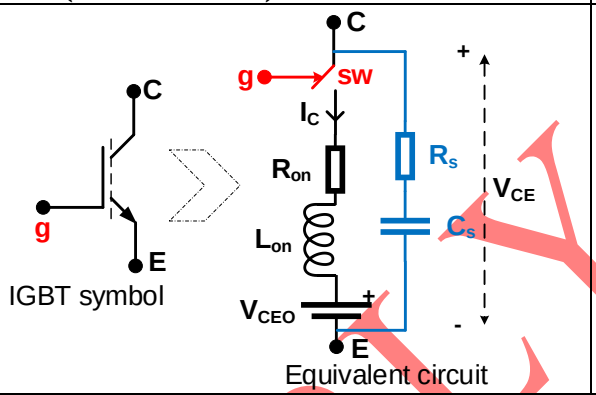
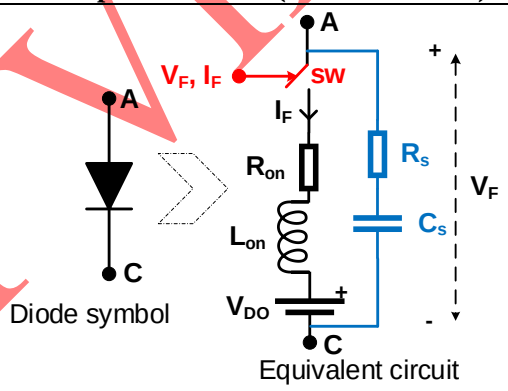


Figure 5. *(a) Typical output characteristics of the IGBT, ($V_{GE} = 15V$), (b) typical forward characteristics of the diode*

The approximated semiconductor switch models and their corresponding parameters at a temperature of 125 ℃ are illustrated in Table 4. These models include macro representations of the actual IGBT and diode devices, focusing on their functional characteristics while excluding considerations of device geometry and intricate physical processes.

Table 4. *Approximated semiconductor switch models and their estimated parameters at 125℃*

IGBT (FF600R17ME4)	**Reverse-parallel diode (FF600R17ME4)**
	
On-state resistance R_{ON}= 0.0021462986 Ω	On-state resistance R_{ON}= 0.001210755 Ω
Internal inductance L_{ON}= 20 nH [41]	Internal inductance L_{ON}= 0
Forward voltage drop V_{CE0}= 1.0376 V	Forward voltage drop V_{D0}= 1.1710 V
Snubber resistance R_s= 1M Ω	Snubber resistance R_s= 1M Ω
Snubber capacitance C_s= 250 nF	Snubber capacitance C_s= 250 nF

The conduction loss of the IGBT (P_{C-IGBT}) and the conduction loss of the reverse-parallel diode ($P_{C-diode}$) are calculated using (6) and (7), respectively. These equations perform rectangle-type numerical integration with a sample time T_s to determine the average instantaneous conduction loss over one period T_{period}. The rectangle method is easy to apply compared to trapezoidal integration, as the simulation models have no continuous states which are numerically solved in discrete form. This means any signal remains constant during T_s, so the area under the curve can be perfectly filled with n small rectangles, as shown in Figure 6. Within one period, n can reach a maximum value of $T_{period}/T_s = 10000$. The average conduction loss of each semiconductor device is calculated by summing the areas of these rectangles and dividing by T_{period}

$$P_{C-IGBT} = \frac{1}{T_{period}} \sum_{i=1}^{n} \left[V_{CE0} I_{C+} R_{ON} {I_C}^2\right] T_s \quad (6)$$

$$P_{C-diode} = \frac{1}{T_{period}} \sum_{i=1}^{n} \left[V_{D0} I_{F+} R_{ON} {I_F}^2\right] T_s \, . \quad (7)$$

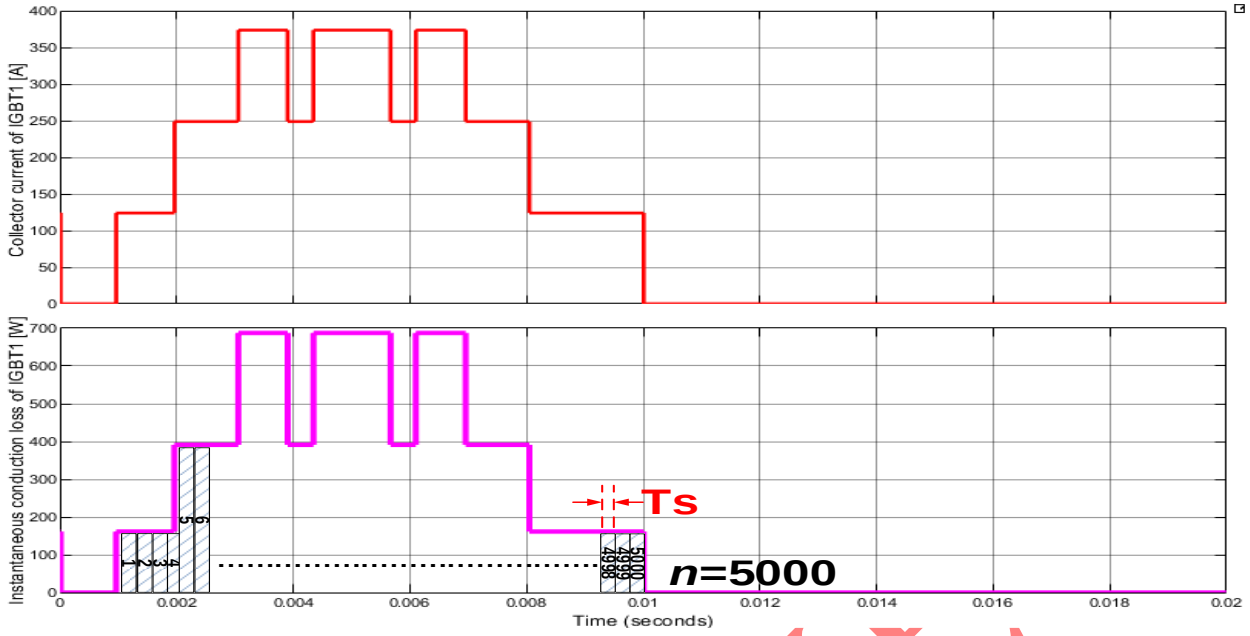


Figure 6. *The collector current and instantaneous conduction loss of IGBT1 in PUC-MLI for a R-load* $(f_c = 100Hz)$

4.2. Switching Loss Calculation of IGBT and Diode

The turn-on and turn-off losses of the IGBT as well as the turn-off (recovery) loss of the diode can be estimated using curve fitting techniques applied to the semiconductor characteristics provided in the semiconductor datasheet [41]. By this way, the energy losses of the IGBT and the diode can be accurately approximated using high order polynomials. In this regard, the turn-on and turn-off energy losses of the IGBT (FF600R17ME4) can be expressed as third order polynomials, given below. The resulting energy loss curves of the IGBT at a temperature of 125℃ are shown in Figure 7 for the range $50A \leq I_C \leq 1200A$

$$E_{IGBTon}(mJ) = 8.235 \times 10^{-7} \times {I_C}^3 - 0.0008527 \times {I_C}^2 + 0.5802 \times I_C - 11.24 \quad (8)$$

$$E_{IGBToff}(mJ) = 6.771 \times 10^{-8} \times {I_C}^3 - 0.0001601 \times {I_C}^2 + 0.3668 \times I_C + 2.581\,. \quad (9)$$

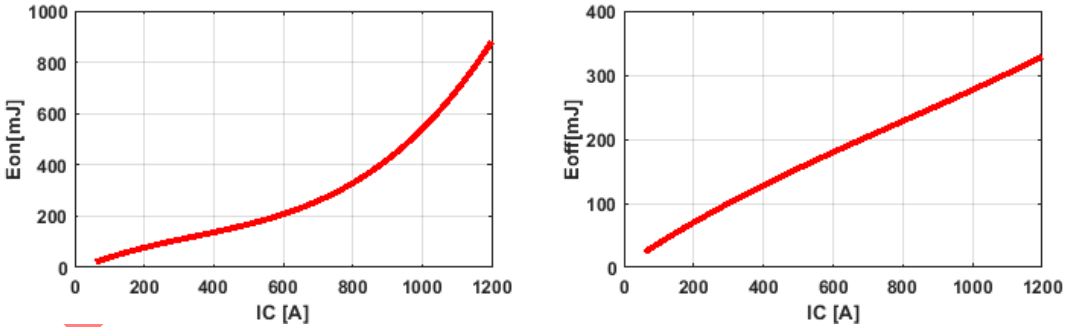


Figure 7. *The approximated energy loss curves of the IGBT (FF600R17ME4)* $(V_{GE} = \pm 15V, R_{Gon} = R_{GoF} = 1\Omega, V_{CE} = 900V)$

Similarly, the turn-off energy loss of the reverse-parallel diode at a temperature of 125℃ can be expressed as a fourth order polynomial expressed in (10). The approximated loss curve of the diode is plotted in Figure 8 for $V_{CE} = 900V$ and $50A \leq I_F \leq 1200A$

$$E_{rec}(mJ) = 4.875 \times 10^{-11} \times {I_F}^4 - 9.105 \times 10^{-8} \times {I_F}^3 - 7.148 \times 10^{-5} \times {I_F}^2 + 0.2268 \times I_F + 45.83\,. \quad (10)$$

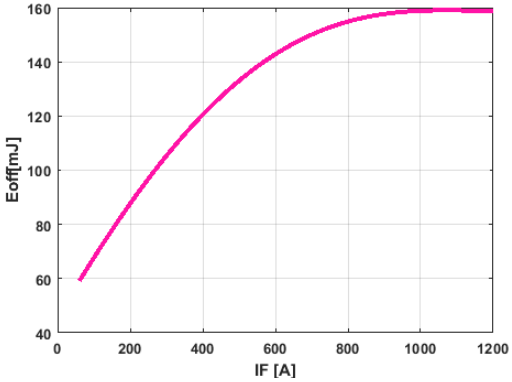


Figure 8. *The approximated recovery energy loss of the reverse-parallel diode (FF600R17ME4)*

The turn-on and turn-off energy loss of each IGBT as well as the turn-off (recovery) losses of each reverse parallel diode are numerically calculated in MATLAB simulation environment as shown in Figure 9. Initially, a rising and a falling edge detector detects the turn-on and turn-off instants of the IGBT by monitoring the logical gate signal. Upon detecting a change in its input, the edge detectors generate a pulse with a magnitude of 1 for the duration of T_s. The collector current of the IGBT (I_C) is sent to two function blocks that compute the turn-on and turn-off switching losses using (8) and (9), respectively. At the same time, the forward diode current (I_F) is sent to another function block that applies (10). During loss calculations, (8), (9), and (10) are multiplied by either ($2V_{CE}/900$) or ($V_{CE}/900$) to normalize the operating voltage of the semiconductor. This adjustment accounts for variations in the actual semiconductor voltage during the simulation, which may differ from the base voltage ($V_{CE} = 900V$) provided in the datasheet [41]. The output of the rising edge detector is connected to a delay block which delays the input signal for one sample time T_s. This delay is necessary because when the turn-on gate signal is applied to the IGBT, it goes to conduction after a time T_s. By incorporating this delay, the IGBT current can be measured precisely at the moment the rising edge detector generates its pulse, ensuring accurate calculation of the turn-on loss. The function of the multiplication blocks is to ensure that the losses are calculated only at the exact turning on/off instants of the semiconductor. Since PUC-MLI has a total of six IGBTs and six diodes, the calculation stages depicted in Figure 9 are simultaneously executed for each IGBT and diode, with all losses aggregated during the simulation. In this regard, the total average conductor losses P_{cond} and the average switching losses P_{sw} of the PUC-MLI are calculated separately using (11) and (12), respectively

$$P_{cond} = \sum_{i=1}^{6}(P_{C-IGBT-i} + P_{C-diode-i}) \tag{11}$$

$$P_{sw} = \frac{10^{-3}}{T_{total}}\sum_{i=1}^{6}\left(E_{IGBTon-i} + E_{IGBToff-i} + E_{rec-i}\right). \tag{12}$$

Since the switching losses represent the energy dissipation of the semiconductor during its turn-on and turn-off instances, the total energy loss is divided by the simulation time T_{total} to calculate P_{sw}. Finally, (13) determines the total semiconductor losses of the PUC-MLI

$$P_{LOSS} = P_{cond} + P_{sw}. \tag{13}$$

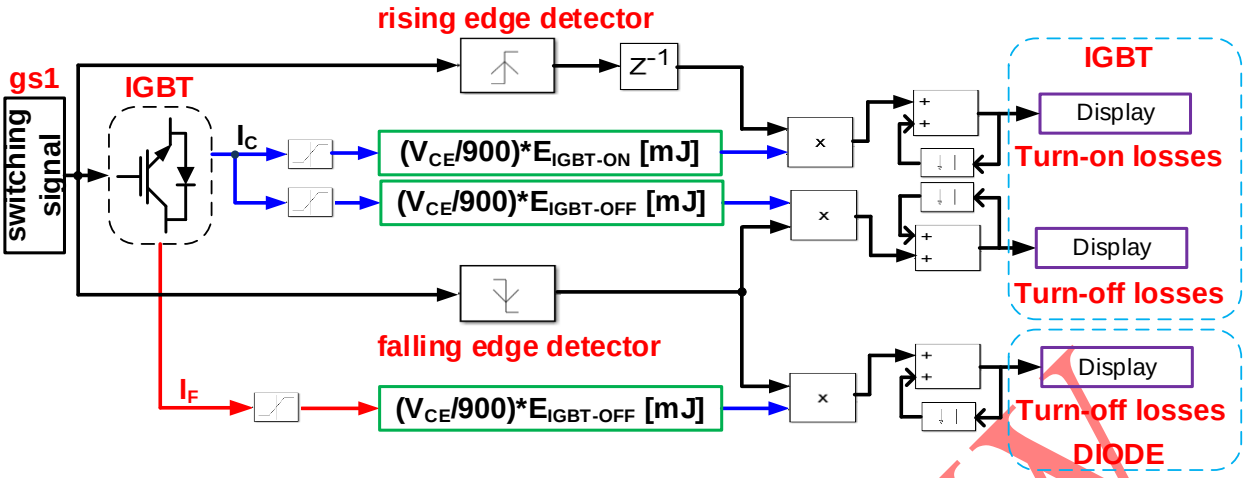


Figure 9. *The implementation of turn-on/off switching loss calculations in simulation environment*

Figures 10 and 11 illustrate various signal measurements taken during loss calculations for one IGBT and one diode of the PUC-MLI, respectively. For clarity, a low value of $f_c = 100\ Hz$ is applied to the PD-PWM method with m_{ind}=0.95 when the inverter feeds its load.

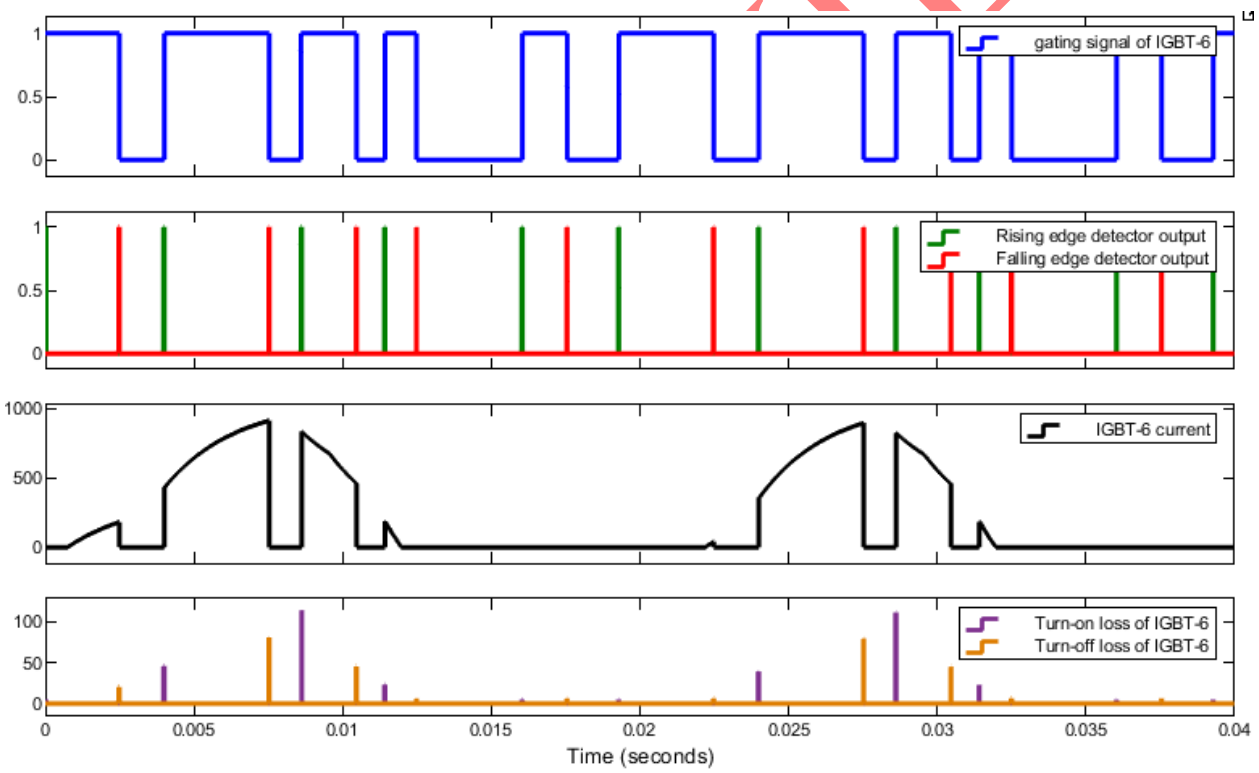


Figure 10. *The measurements of turn-on/off switching loss calculation for IGBT-6*

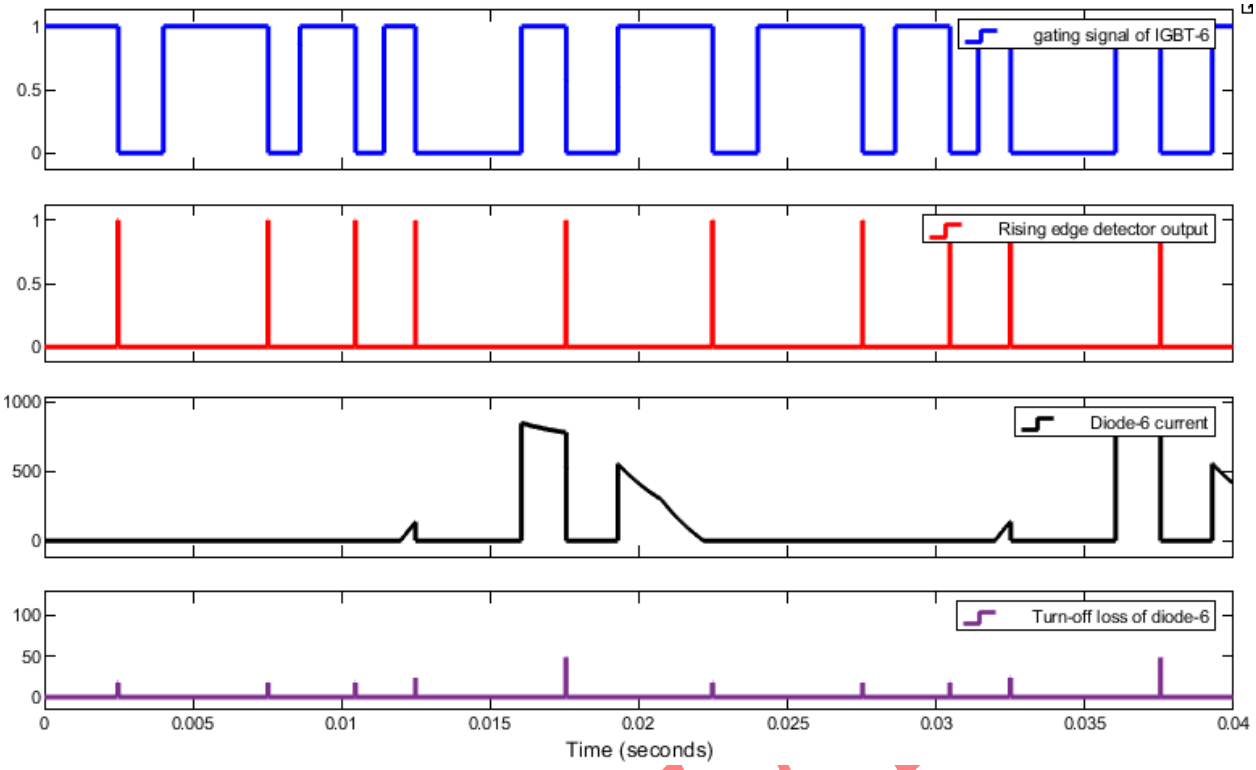


Figure 11. *The measurements of turn-off loss calculation for diode-6*

5. RATING DETERMINATION OF PUC-MLI

When designing an inverter, normally the voltage and current ratings of the semiconductor devices are typically determined based on the required power and voltage ratings of the inverter. However, in this study, the power and voltage ratings of the inverter are determined from the chosen semiconductor ratings. According to the datasheet of the IGBT (FF600R17ME4), the rated voltage and current of the IGBT are $1700V$ and $600A$, respectively. The required DC voltage sources for seven-level PUC operation are $V_{dc1} = 3E$ and $V_{dc2} = E$. During simulations, the maximum blocking voltage is observed as $3E$ for all six-IGBTs, so the value of E is determined by the voltage rating of the IGBT. For a 50% safety margin, $E = 0.5 * 1700/3 \cong 285V$, so V_{dc1} and V_{dc2} are specified as $855V$ and $285V$, respectively. With these adjustments, the open-circuit output voltage of the inverter is approximately $573V$ for all PWM methods at $f_c = 10\ kHz$. Since the continuous DC collector current rating of the IGBT is 600 A, this value should not be exceeded for each IGBT. The rated load impedance at a given power factor is determined based on this constraint, since the open-circuit output voltage of the inverter has been previously specified. Under these conditions, the rated load is calculated as $Z_L = 1.0\Omega$ at 0.8 pf lagging. When this load is connected to the inverter's output terminal, the maximum DC collector current is observed as $242A < 600A$, and the maximum peak collector current is $810A < 1200A$ [41]. So, with this load, all the current conditions are met for the IGBTs in the PUC-MLI. Finally, the apparent power rating of the inverter at the fundamental frequency can be determined as $S = V_{load(rms)} x I_{load(rms)} = 569.3x569.3 = 324.1\ kVA$ when the harmonics are neglected. Table 5 summarizes the specifications of the single-phase PUC-MLI used in the case studies.

Table 5. *Rated inverter parameters used in simulation studies*

PUC-MLI parameters	**Value**
Voltage level count	7
Output power	324.1kVA
Output rms voltage (*fundamental*)	569.3V at $m_{ind} = 0.95$
Load power factor	0.8 lagging

DC link voltage, V_{dc1}, V_{dc2}	855V, 285V
Maximum switching frequency, $f_{sw(\max)}$	10kHz [41]

6. COMPARATIVE NUMERICAL STUDIES

The parameters provided in Tables 4 and 5 are used in the simulation environment to conduct the numerical studies on the seven-level PUC-MLI. These studies aim to gather data necessary for evaluating the output voltage waveform, output current quality, and semiconductor losses obtained for various case studies by altering the modulation index, carrier frequency and PWM method. The simulation model offers flexibility, allowing users to select the PWM method, modulation index, phase shift of the output voltage waveform, carrier frequency, fundamental frequency, and load parameters of the PUC-MLI. The sample time is set as $T_s = 2\mu s$ and the period is specified as $T_{period} = 20ms$ for 50-Hz inverter output. The simulation time is always chosen as $T_{total} = kT_{period}$, where $k \geq 4$ is an integer.

6.1. Case-1: DC Bus Utilization Evaluation

Firstly, the output voltage and current waveforms of the PUC-MLI are analyzed to verify whether the correct voltage levels are achieved at the inverter output. Since the waveforms of the level-shifted PWM methods are found to be similar, only PD-PWM is compared to PS-PWM. As shown in Figure 12, symmetrical AC voltage waveforms are obtained in all PWM methods for all m_{ind} values under rated load conditions. Notably, the voltage levels increase as m_{ind} rises. For very low m_{ind}, such as 0.15, three voltage levels are present at the output, while this number increases to seven for $m_{ind} = 0.95$. Since the rated load is inductive, the current waveform approaches a sinusoid as m_{ind} rises. Secondly, the impact of changing f_c on the output voltage of the PUC-MLI is investigated for low, medium, and high m_{ind} values under rated load conditions. Table 6 summarizes the fundamental rms output voltage under various f_c and m_{ind} values. Across all PWM methods, altering f_c for a fixed m_{ind} has negligible effect on the fundamental component of the output voltage, with variations remaining below 1V. Furthermore, all level-shifted PWM methods yield identical output voltages for varying f_c values at the same m_{ind}. When comparing the PS-PWM method to level-shifted PWM methods as a whole, voltage variations of up to 0.5% are observed for a given m_{ind}. The maximum DC-bus utilization factor for the inverter across all PWM methods occurs at the maximum value of $m_{ind} = 1$, reaching 66.6% of the maximum DC bus voltage of $3E = 855V$.

Table 6. *Fundamental output rms voltage of PUC-MLI under rated load*

PWM method	$m_{ind} = 0.35$		$m_{ind} = 0.65$		$m_{ind} = 0.95$	
	f_c=1 kHz	f_c=10 kHz	f_c=1 kHz	f_c=10 kHz	f_c=1 kHz	f_c=10 kHz
PD-PWM	208.3 V	207.9 V	388.9 V	389.2 V	569.4 V	569.0 V
POD-PWM	208.3 V	207.9 V	388.9 V	389.2 V	569.4 V	569.0 V
APOD-PWM	208.3 V	207.9 V	388.9 V	389.2 V	569.4 V	569.0 V
PS-PWM	208.0 V	208.6 V	388.3 V	389.8 V	569.7 V	569.5 V

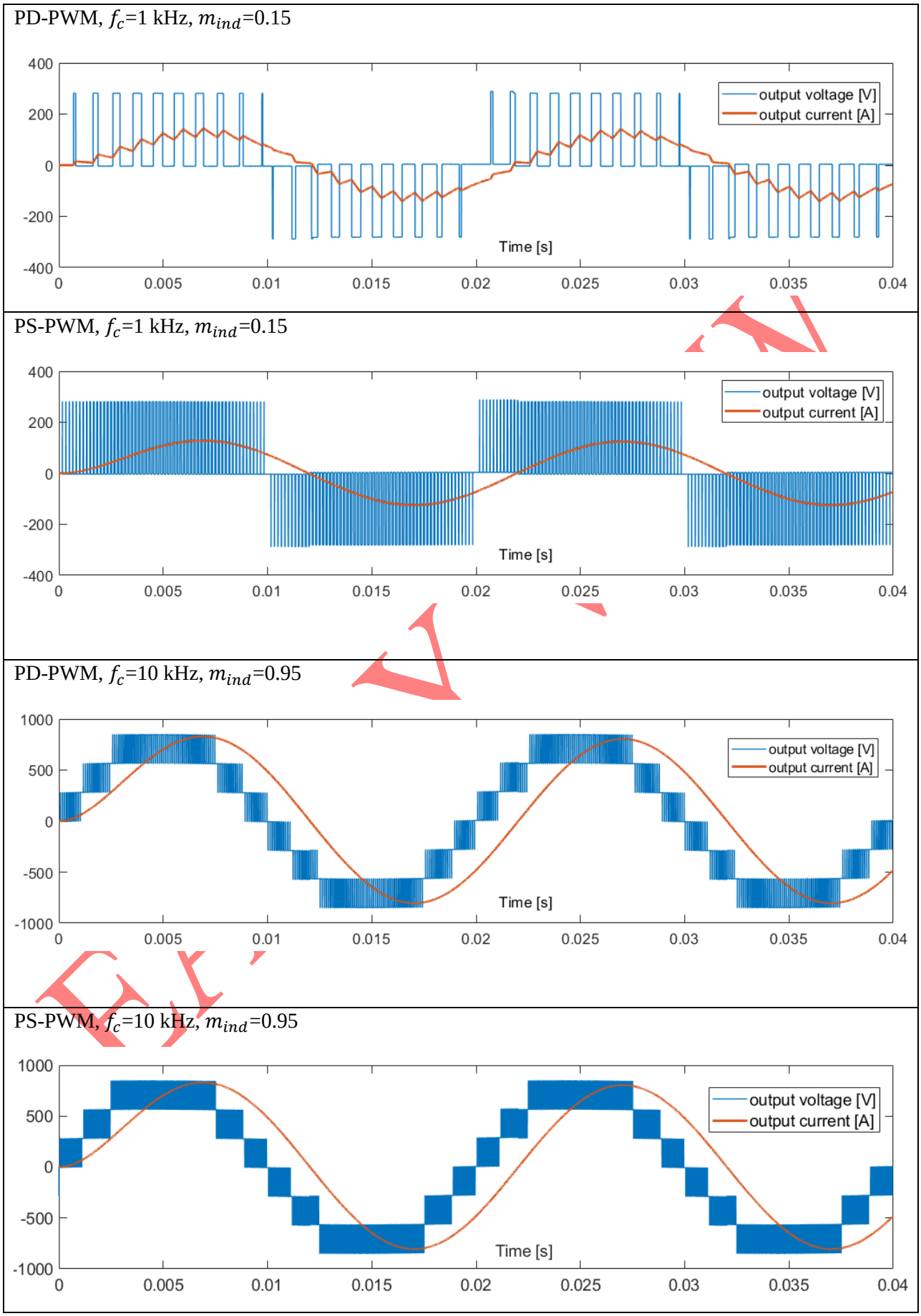
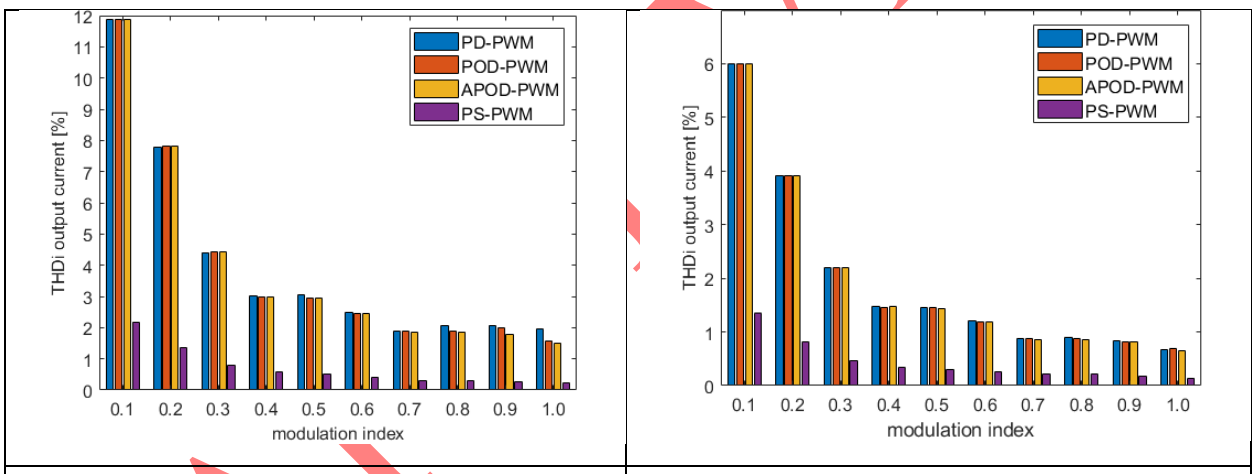


Figure 12. *Output voltage and current waveforms of PUC-MLI under rated load*

6.2. Case-2: Output Current THD Evaluation

In this case study, the THD of the output current waveform of the PUC-MLI is analyzed for each multicarrier PWM method under rated load conditions. The DC sources of the inverter are set to their rated values, with $V_{dc1} = 285V$ and $V_{dc2} = 855V$, respectively. Figure 13 depicts the current THD measurement results for the PUC-MLI at various f_c and m_{ind} values. The carrier frequency f_c is incrementally increased from 1 kHz to the permissible limit of 10 kHz for the selected IGBT model (FF600R17ME4). The modulation index m_{ind} is varied from 0.1 and 1.0 in steps. Upon initial examination, the results reveal that the THD of the output current waveform decreases as the carrier frequency, regardless of the PWM method used. Furthermore, an increase in the modulation index m_{ind} leads to a reduction in THD due to the corresponding rise in the number of voltage levels at the output, resulting in an output voltage that more closely resembles a sinusoidal waveform. When compared to level-shifted PWM approaches, the PS-PWM method consistently results in significantly lower current THD. Even at a low carrier frequency of f_c = 1 kHz, for $m_{ind} \geq 0.3$, PS-PWM method always keeps THD within the bound of less than 1%, which is below the 5% threshold set by the IEEE-519 power quality standard. Generally, level-shifted PWM methods yield similar quality current waveforms, with minor deviations in THD performance of the inverter as the carrier frequency increases. Therefore, the power quality of the PUC-MLI does not strongly depend on the choice among level-shifted PWM methods. In more detail, $m_{ind} > 0.7$, APOD-PWM method provides generally lower THD results among all level-shifted PWM methods, with the POD-PWM coming in second. This case study highlights the importance of considering power quality when selecting a PWM method for PUC-MLI applications, suggesting that the PS-PWM method may be a suitable choice if the other factors are disregarded.



(a) The carrier frequency $f_c = 1kHz$.

(b) The carrier frequency $f_c = 2kHz$.

(c) The carrier frequency $f_c = 5kHz$.

(d) The carrier frequency $f_c = 10kHz$.

Figure 13. *The current THD measurement results for PUC-MLI under rated load at different f_c and m_{ind} values*

6.3. Case-3: Semiconductor Loss Evaluation

The semiconductor losses of the PUC-MLI have been thoroughly analyzed in this case study. Initially, the total semiconductor losses, denoted as P_{LOSS} in (13), are numerically compared across various multicarrier PWM methods at varying carrier frequencies, as illustrated in Figure 14. It is observed that level-shifted PWM techniques, such as PD, POD, and APOD, exhibit nearly identical losses under rated load conditions for all modulation indices and carrier frequencies. However, the PS-PWM method results in semiconductor losses approximately 3.3 times higher on average compared to the level-shifted PWM methods. Additionally, it is noted that increasing the modulation index generally leads to higher semiconductor losses for all PWM methods, primarily due to the increased load current. However, in case of PS-PWM method operating at carrier frequencies of 5 and 10 kHz, increasing the modulation index differently effects the overall losses of the PUC-MLI. Specifically, for modulation indices greater than 0.6, the overall losses do not exhibit the nearly linear increase typically observed when the PS-PWM method is applied to the PUC-MLI under rated load conditions.

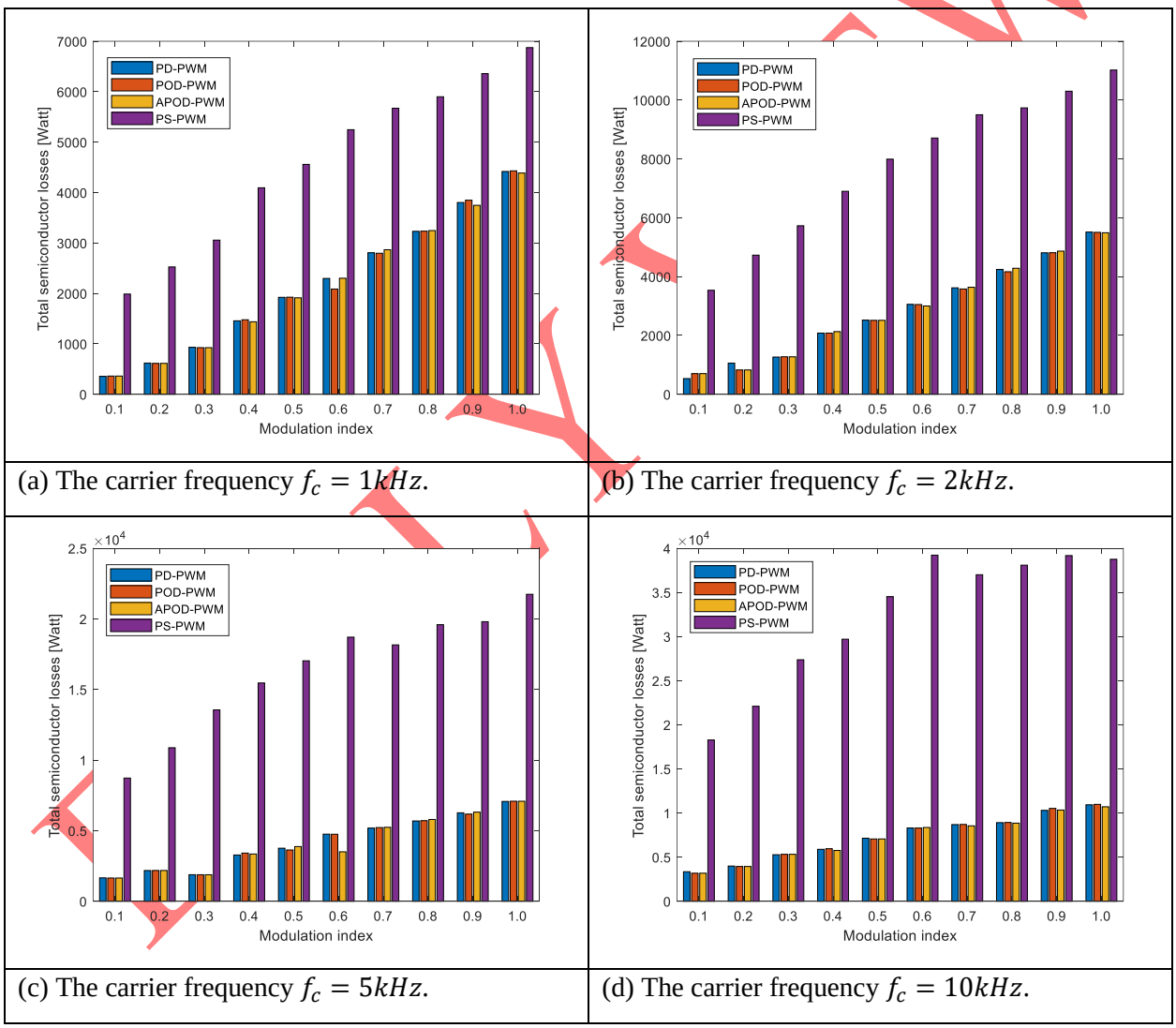
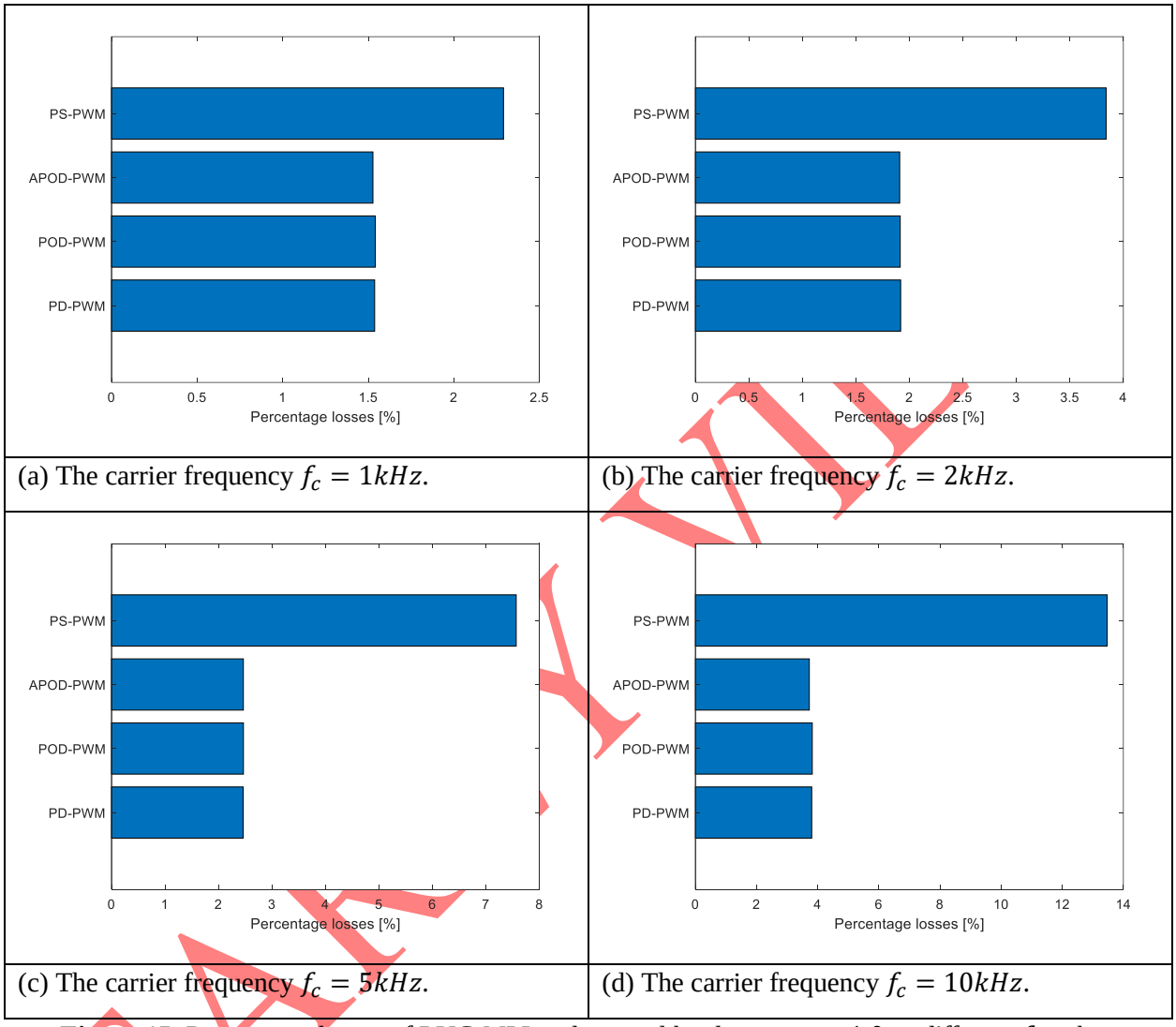


Figure 14. *Total semiconductor losses of PUC-MLI under rated load at different f_c and m_{ind} values*

Figure 15 shows the calculated percentage loss of the PUC-MLI under rated load conditions with $m_{ind} = 1.0$ at various carrier frequencies. The percentage loss of the inverter ($P_{LOSS\%}$) can be calculated as,

$$P_{LOSS\%} = \frac{P_{LOSS}}{P_{LOAD}} x100\% \quad (14)$$

where, P_{LOAD} is the active power dissipated by the rated load at fundamental frequency. The results reveal that they are consistent with the results presented in Figure 14. The losses observed for level-shifted PWM methods, such as PD, POD, and APOD, are nearly identical, averaging 2.48% across all carrier frequencies. In contrast, when the PS-PWM method is employed as the switching technique for the IGBTs, the average loss increases significantly, reaching approximately 17% across all carrier frequencies. This represents nearly a sixfold increase in losses compared to those obtained with level-shifted PWM methods.



(a) The carrier frequency $f_c = 1kHz$.

(b) The carrier frequency $f_c = 2kHz$.

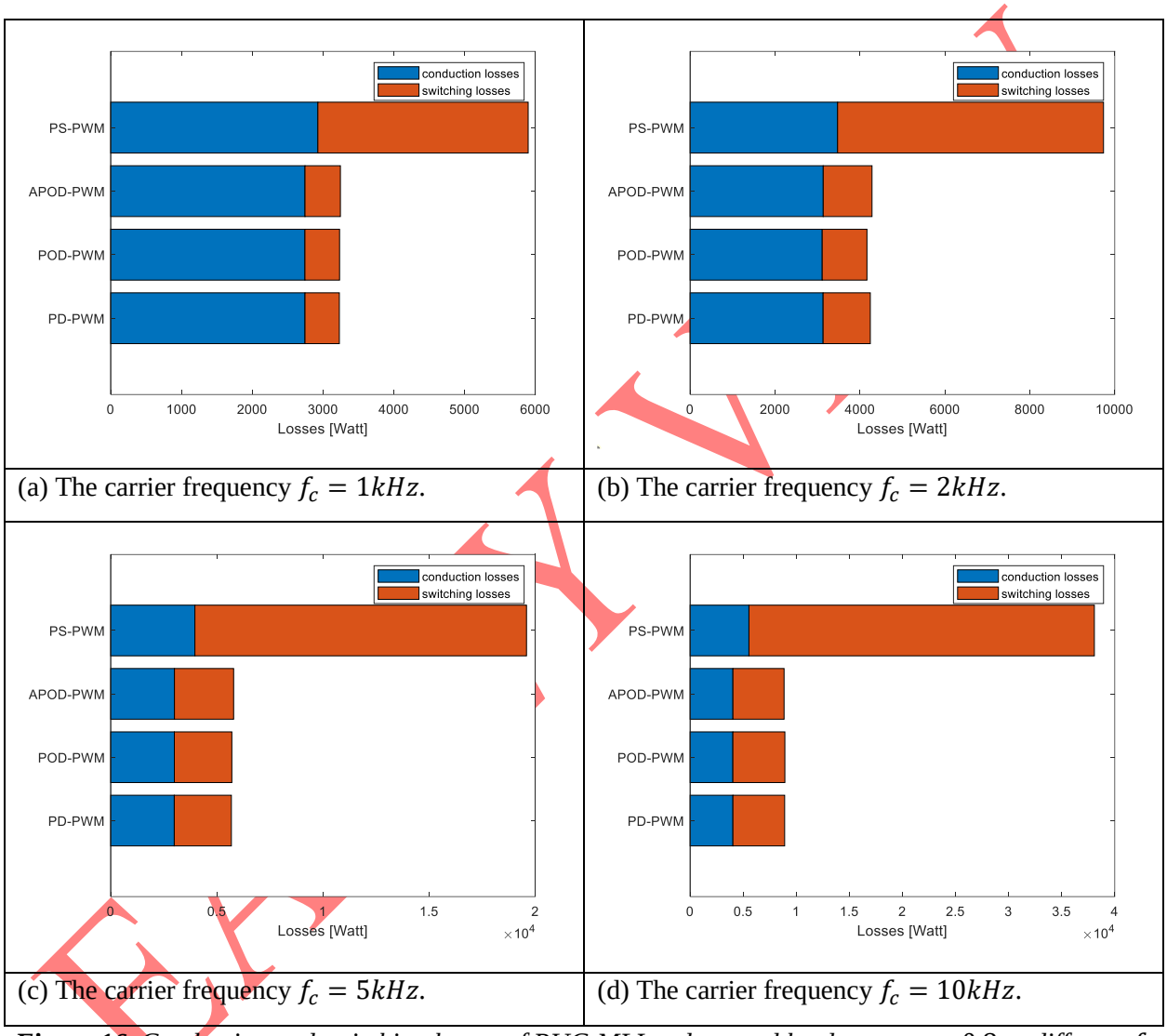
(c) The carrier frequency $f_c = 5kHz$.

(d) The carrier frequency $f_c = 10kHz$.

Figure 15. *Percentage losses of PUC-MLI under rated load at* $m_{ind} = 1.0$ *at different* f_c *values*

Figure 16 depicts the conduction and switching losses of the PUC-MLI at $m_{ind} = 0.8$ under various carrier frequencies when different PWM methods are applied under rated load conditions. At first glance, it is evident that, PS-PWM produces significantly higher switching losses compared to level-shifted PWM methods under identical operating conditions. Moreover, it has been observed that PD-PWM, POD-PWM, and APOD-PWM methods yield nearly identical conduction losses, whereas the PS-PWM method results in higher conduction losses under the same conditions. Another key finding is that conduction losses are less sensitive to variations in carrier frequency compared to switching losses. A detailed analysis reveals that switching losses increase from approximately 6 kW to 10 kW as the carrier frequency rises from 1 kHz to 2 kHz. For higher carrier frequencies, switching losses for the PS-PWM method escalate rapidly, ranging from around 20 kW to nearly 40 kW, leading to an inverter efficiency of less than 90%. At lower carrier frequencies, the majority of semiconductor losses for level-shifted PWM methods are attributed to the internal resistances of the semiconductors. However, as the carrier frequency increases, this proportion approaches approximately 50%. For the PS-PWM method, however, more than 50% of the total losses are

attributable to the switching phenomenon, which becomes increasingly significant as the carrier frequency rises. Figure 17 illustrates the average switching counts obtained for one IGBT among the six. The measurements are averaged over one operating period of the PUC-MLI ($T_{period} = 20ms$), accounting for both turn-on and turn-off conditions. It is clearly seen that the switching counts are not uniformly distributed among the switching methods with noticeable variations. There is a significant difference in switching counts between level-shifted and phase-shifted PWM methods under rated load conditions across various carrier frequencies and modulation indices. The PS-PWM method consistently produces much higher switching counts than level-shifted PWM methods. At carrier frequencies of 1 kHz and 2 kHz, this ratio is approximately 5, while for carrier frequencies of 5 kHz and 10 kHz, the ratio exceeds 5.



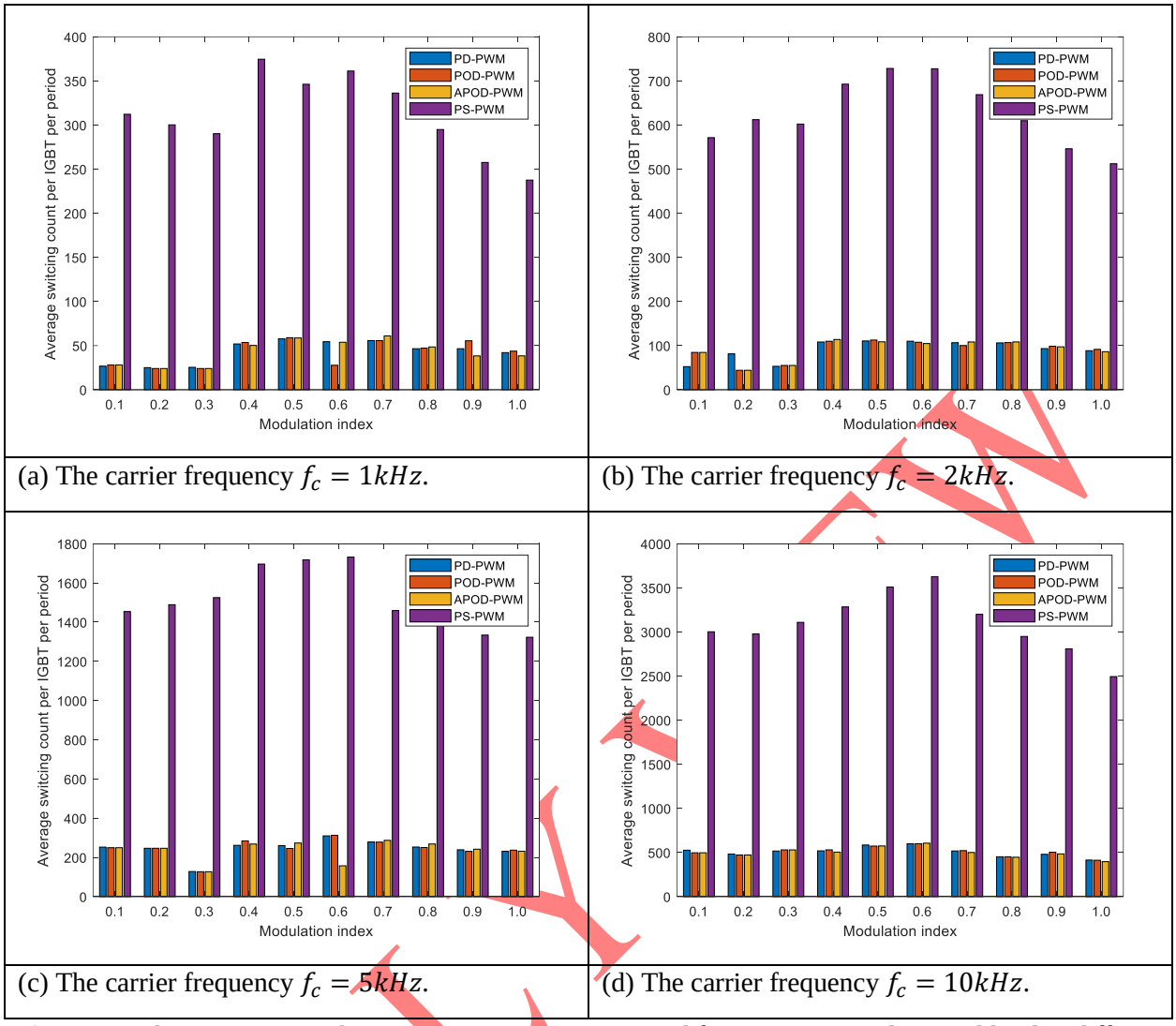
(a) The carrier frequency $f_c = 1kHz$.

(b) The carrier frequency $f_c = 2kHz$.

(c) The carrier frequency $f_c = 5kHz$.

(d) The carrier frequency $f_c = 10kHz$.

Figure 16. *Conduction and switching losses of PUC-MLI under rated load at $m_{ind} = 0.8$ at different f_c values*



(a) The carrier frequency $f_c = 1kHz$.

(b) The carrier frequency $f_c = 2kHz$.

(c) The carrier frequency $f_c = 5kHz$.

(d) The carrier frequency $f_c = 10kHz$.

Figure 17. *The average switching count per IGBT per period for PUC-MLI under rated load at different* f_c *and* m_{ind} *values*

6.4. Discussion

The numerical results from the case studies demonstrate that the harmonic and loss performance of the PUC-MLI are significantly influenced by carrier specifications and the choice of carrier frequency. The findings reveal how varying degrees of modulation freedom affect the inverter's output harmonic content and switching losses. Based on these results, it can be concluded that the PS-PWM method is generally not a practical choice as a switching method for the PUC-MLI due to its high semiconductor losses, unless other considerations outweigh this limitation. However, if achieving a high-quality output voltage waveform is a priority, the PS-PWM method may be a viable option despite its higher semiconductor losses compared to level-shifted PWM methods, as it consistently produces lower harmonic content. On the other hand, there is little to no significant difference when choosing among level-shifted PWM methods (PD-PWM, POD-PWM, and APOD-PWM), as all of them generate comparable semiconductor losses and output harmonics under identical operating conditions. The decision between these methods can instead be guided by features such as the self-capacitor voltage balancing capability of the inverter.

7. CONCLUSIONS

The conventional MLIs (NPC, FC, and CHB) are the fundamental MLI options which suffer from significant disadvantages, such as high control complexity and increased cost as the output voltage level rises. To address these challenges, the PUC-MLI topology has been introduced in the literature, offering a

reduced device count and lower costs compared to conventional MLI topologies. However, the switching generation method for the PUC-MLI is not straightforward, in which additional steps should be taken to apply the classical multicarrier PWM methods to control this inverter. On the other hand, existing literature on PUC-MLI switching signal generation is often unclear and lacks detailed explanations on its design. In this study, a combinational logic circuit was designed by considering the 'sum of minterms' method, based on the traditional switching signal generation technique used for conventional CHB MLIs. This circuit functions by summing of the minterms allowing to map the input set to the output with minimal terms. The output signals of this circuit serve as the semiconductor switching signals for PUC-MLIs. The proposed method is explained step by step in a clear and detailed manner, with a generalizable structure that accommodates an increasing number of minterms as the converter's level count increases. This approach is both practical and flexible, making it suitable for adaptation to simulation and experimental studies, and contributes significantly to the existing literature. This study also presents in-depth comparative analysis of PUC-MLIs under various multicarrier PWM techniques. The proposed loss calculation models are generalizable, enabling the separation of conduction and switching losses for each semiconductor in the simulation environment. The comparative studies provide guidance for selecting the most appropriate multicarrier PWM method for PUC-MLIs. When choosing a switching method, a trade-off exists between harmonic performance and semiconductor losses. While the PS-PWM method reduces harmonics, it results in higher losses. Conversely, level-shifted PWM methods reduce losses but introduce greater output distortion. This study offers a comprehensive numerical comparison to assist in selecting the most suitable multicarrier PWM method for PUC-MLIs.

CONFLICTS OF INTEREST

No conflict of interest was declared by the author.

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