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ADVANCING MEMORY DENSITY: A NOVEL DESIGN FOR MULTIPLE-BIT-PER-CELL PHASE CHANGE MEMORY

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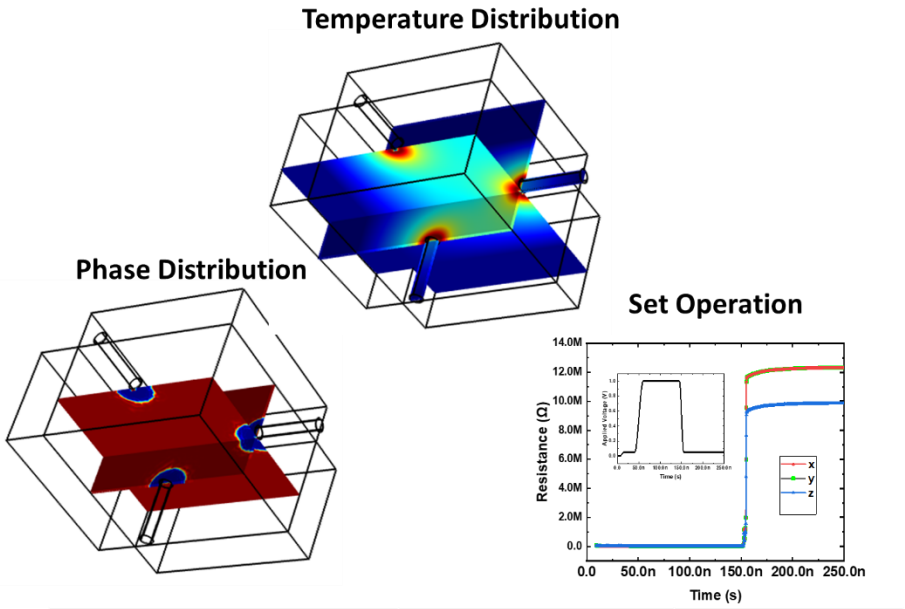
Highlights

- Innovative Multiple-Bit-Per-Cell PCM Design
- Use of GST for Superior Performance
- Detailed 3D Temperature and Phase Distribution Analysis
- Significant Resistance Modulation
- Optimized Design for Enhanced Device Performance

Graphical Absract



Design Concepts	Resistance level	Storage information
General design (REF)	2 states	1 bit
Middle resistance level device(REF)	3 and/or 4 states	1 or 2 bit
New design	**2 states (x3 from direction)**	**1 bit x 3 = 3 bit**

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ABSTRACT: Multiple-bit-per-cell phase-change memory (MPCM) has emerged as a promising solution to address the escalating demands for high-density, low-power, and fast-access memory in modern computing and data storage systems. This paper presents a novel device design aimed at enabling multiple bits per cell in phase-change memory, thereby significantly enhancing memory density while maintaining performance and reliability. Leveraging innovative material compositions and advanced fabrication techniques, the proposed design demonstrates the potential to push the boundaries of memory capacity, efficiency, and scalability. Through comprehensive simulation analysis and performance evaluations, we showcase the feasibility and advantages of the new device design, highlighting its potential to revolutionize memory architectures and meet the evolving needs of next-generation computing systems.

Keywords: *Phase Change Memory, Multiple-Bit-Per-Cell, Finite Element Modeling, Novel Design, Memory Architecture*

1. INTRODUCTION

As the demand for high-density, low-power, and fast-access memory continues to escalate in modern computing and data storage systems, researchers are exploring novel avenues to meet these ever-growing requirements [1-6]. Among the promising contenders in this landscape, multiple-bit-per-cell phase-change memory (PCM) stands out as a transformative technology with the potential to revolutionize memory architectures [7-9]. Traditional PCM technology, known for its non-volatile characteristics and scalability, has already demonstrated its prowess in various applications [10-13]. However, to further enhance its storage capacity and efficiency, researchers have turned their attention towards enabling multiple bits per cell, thereby exponentially increasing the memory density without compromising on performance [14-19]. For this purpose, common strategies have included modifying the phase change properties through graded doping and the use of multilayer stacks of phase change alloys. Graded doping involves the incorporation of elements such as nitrogen in $Ge_2Sb_2Te_5$ [20], selenium in GeSb[21], and the formulation of $Ga_2Te_2Sb_5$[22], each of which adjusts the material properties to optimize switching behavior. Alternatively, multilayer stacks combine different phase change materials with varying phase transition characteristics, such as Sb_2Te_3 with $Ge_2Sb_2Te_5$[23, 24], GeTe with $Ge_2Sb_2Te_5$[25], and InSe with $Ge_2Sb_2Te_5$[26].

Through a comprehensive analysis of the underlying principles, fabrication processes, and performance characteristics, this study explores the potential of a novel multiple-bit-per-cell phase change memory (MPCM) device, specifically utilizing $Ge_2Sb_2Te_5$ (GST) as the base phase change material. Over the years, various PCM devices utilizing different phase change alloys have been constructed and placed, demonstrating the diverse approaches in phase change memory technology, however, GST has emerged as the most extensively used and studied due to its exceptional thermal and electrical properties. The widespread adoption and research interest in GST highlight its effectiveness in delivering reliable and efficient performance for PCM applications. By presenting simulation results and performance evaluations, we demonstrate that our innovative design achieves higher storage capacities while maintaining reliability and endurance. The multiple-bit-per-cell capability, facilitated by the superior

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phase change characteristics of GST, represents a significant advancement in memory technology. This advancement provides a promising pathway to meet the increasing demands of modern computing and data storage applications. Our study aims to contribute to this evolving field by introducing a groundbreaking device design based on GST and offering insights into its potential impact on future memory architectures, thereby paving the way for next-generation data-centric solutions.

2. MATERIAL AND METHODS

2.1. Device Structure

A 50 nm-thick active layer based on phase-change material GST is encapsulated between three heater-metal electrodes made of 30 nm WTi. These electrodes are strategically positioned from three distinct directions: x, y, and z, as depicted in Figure 1 b). Each heater electrode corresponds to a bottom contact, which acts as the ground terminal. During current distribution, the electrodes also serve as thermal reservoirs. Adjacent to the WTi layer, a stack of Ta and Au layers is utilized. Additionally, Al_2O_3 serves as an isolation barrier to protect the device from environmental influences. This sophisticated layered architecture ensures efficient performance, management of the heat distribution, and enhanced durability of the device from the all directions.

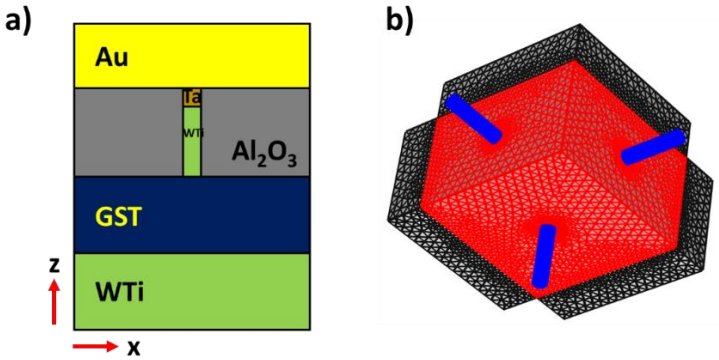

Figure 1. a) General phase change memory cell structure: 6 nm diameter circular heater contact and 80x80x50 nm GST layer. Ta/Au stack acts as the contact electrode for devices, and Al_2O_3 is used as isolation. b) 3-D structure of PCM cell (blue circulars are WTi heater contacts, red rectangular is GST and blacks are WTi bottom contacts)

2.2. Finite Element Model

In the realm of reset operation of phase-change simulation, traditional approaches have largely relied on two-dimensional electro-thermal and crystallization models [27-29]. However, for the nuanced requirements of a PCM device, we have innovatively developed a 3-D finite element simulation. This advanced model also emphasizes the significance of the top contact shape in modifying a mixture phase level, a concept elaborated further by Cinar in 2015[30]. In the present study, aimed at the design of a multi-bit-per-cell memory device, we employed 3D finite element simulations within a cell featuring a single active layer of GST with three heater electrodes. These simulations intricately incorporate phase-change kinetics, electrical properties, thermal characteristics, and percolation phenomena. The simulation framework is built upon an iterative approach, utilizing coupled differential equations that are temperature-dependent. Additionally, the inclusion of the Seebeck coefficient allows for the consideration of thermoelectric effects[31, 32], as well as adding Peltier effect [33]. The dynamics of the switching process exhibit a high sensitivity to both the programming current distribution and defect density. This is attributed to the inhomogeneous current flow and varying crystallite distribution during the phase-change process. To accurately capture these effects within the simulation, optimization of nucleation and

growth rates becomes imperative, as highlighted by Cinar (2015). Furthermore, our simulation framework employs adaptive meshing strategies. Specifically, the mesh elements for the phase-change layer ranges of 1x1x1 nm^3, while the contact regions (not for heater) are represented with a maximum mesh size of 2x2x2 nm^3. This granularity ensures a comprehensive understanding of the entire switching process. Boundary conditions are meticulously defined; the top and bottom surfaces of the metal electrodes, along with all external surfaces, are set as Dirichlet boundary conditions. Conversely, Neumann boundary conditions are applied to the interface surfaces. Given the field insulation properties of the Al_2O_3 layer, which is considered a near-perfect insulator, our simulation predominantly focuses on the top and bottom electrodes in the three specified directions, along with the GST layer, to depict the simulation results effectively. The simulation model is modular, comprising distinct submodels for electrical, thermal, and phase-change phenomena. This multiphysics approach allows for the nonlinear interactions between these submodels to be accurately represented. Each submodel is assigned specific tasks: the electrical model encompasses temperature and phase-dependent electrical conductivity variations; the thermal model addresses heat diffusion equations to calculate joule heating from electrical current, incorporating temperature and phase-dependent thermal conductivity; and finally, the phase-change model evaluates temperature-dependent nucleation and growth kinetics of crystallites, both homogeneous and heterogeneous.

Within the submodels, distinct equations are addressed based on the temperature and phase states of the materials under consideration. In the electrical submodel, the Laplace equation $\nabla.[\sigma\nabla F] = 0$ is iteratively solved, employing 10 ps time steps, for each mesh element. This is executed in tandem with the thermal submodel to derive the spatial electrical potential distribution, represented as F(x,y,z). Here, σ denotes the electrical conductivity of the materials. At ambient temperature, the electrical conductivities σ are reported as 2770 S/m for the crystalline phase and 3 S/m for the amorphous phase, as documented by Reifenberg et al. (2006). It is noteworthy that the electrical conductivity σ exhibits a temperature-dependent nature, which is further influenced by the structural phase of the GST layer. Consequently, as the temperature rises, the GST layer demonstrates increased conductivity, regardless of its phase, primarily due to the temperature-dependent σ values, with a more pronounced effect observed in the amorphous phase, as highlighted by Cinar et al. (2015).

In the thermal submodel, the electrical potential within the device gives rise to two significant parameters contributing to the heat generation, expressed as $Q = (JA)\ 2R\Delta t$, where A represents the cross-sectional area and Δt denotes the simulation time step. These parameters are the electrical current density, J, and the resistance value, R, of the material. The heat diffusion equation is employed to determine how temperature is distributed within the materials. Consequently, this heat equation is solved iteratively to derive the temperature distribution, represented as T(x,y,z).

$$C\ \partial T/\partial t - \nabla.[\kappa\nabla T] = Q + Qth \quad (1)$$

Here, C represents the heat capacity and κ denotes the thermal conductivity. The term $Qth = -TJ\nabla S$ incorporates the influence of the thermoelectric effect on heating. In this expression, S signifies the temperature-dependent Seebeck coefficient, and ∇S is defined as $dSdt\nabla T$, as referenced in studies by Cinar et al. (2015) and Fiflis et al. (2013)[34].

For the GST material, the thermal conductivity κ values at room temperature are reported as 0.7 W/(Km) for the crystalline phase and 0.3 W/(Km) for the amorphous phase, as documented by Won et al. (2012). Additionally, the Seebeck coefficient, S, is specified as 47 μV/K for the crystalline phase and 380 μV/K for the amorphous phase, as cited in studies by Cinar et al. (2015) and Fiflis et al. (2013). In the simulation, the heat capacity of GST remains consistent at 202 J/(kg K) for both crystalline and amorphous phases when T<800 K. To account for the phase transition, latent heat is incorporated into the calculations using a smooth Gaussian function centered on the melting point (Tm=892 K), as outlined by Reifenberg et al. (2006) and Peng et al. (1997)[35]. It is evident from the equations and the units of the parameters that the majority of the simulation parameters are temperature-dependent. Consequently, the temperature

distribution within the device significantly influences the phase change kinetics and ultimately determines the final phases of the materials.

When a programming pulse is applied to a PCM device, several key parameters critically influence the phase transition within a specific mesh element. These parameters include local temperature, temperature-dependent activation energy, and the state of adjacent cells. Considering the factors, the mesh element undergoes a phase transition randomly within the active region, leading to the formation of crystal nuclei. These nuclei can then grow, resulting in either a homogeneous or heterogeneous phase configuration within the active region. Because of temperature differences between the active region and its surroundings, crystallization outside the active region has minimal impact on the switching process. To model the probability rate of the crystallization process, the following equation is used, which depends on the nucleation rate, In, and the growth velocity of the nuclei, Vg,

$$dP/\,dt = In\,(T)\,(1-P/N) + \mathrm{Vg}(T)\,(1-P/a0) \quad (2)$$

In the given equation, P represents the probability of crystallization, N stands for the number of molecules per unit volume, and a0 denotes the atomic jump distance. The terms In(T) and Vg(T) correspond to the temperature-dependent nucleation and growth rates, respectively. For a deeper understanding of their influence on the phase change of the material, refer to the study by Cinar (2015).
In general, to ascertain the comprehensive physical properties of semiconductors, encompassing both the crystalline and amorphous phases within, the Bruggeman effective medium approximation (EMA) proves to be a valuable method for application. Utilizing this approach, we can compute the electrical conductivity and thermal conductivity. Specifically, the electrical conductivity can be determined using the equation proposed by Bruggeman et al. (1935)[36].

$$(f, \sigma a\,\sigma c\,) = 0.25\{(2\sigma p - \sigma\,'p) + (2\sigma p - \sigma\,'p)\,2 + (8\sigma a\sigma c\,)\,\}1/2 \quad (3)$$

In the provided equation, σ_a and σ_c represent the electrical conductivities of the amorphous and crystalline phases, respectively, while f denotes the crystallization fraction. Also, $\sigma_p = (1\text{-f})\,\sigma_a + f\,\sigma_c$ $\sigma'_p = (1\text{-f})\,\sigma_c + f\,\sigma_a$. By integrating all submodels and formulas, we can obtain a comprehensive understanding of the electrical, thermal, and phase change profiles within the device, particularly for both GST layers. Once the crystallization fractions within the volume of the GSTs are determined, the device resistance during and/or after the application of a pulse can be computed.

3. RESULTS AND DISCUSSION

The innovative design of our phase change memory (PCM) device incorporates a sophisticated temperature control mechanism that ensures homogeneous temperature changes in three distinct directions, dictated by the applied voltage. This precision temperature management is crucial for the reliable operation of the switching mechanism, which transitions the phase change material between different states to store data. By carefully controlling the voltage, the device can induce temperature gradients along the x, y, and z axes, allowing for the precise manipulation of the material's phase. This multi-directional temperature modulation enables the PCM to achieve clear and distinct phase states, essential for accurately representing multiple data levels within each cell. The homogeneous temperature distribution across all three directions ensures consistent and repeatable phase transitions, thereby enhancing the reliability and efficiency of the data storage process. This advanced thermal management approach not only improves the device's performance and data integrity but also contributes to its ability to store a higher density of information, pushing the boundaries of current memory technology.

A detailed 3-D illustration of temperature distribution is presented in Figure 2. These simulations reveal the temperature distribution within the GST layer when subjected to distinct programming voltage pulses: Figure 2a) 1 V applied in the z direction (Tmax = 1029 ^{0}C), 0.8 V in the x direction (Tmax = 658 ^{0}C), and 0.6 V in the y direction (Tmax = 532 ^{0}C), Figure 2b) 1 V applied in the x and z directions (Tmax =

1061 ^{0}C) and 0.6 V in the y direction (Tmax = 519 ^{0}C), and Figure 2c) 1 V applied uniformly in the x, y, and z directions, (Tmax = 1077 ^{0}C).

Each voltage pulse maintains a duration of 100 nanoseconds with a trailing edge of 10 nanoseconds. The simulations indicate that the temperature distribution within the GST layer is homogeneous in all directions due to contact shape, ensuring even thermal management across the material. Notably, the maximum observed temperature varies with the amplitude of the applied voltage, reflecting how different voltage pulse configurations affect the thermal profile. Higher voltages result in higher peak temperatures, which, in turn, influence the phase change behavior within the GST layer. Consequently, each voltage configuration leads to distinct temperature distributions and maximum temperature values, inducing various phase transitions in the GST material. This comprehensive analysis underscores the critical relationship between applied voltage amplitude and thermal behavior in phase change memory devices, providing significant insights into how these variations impact the material's phase state and overall device performance.

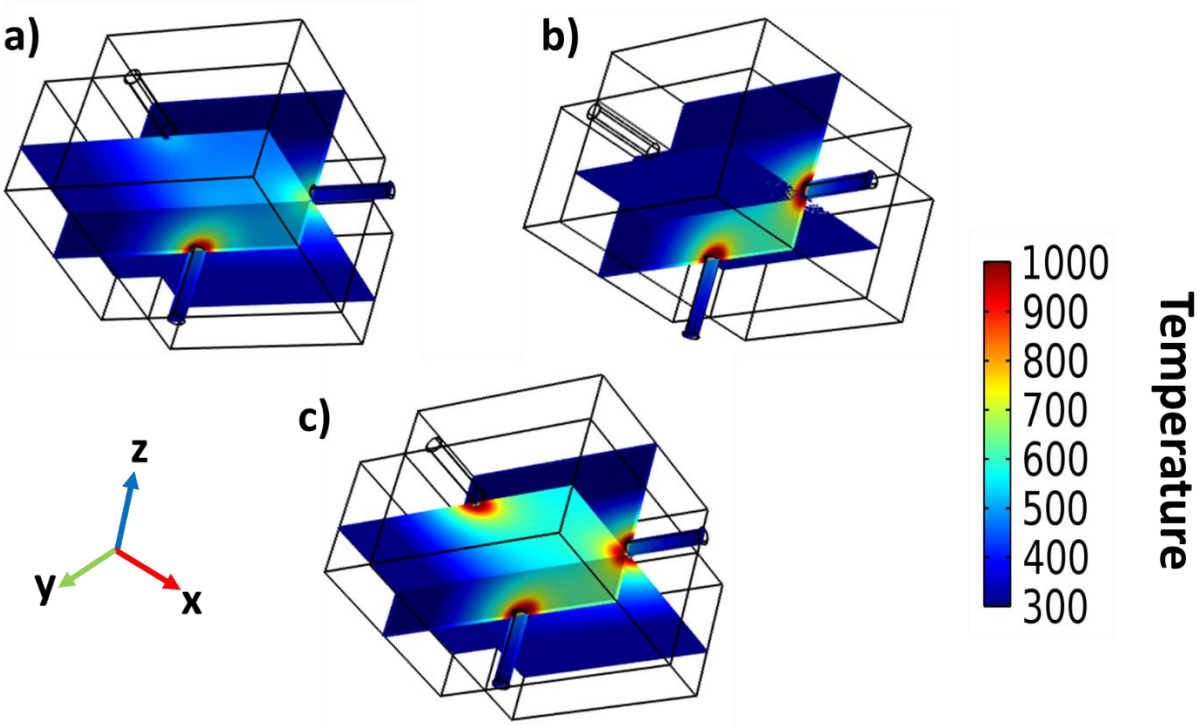

Figure 2. 3-D illustration of temperature distribution is plotted in three 6 nm circular top contact heaters device. The simulations depict the temperature distribution within the GST layer during programming voltage pulses with the following configurations: a) 1 V in the z direction, 0.8 V in the x direction, and 0.6 V in the y direction b) 1 V applied in the z and x directions and 0.6 V in the y direction, and c) 1 V applied in all three directions,. Each pulse has a duration of 100 ns with a trailing edge of 10 ns. This comprehensive analysis provides insights into how different voltage conditions affect the thermal profile within the GST layer.

As voltage is applied, it generates a corresponding temperature gradient within the material. When the temperature reaches specific thresholds, it causes the material to switch between amorphous and crystalline phases. Each phase has distinct electrical properties, such as different resistances, which can be reliably read and written to represent multiple bits of data. Due to the design concept and thermoelectric effects, these short-range thermal interactions are crucial for the performance of such devices.

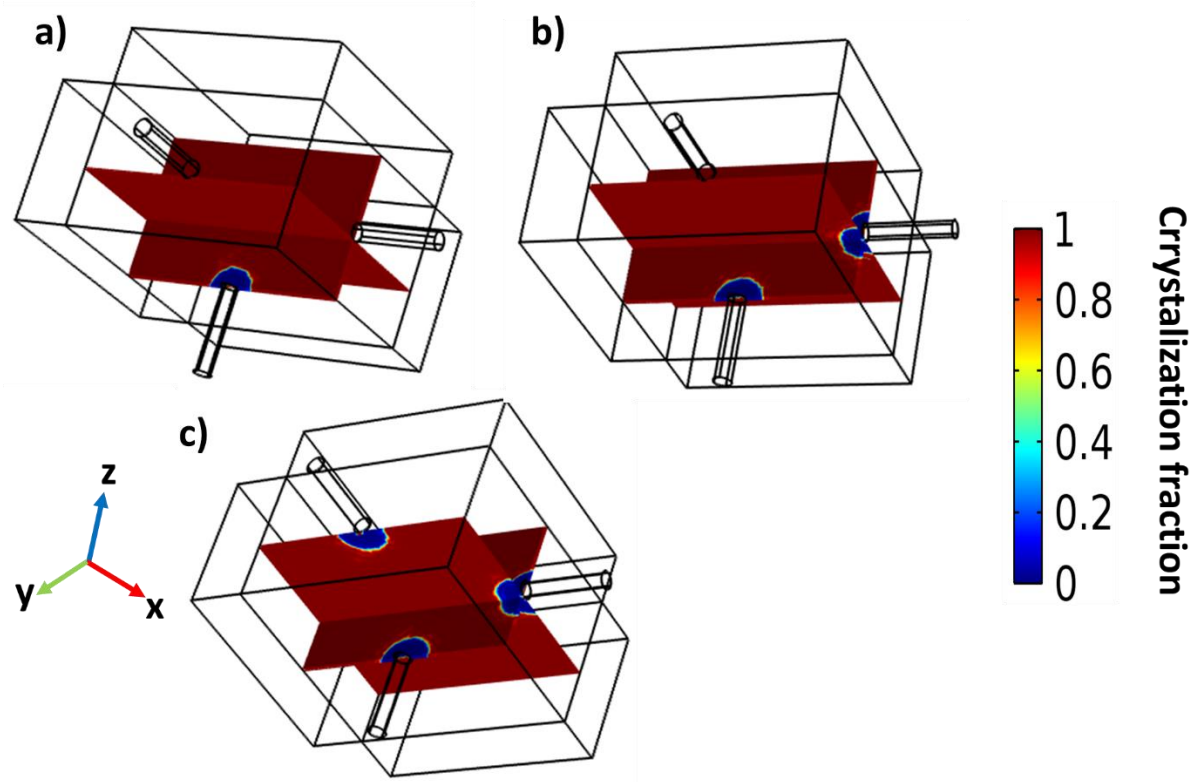

Figure 3. The crystallization fraction, f within the PCM layer of circular top contacts PCM cells is depicted after applying distinct programming voltage pulses: a) 1 V in the z direction, 0.8 V in the x direction, and 0.6 V in the y direction b) 1 V applied in the z and x directions and 0.6 V in the y direction, and c) 1 V applied in all three directions, using a 100 ns reset pulse with a 10 ns trailing edge. The color scale represents f =1 (red) for crystalline phases and =0 (blue) for amorphous phases. A vertical and horizontal cross-sections of the device, taken through the center, illustrates how different pulse amplitudes result in varying device resistances, namely phase differences.

From the simulation results depicted in Figure 3, it is evident that the phase distribution varies significantly depending on the applied voltage pulse amplitude. The crystallization fraction, f within the PCM layer is illustrated after applying three distinct programming voltage sequences: Figure 3a) 1 V in the z direction, 0.8 V in the x direction, and 0.6 V in the y direction, Figure 3b) 1 V applied in the z and x directions, and 0.6 V in the y direction and Figure 3c) 1 V applied uniformly in all three directions. Each programming pulse has a duration of 100 ns with a trailing edge of 10 ns. Vertical and horizontal cross-sections of the device, taken through the center, visually demonstrate how these different pulse amplitudes lead to varying device resistances, reflecting differences in phase distribution. This analysis underscores the impact of applied voltage pulse characteristics on the crystallization behavior of the PCM layer, highlighting its importance in optimizing device performance and functionality.

The switching process is highly sensitive and controlled, ensuring that the phase change occurs uniformly across the entire memory cell. This uniformity is crucial for maintaining data integrity and preventing partial switching, which could lead to data errors. By fine-tuning the voltage and, consequently, the temperature, we achieve precise control over the phase state of the material. This capability allows for rapid and repeatable switching between phases, enabling efficient data storage and retrieval at high speeds. The ability to reliably control phase switching through temperature changes not only enhances the performance and density of the PCM device but also underscores its potential for next-generation memory applications.

After obtaining the phase distribution, the calculated resistance values in the three directions of the device for a 1 V applied voltage pulse with a duration of 100 ns with a trailing edge of 10 ns are illustrated in Figure 4. The simulation results depict the Set operation with Figure 4a) a constant 1 V pulse and Figure 4b) varying programming voltages for a 100 ns pulse width with a 10 ns trailing edge. Figure 4a) shows

the resistance vs. time for the three directions, while Figure 4b) presents the resistance vs. applied voltage for the three directions. The obtained resistances in the x and y directions are similar, whereas the z direction exhibits different resistance values due to the thinner phase change material in the z direction.

Before the voltage was applied, the device resistance was measured at 30 kΩ in the x and y directions and 19 kΩ in the z direction. After applying the 1 V voltage pulse, the resistance increased to 12.5 MΩ in the x and y directions and 9.6 MΩ in the z direction. This represents a resistance change of approximately 420-fold in the x and y directions and 500-fold in the z direction. The data revealed that the z direction exhibited a notably lower resistance compared to the x and y directions. This lower resistance in the z direction is attributed to its reduced thickness, which facilitates a more efficient phase change due to the shorter path for current flow and heat dissipation. Consequently, the phase change material in the z direction undergoes a more uniform and complete transition, resulting in lower overall resistance.

Additionally, we conducted a detailed analysis of resistance as a function of the applied voltage (Figure 4b)). The resistance vs. voltage graph showed a characteristic abrupt switching behavior, clearly demarcating the transition from the crystalline to the amorphous state. This sharp switching is indicative of the rapid phase change occurring within the material, where a small increase in voltage induces a significant rise in resistance, marking the transformation from a highly conductive crystalline phase to a much more resistive amorphous phase. This abrupt switching is essential for the reliable operation of PCM devices, as it allows for distinct and stable data states that can be precisely controlled and detected. The ability to obtain clear resistance characteristics in multiple directions and to observe abrupt switching behavior underscores the effectiveness of our PCM device design in achieving efficient and high-density data storage.

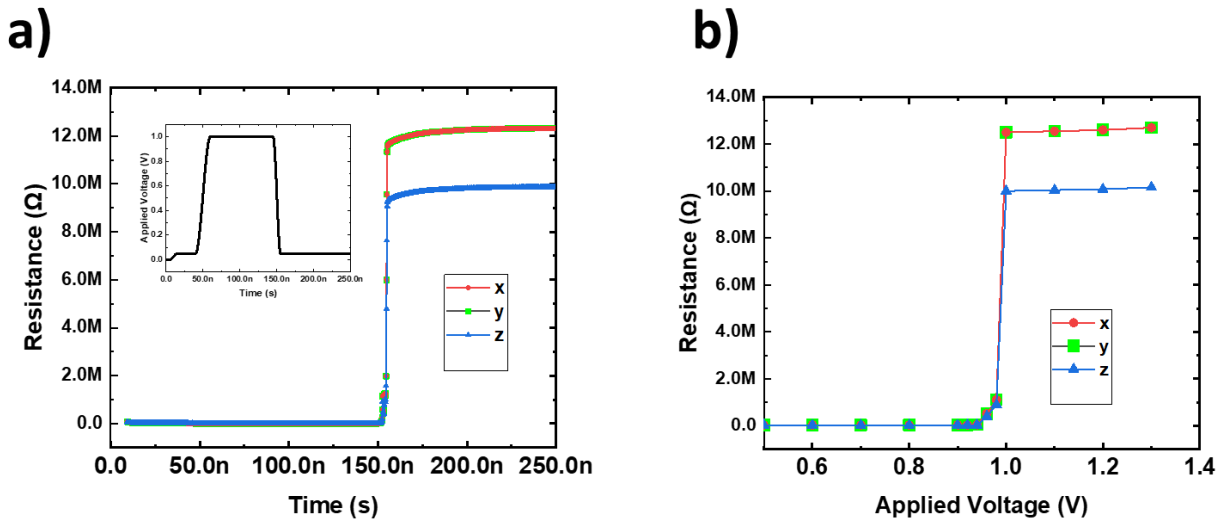

Figure 4. Simulation results of Set operation for a) 1 V and b) increasing programming voltages for a 100 ns width pulse with 10 ns trailing edge. a) Resistance vs Time for three directions and b) Resistance vs Applied Voltage in three directions.

The novel design of our phase change memory (PCM) device introduces an innovative approach to data storage, enabling significant advancements in memory technology. Unlike traditional PCM systems that store a single bit per cell by differentiating between two phases, our design utilizes a unique three-directional phase change mechanism. This approach allows each memory cell to represent three distinct levels, corresponding to 0, 1, and 2, effectively enabling the storage of three bits per cell. As a result, the device can store information at a much higher density, significantly increasing data capacity without increasing the physical footprint. Simulations confirm the clear distinction between these levels, ensuring reliable data encoding and retrieval. This breakthrough in PCM technology not only enhances storage efficiency but also paves the way for faster data access and reduced power consumption, marking a

significant leap forward in the development of high-performance, scalable memory solutions for a wide range of applications.

4. CONCLUSIONS

In summary, the introduction of our novel multiple-bit-per-cell phase-change memory (PCM) device design marks a significant step forward in memory technology. Through meticulous engineering and innovative approaches, we have demonstrated the feasibility of achieving higher memory densities while maintaining performance and reliability. This advancement holds great promise for addressing the escalating demands of modern computing and data storage systems, offering enhanced efficiency and scalability. As we continue to refine and optimize this design, we anticipate further breakthroughs in memory architectures and the realization of even more powerful computing capabilities.

Declaration of Ethical Standards

The authors declare that they have carried out this completely original study by adhering to all ethical rules including authorship, citation and data reporting.

Credit Authorship Contribution Statement

Ibrahim Çınar conceived and designed the study, conducted the experiments, analyzed the data, and wrote the manuscript.

Declaration of Competing Interest

The authors declared that they have no conflict of interest.

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Data Availability

Data supporting the findings of this study can be obtained from the corresponding author with reasonable requests to assist in scientific studies.

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