Black Sea Journal of Engineering and Science
doi: 10.34248/bsengineering.1532974

Open Access Journal
e-ISSN: 2619 – 8991

Research Article
Volume 7 - Issue 5: 1014-1021 / September 2024

DC REGULATION AND LOOP GAIN ANALYSIS OF A DC-DC SWITCH MODE POWER SUPPLY: A CASE STUDY ON A SYNCHRONOUS PWM CONTROLLED BUCK CONVERTER

Cağfer YANARATEŞ[1], Aytaç ALTAN[2]*

[1]*Gümüşhane University, Department of Electrical and Energy, Kelkit Aydın Doğan Vocational School, 29600, Gümüşhane, Türkiye*
[2]*Zonguldak Bülent Ecevit University, Department of Electrical Electronics Engineering, 67100, Zonguldak, Türkiye*

Abstract: This study investigates the DC regulation of a DC-DC buck converter operating with pulse width modulation (PWM), taking into account the internal resistance of the coil and the on-resistance of the switching device. The effect of these parameters on the input/output disturbances is analyzed in continuous-conduction mode under constant frequency voltage mode control. The study also explores the effect on loop gain using the IRU3037 8-pin IC synchronous PWM controlled buck converter. The transfer function of the IRU3037 IC is derived from datasheet values using state-space averaging and AC small signal methods. A Type II compensator is then designed based on the derived transfer function. In addition, the step response characteristics of the open-loop and closed-loop circuits are investigated by time domain analysis.

Keywords: Switch mode power supply, IRU3037 IC, Synchronous PWM control, Loop gain analysis, Type II compensator

***Corresponding author:** Zonguldak Bülent Ecevit University, Faculty of Engineering, Department of Electrical Electronics Engineering, 67100, Zonguldak, Türkiye
E mail: aytacaltan@beun.edu.tr (A. ALTAN)
Cağfer YANARATEŞ https://orcid.org/0000-0003-0661-0654
Aytaç ALTAN https://orcid.org/0000-0001-7923-4528

Received: August 14, 2024
Accepted: September 08, 2024
Published: September 15, 2024

Cite as: Yanarateş C, Altan A. 2024. DC regulation and loop gain analysis of a DC-DC switch mode power supply: A case study on a synchronous PWM controlled buck converter. BSJ Eng Sci, 7(5): 1014-1021.

1. Introduction

Nowadays, effective electrical energy conversion is greatly facilitated by power electronic devices (Alavi et al., 2020; Samosir et al., 2023; Sangeetha et al., 2023). One of the most common circuit topologies for power processing is the second order pulse width modulation (PWM) DC-DC buck converter, which uses an inductor and a capacitor (Naik and Mehta, 2017). Its simple topology and strong frequency domain control characteristics, in particular the absence of non-minimum phase (right half-plane zero) is one of its main advantages, and this advantageous characteristic allows a wide bandwidth of the control loop, resulting in a fast transient response to changes in load and input voltage (Simmons and Tymerski, 2021; Boukerdja et al., 2020).

DC electrical power is converted by a DC-DC switch mode power supply (SMPS) to be used by other devices by changing the supply voltage. When designed to operate at high frequencies, an SMPS can achieve unity efficiency and become smaller in size. Both step-up and step-down conversion can be achieved by placing the switch, diode and inductor in different configurations. Regulation of the output voltage is required to use a feedback system. However, feedback raises the issue of stability (Zhou et al., 2024). In order for the converter to be stable, the compensation must be implemented correctly, otherwise the converter would be slow to respond (Yasuda and Itoh, 2024). In this respect, knowledge of the loop gain is crucial for designing an effective compensation scheme (Lu et al., 2023; Hsieh and Lee, 2022; Beghou et al., 2021).

The loop gain is the sum of the gains around a feedback loop, either as a ratio or in decibels in electronics and control systems theory (Ravi and Ghosh, 2022). To control an SMPS, feedback loops are frequently employed in electronics such as amplifiers and oscillators, and more generally in both electronic and non-electronic control systems (Simmons and Tymerski, 2021). In a feedback loop, an output of the equipment is sampled and used to change the input, thereby improving the control of the output. The behaviour of the device is determined by the loop gain and the associated idea of loop phase shift, specifically whether the output is stable or unstable, which can cause oscillation (Chadha and Kazimierczuk, 2020).

An SMPS is classified as a PWM converter if its switching frequency f_sw is fixed, and the conversion ratio depends on duty ratios (Xie and Guo, 2019). A converter is considered pulse frequency modulated (PFM) if f_sw varies based on load or other factors to maintain the prearranged conversion ratio (Singh et al., 2020). SMPSs have two major advantages: they are relatively easy to analyze and simulate, and the switching harmonics are well known, so that switching noise can be dealt with systematically (Jing et al., 2022). The output of the SMPS is controlled and stabilized by negative feedback (Kapat

This work is licensed (CC BY-NC 4.0) under Creative Commons Attribution 4.0 International License

and Krein, 2020). However, the tendency to oscillate, known as converter instability, is a potential problem with the use of feedback and must be dealt with by compensation (Kobaku et al., 2020). The error in the system can be suppressed by having a large DC loop gain (Michal, 2016). However, large gain systems are more prone to instability. Therefore, a thorough loop gain analysis is required and the design of an efficient controller is crucial (Su and Li, 2020; Leoncini et al., 2022). By adjusting the values of the passive components, the transfer function of the compensator can be shaped in the loop gain analysis. Additionally, zeros, poles, and any DC gain can be achieved. Unlike linear systems, switching converters are time-varying non-linear systems whose loop gain is difficult to derive (Lu et al., 2023; Polivka et al., 1980; Lin et al., 2021). It is therefore necessary to obtain a time-invariant linear model. The dynamic (AC small signal) state space methodology, which is the most practical and widely used approach, is applied in this study (Suman et al., 2012; Herbst, 2019).

In this study, the effects of input and output disturbances on the DC regulation performance of a synchronous buck converter are investigated in detail. In addition, the commercially available IRU3037 8-pin synchronous PWM controlled buck converter is used as a case study. Parameters based on datasheet values are used to derive the transfer function. Using this transfer function, a PI controller is designed and comparative analysis is carried out by performing open-loop and closed-loop analyses.

The rest of the paper is structured as follows. The DC regulation principles of SMPS are discussed in Section 2, with particular emphasis on the methods used to achieve stable and efficient operation. Section 3 presents a detailed case study of the IRU3037 IC synchronous PWM controlled buck converter, highlighting its design and operating characteristics. The design process of the Type II (PI controller) compensator, including the rationale behind the selection of the parameters, is analyzed in detail in this section. Furthermore, this section presents the derivation of the system transfer function and gives an insight into the mathematical modelling and analysis techniques used in this study. Section 4 includes the simulation results and discussions, where the performance of the proposed design is evaluated and compared with existing methods. Finally, Section 5 concludes the paper with a summary of the main findings and suggestions for future work in this area.

2. DC Regulation of SMPSs

The closed-loop network of a DC-DC power supply consists of a power stage, a modulator for generating the pulses for the power stage with an output voltage V_{out}, a filter capacitor C_f, a divider leading to a compensator in which the reference voltage V_{ref} and the feedback voltage V_f are compared and the duty cycle D is produced accordingly (Rahimi and Emadi, 2008). The schematic diagram of a DC regulator is shown in Figure 1.

The issue addressed in this study is that how the output of the system is affected by a step change (disturbance) in either the input voltage V_{in} or the load (output current) I_{out}. In many real applications, both are unavoidable. In the presence of the disturbances mentioned above, V_{out} will react in a similar way, but the issue is whether there will be a permanent shift away from the desired output or a return to the reference tracking value (Bryant and Kazimierczuk, 2006). The generic representation of the change in output is given in Figure 2.

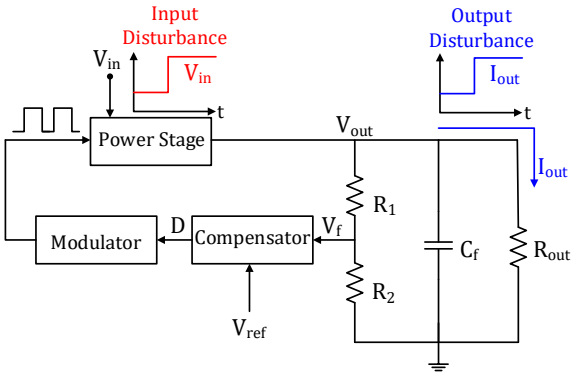

Figure 1. Schematic diagram of the closed loop network for a DC-DC power supply regulator.

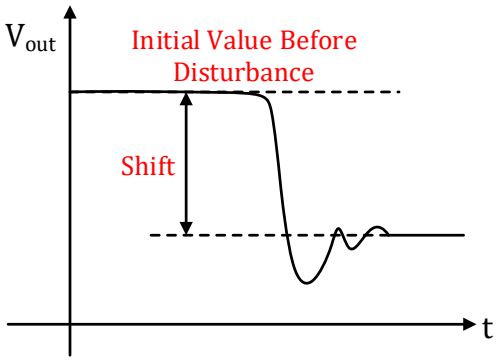

Figure 2. Generic representation of output response to step changes in input voltage or load current.

DC regulation analysis is used to observe the system to assess its behaviour and determine the amount of variation to be compensated. To understand the importance of DC regulation analysis, it can be said that the output of an electrical/electronic circuit consisting of many sub-systems is critical to the stability of the overall system as it is used as a reference in the other sub-systems. Apart from the dependence on a reasonably constant output, a robust system design captures not only the nominal or normal behaviour of the system, but also the degree of uncertainty and fluctuation (Linares-Flores et al., 2013). The voltage regulator with a feedback loop is given in Figure 3.

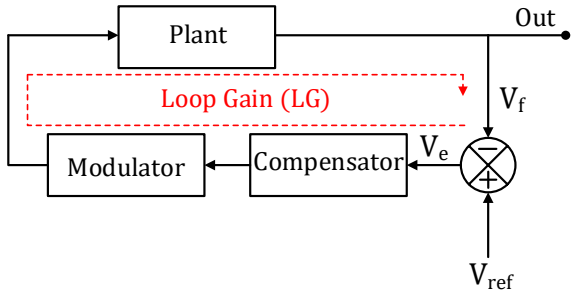

Figure 3. Voltage regulator with feedback loop for DC control analysis.

In addition to the main parts, it is shown with V_{ref}, a summation junction to compare the reference to the output, or a scaled output V_f through a divider which determined by the application and its limitations to calculate the error V_e.

The loop gain is a very important parameter that provides information for designing a reliable and robust compensator to ensure that the system will be stable at a desired bandwidth. The relationship between loop gain, V_{ref}, V_f and V_e is given by

$$Loop\ Gain = \frac{V_f}{V_e} \quad (1)$$

$$Error = V_e = V_{ref} - V_f \quad (2)$$

$$Error = V_{ref} - V_e * Loop\ Gain \quad (3)$$

The value of the loop gain in DC or extremely low frequencies is of interest, which typically have large values, certainly greater than 1. In this regard, V_e and $Loop\ Gain$ in DC are given by

$$V_e(DC) = \frac{V_{ref}}{1 + Loop\ Gain(DC)}\ ; Loop\ Gain(DC) \gg 1 \quad (4)$$

The block diagram including the effects of input and output disturbances, which can be modelled as additional inputs passing through transfer functions, is given in Figure 4. To derive the transfer functions $G_{input}(s)$ and $G_{output}(s)$, the implementations are carried out on a synchronous DC-DC buck converter topology by opening the loop (no feedback) for both cases: a step change in V_{in} and a step change in I_{out}. The generic circuit diagram of a synchronous DC-DC buck converter is shown in Figure 5.

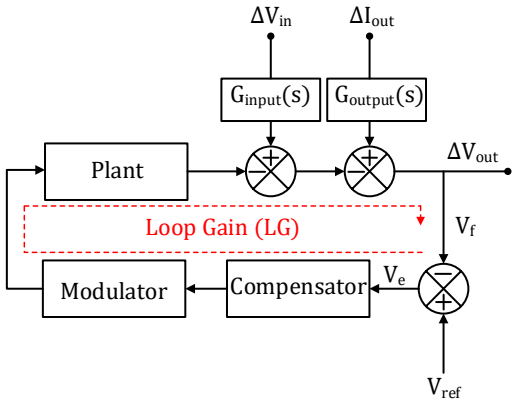

Figure 4. Block diagram showing the effects of input and output disturbances in a DC-DC buck converter.

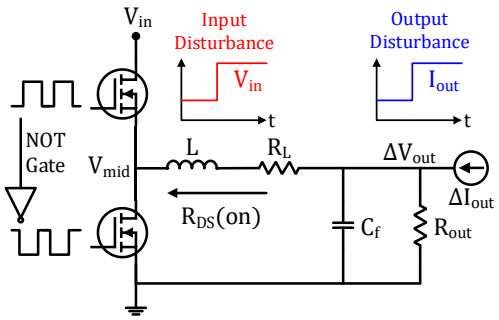

Figure 5. Generic circuit diagram of a synchronous DC-DC buck converter.

For a given operating point with a certain duty cycle, the change in V_{in} will modify V_{mid} and consequently be transmitted to V_{out}. Considering that the internal resistance of the inductor R_L is very small, close to 1, the value of V_{mid} is approximated as:

$$V_{mid} = V_{in}D \cong V_{out} \quad \Rightarrow \Delta V_{out} \cong \Delta V_{in}D \quad (5)$$

It is obvious that the transfer function $G_{input}(s)$ is the duty cycle D. Since the DC regulation of the converter is considered, the capacitor is open. The system includes R_L and the resistances of the $R_{DS}(on)$ transistors in parallel with R_{out}, which is much higher in real applications. In this respect, the relationship between ΔI_{out} and ΔV_{out}, and therefore the transfer function $G_{output}(s)$, is written as

$$\Delta V_{out} = \Delta I_{out}(R_L + R_{DS}(on)) \,//\, R_{out}) \quad (6)$$

$$\Delta V_{out} \cong \Delta I_{out}(R_L + R_{DS}(on)) \quad (7)$$

$$G_{output}(s) = R_L + R_{DS}(on) \quad (8)$$

3. A Case Study: IRU3037 IC Synchronous PWM Controlled Buck Converter

The IRU3037 8-pin synchronous PWM controlled buck converter is used as a case study, the schematic of which is shown in Figure 6. A key feature of the IRU3037 controller IC is its ability to provide cost-effective regulation for on-board DC-DC applications, including DDR memory source sink V_{TT} applications, graphics cards and hard disk drives. IRU3037 IC system parameters are listed in Table 1.

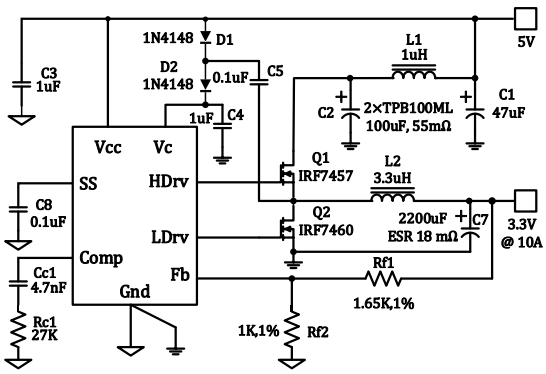

Figure 6. Schematic of the IRU3037 8-pin synchronous PWM controlled buck converter for on-board DC-DC applications.

Table 1. IRU3037 IC system parameters

IRU3037 IC System Parameters	
Input voltage	5 V
Output voltage	3.3 V
Output current	10 A
Switching frequency	200 kHz
Output inductor	3.3 µH
Output capacitor	2200 µF with 18 mΩ ESR
Peak to peak oscillator ramp voltage	V_{OSC} =1.25 V
Reference voltage	V_{REF} =1.25 V
Transconductance gain	G_m =0.6 mA/V or 600 µmho

The zero-crossover frequency, or F_o, is the frequency at which the loop gain is unity. Its value is often between 1/10 and 1/5 of the switching frequency. F_o determines the speed at which the dynamic load response occurs. The higher the F_o, the faster the dynamic response. To obtain a stable system, the slope of the loop gain around F_o should be $-20\ dB$. A stable system often has a phase margin of 45° or more.

The output inductor and the output capacitor are the cause of the pole, so the power stage pole F_{PO} is determined as

$$F_{PO} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \quad (9)$$

$$F_{PO} = \frac{1}{2\pi \times \sqrt{3.3\mu H \times 2200\mu F}} \cong 1.87\ kHz \quad (10)$$

The ESR of the output capacitor is the cause of the zero point F_{ZO}, and it is calculated as

$$F_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (11)$$

$$F_{ZO} = \frac{1}{2\pi \times 18m\Omega \times 2200\mu F} \cong 4\ kHz \quad (12)$$

The desired zero crossover frequency F_O is selected as 20 kHz according to the design criteria correlation between F_O and the switching frequency f_{sw} ($F_O \leq f_{sw}/5 \sim f_{sw}/10$). The standard process for designing compensators in practical circuits involves the use of an error amplifier in conjunction with a network; Type II and Type III compensators are the most commonly used, as Type I compensators exhibit poor performance. As shown in Table 2, the characteristics of the output capacitor and the location of the zero-crossover frequency determine the type of compensation. The Type II compensator, also known as a proportional-integral (PI) controller, is used in this case study because the integration of the derivative action into it causes high noise in the system control.

Table 2. Compensator type selection criteria based on output capacitor characteristics and zero crossover frequency

Compensator Type	Location of Zero Crossing Frequency	Typical Output Capacitor
Type II (PI)	$F_{PO} < F_{ZO} < F_O < f_{sw}/2$	Electrolytic, Tantalum
Type III (PID)	$F_{PO} < F_O < F_{ZO} < f_{sw}/2$	Tantalum, Ceramic

3.1. Type II Compensator Design Process

The configuration of the PI compensator, the desired loop gain and the bode plot of the buck converter power stage are shown in Figure 7.

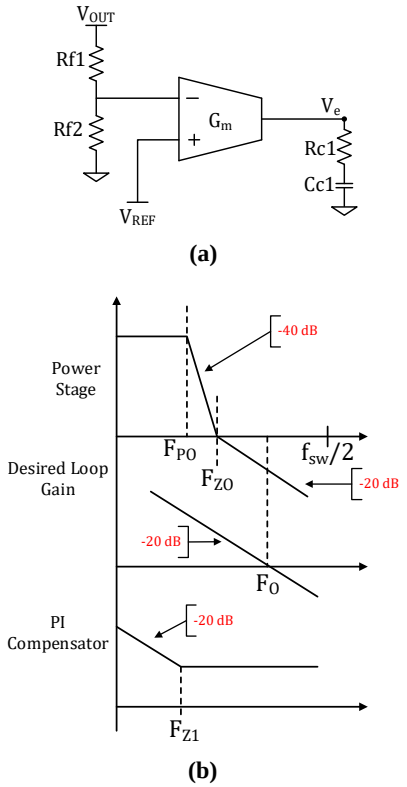

Figure 7. Configuration of **a)** the PI compensator with **b)** the desired loop gain and bode plot of the buck converter power stage.

A zero is present in a PI compensator at

$$F_{Z1} = \frac{1}{2\pi \times Rc1 \times Cc1} \quad (13)$$

The output voltage is calculated using resistors $Rf1$ and $Rf2$. This gives the output voltage and is expressed as

$$\frac{V_{OUT}}{V_{REF}} = \frac{Rf2}{Rf1 + Rf2} \quad (14)$$

The feedback pin of the error amplifier can be connected directly to the output voltage. This appears as

$$V_{OUT} = V_{REF} \quad (15)$$

The zero-crossover frequency is set by the resistor $Rc1$. It is calculated as

$$Rc1 = \frac{2\pi \times F_O \times L \times V_{OSC}}{ESR \times V_{IN} \times G_m} \times \frac{Rf1 + Rf2}{Rf2} \quad (16)$$

Combining Equation (14) with Equation (16), $Rc1$ is expressed as

$$Rc1 = \frac{2\pi \times F_O \times L \times V_{OSC}}{ESR \times V_{IN} \times G_m} \times \frac{V_{OUT}}{V_{REF}} \quad (17)$$

Assigning 75% of F_{PO} as the PI compensator zero:

$$F_{Z1} = \frac{1}{2\pi \times Rc1 \times Cc1} = 0.75 \times F_{PO} \quad (18)$$

Calculating the compensator capacitor $Cc1$ is as:

$$Cc1 = \frac{1}{0.75 \times 2\pi \times F_{PO} \times Rc1} = \frac{\sqrt{L \times C_{OUT}}}{0.75 \times Rc1} \quad (19)$$

The explanation above states that the desired locations for the zeros and poles of the chosen PI compensator are

$$F_{Z1} = 0.75 \times F_{PO} = 0.75 \times 1.87\ kHz \quad (20)$$

$$F_{Z1} \cong 1.4\ kHz \quad (21)$$

For the chosen PI compensator, based on the actual parameters, the resistor and capacitor are computed as

$$Rc1 = \frac{2\pi \times 20KHz \times 3.3\mu H \times 1.25}{18\ m\Omega \times 5\ V \times 0.6 \times 10^{-3}} \times \frac{3.3}{1.25} \quad (22)$$

$$Rc1 \cong 25.3\ k\Omega \quad \Rightarrow selected\ as\ 27\ k\Omega \quad (23)$$

$$Cc1 = \frac{\sqrt{3.3\ \mu H \times 2200\ \mu F}}{0.25 \times 27\ k\Omega} \cong 4.2\ nF \quad (24)$$

$$Cc1\ selected\ as\ 4.7\ nF \quad (25)$$

3.2. System Transfer Function Derivation

The transfer function model of the desired buck converter is obtained using the dynamic (AC small signal) state space methodology. Since the inductor and capacitor are the main energy storage components of the buck converter, the system state variables are inductor current $i_L$and capacitor voltage V_C. Accordingly, the system vector x is defined as

$$x = \begin{bmatrix} i_L \\ V_C \end{bmatrix} \quad (26)$$

The state variable vector x at the steady state operating point is rewritten using

$$X = -A^{-1}BV_{in} \quad (27)$$

$$X = -\frac{adj\begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C_{OUT}} & \frac{-1}{R_{Load}C_{OUT}} \end{bmatrix}}{det\begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C_{OUT}} & \frac{-1}{R_{Load}C_{OUT}} \end{bmatrix}} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} V_{in} \quad (28)$$

$$X = \begin{bmatrix} \frac{{C_{OUT}}^2 DV_{in}}{R_{Load}} \\ DV_{in} \end{bmatrix} \quad (29)$$

Here A, B are the system and input matrices, respectively. The load R_{Load} is chosen to be purely resistive with a value of 0.33 Ω. Applying the steady state vector, the average system, and input matrices, $\frac{\hat{x}(s)}{\hat{D}(s)}$ is obtained as

$$\frac{\hat{x}(s)}{\hat{D}(s)} = \frac{\begin{bmatrix} \hat{i}_L \\ \hat{V}_C \end{bmatrix}}{\hat{D}(s)} = \begin{bmatrix} \frac{V_{in}(C_{OUT}R_{Load}s + 1)}{C_{OUT}LR_{Load}s^2 + Ls + R_{Load}} \\ \frac{V_{in}R_{Load}}{C_{OUT}LR_{Load}s^2 + Ls + R_{Load}} \end{bmatrix} \quad (30)$$

The transfer functions connecting D to i_L and V_{OUT} can be obtained by substituting the values of the IRU3037 IC components into Equations (31) and (33).

$$\frac{i_L(s)}{D(s)} = \frac{V_{in}}{L} \frac{s + \frac{1}{R_{Load}C_{OUT}}}{s^2 + \frac{s}{R_{Load}C_{OUT}} + \frac{1}{LC_{OUT}}} \quad (31)$$

$$\frac{i_L(s)}{D(s)} = \frac{0.011s + 15.15}{7.26 \times 10^{-9}s^2 + 10^{-5}s + 1} \quad (32)$$

$$\frac{V_{OUT}(s)}{D(s)} = \frac{V_{in}}{C_{OUT}L} \frac{1}{s^2 + \frac{s}{R_{Load}C_{OUT}} + \frac{1}{LC_{out}}} \quad (33)$$

$$\frac{V_{OUT}(s)}{D(s)} = \frac{0.0075}{7.26 \times 10^{-9}s^2 + 10^{-5}s + 1} \quad (34)$$

4. Results and Discussions

Understanding the transient and steady state responses of systems requires an understanding of time domain analysis. It is essential to understand how a system operates in the initial stages of a disturbance and how it transitions to a stable state. The step response of the voltage transfer function $V_{OUT}(s)/D(s)$ is shown in Figure 8. Table 3 shows the step response characteristics of the open loop voltage transfer function of the IRU3037 IC.

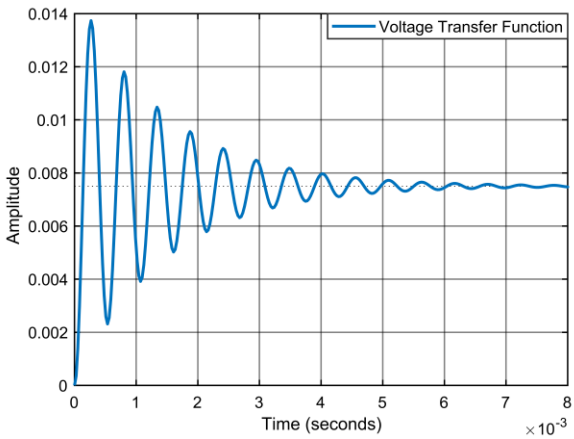

Figure 8. Step response of the voltage transfer function.

Table 3. Step response characteristics of the open-loop voltage transfer function for the IRU3037

Step Response Characteristics	IRU3037 IC Open Loop Voltage Transfer Function
Rise time (s)	9.2929e-05
Settling time (s)	0.0057
Settling minimum	0.0023
Settling maximum	0.0137
Overshoot (%)	83.1365
Undershoot (%)	0
Peak	0.0137
Peak time (s)	2.6768e-04

The step response of the current transfer function $i_L(s)/D(s)$ is given in Figure 9. Table 4 shows the step response characteristics of the open loop current transfer function of the IRU3037.

The step response of the closed loop voltage transfer function $V_{OUT}(s)/D(s)$ is given in Figure 10. Table 5 shows the step response characteristics of the closed loop voltage transfer function of the IRU3037 IC.

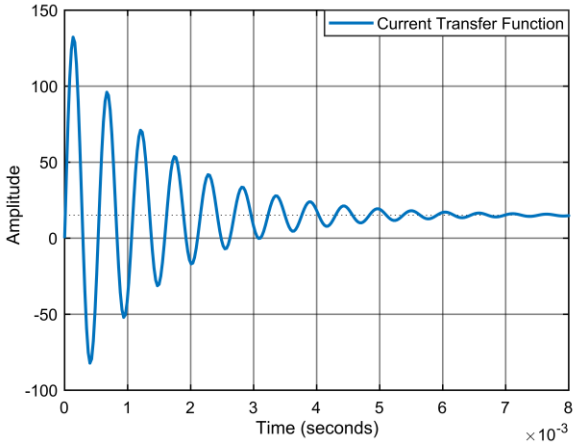

Figure 9. Step response of the current transfer function.

Table 4. Step response characteristics of the open loop current transfer function for the IRU3037

Step Response Characteristics	IRU3037 IC Open-Loop Current Transfer Function
Rise time (s)	8.1319e-06
Settling time (s)	0.0058
Settling minimum	-82.1559
Settling maximum	132.2361
Overshoot (%)	772.7586
Undershoot (%)	542.2288
Peak	132.2361
Peak time (s)	1.3384e-04

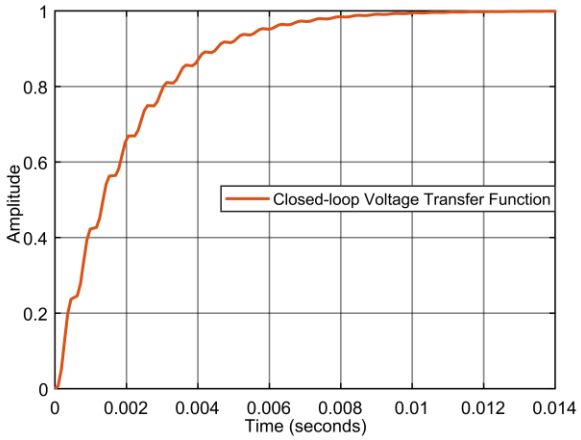

Figure 10. Step response of the closed loop voltage transfer function.

Table 5. Step response characteristics of the closed loop voltage transfer function for the IRU3037

Step Response Characteristics	IRU3037 IC Closed Loop Voltage Transfer Function
Rise time (s)	0.0043
Settling time (s)	0.0077
Settling minimum	0.9040
Settling maximum	0.9996
Overshoot (%)	0
Undershoot (%)	0
Peak	0.9996
Peak time (s)	0.0149

The step response of the closed loop current transfer function $i_L(s)/D(s)$ is given in Figure 11. Table 6 provides the step response characteristics of the closed loop current transfer function of the IRU3037 IC.

Table 7 shows the DC loop gain of the system as the product of the derived output voltage transfer function along the closed loop for various input and output disturbances, denoted as D_{in} and D_{out} respectively. The gain without any disturbance is obtained from the simulation result as 3.6.

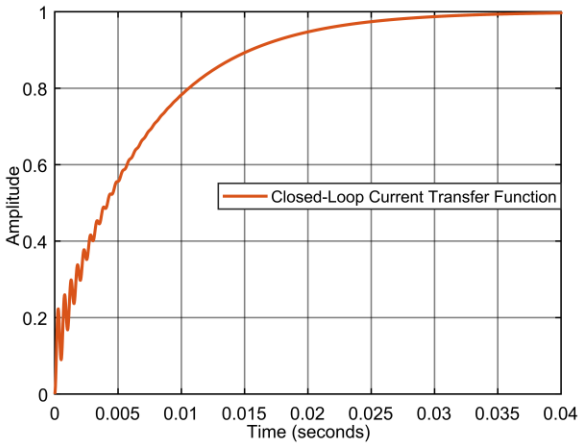

Figure 11. Step response of the closed loop current transfer function.

Table 6. Step response characteristics of the closed loop current transfer function for the IRU3037

Step Response Characteristics	IRU3037 IC Closed Loop Current Transfer Function
Rise time (s)	0.0153
Settling time (s)	0.0268
Settling minimum	0.9000
Settling maximum	0.9986
Overshoot (%)	0
Undershoot (%)	0
Peak	0.9986
Peak time (s)	0.0454

Table 7. DC loop gain for various input and output disturbances

Voltage Transfer Function DC Loop Gain				
Input Disturbance		Output Disturbance		Input & Output Disturbance
D_{in}	Loop Gain	D_{out}	Loop Gain	Loop Gain
0.1	3.465	1.0	2.530	2.450
0.2	3.337	1.5	2.162	2.036
0.3	3.217	2.0	1.864	1.711
0.4	3.103	2.5	1.617	1.448
0.5	2.995	3.0	1.410	1.232
0.6	2.892	3.5	1.232	1.051
0.7	2.795	4.0	1.079	0.898
0.8	2.702	4.5	0.946	0.765
0.9	2.614	5.0	0.829	0.650
1.0	2.530	5.5	0.725	0.549

5. Conclusion

Feedback loops are widely used in electronics and control theory, whether they are electronic or not, to regulate equipment and devices. Oscillators and amplifiers are two examples of such applications. A feedback loop modifies the input and amplifies the output control by using a sample of the output of a device, process or plant. The loop gain and the associated idea of loop phase shift control the behaviour of the device, in particular whether the output is stable and not prone to oscillation. In this context, the DC regulation of a buck converter, which is a DC-DC SMPS operating on a PWM signal, is carried out in this study. Particular attention has been paid to the internal resistance of the coil and the on-resistance of the controllable circuit element (switching device), which are essential in the system. It has been investigated how these parameters create disturbances in the input and output load of the system and how they affect the loop gain. The transfer function of the IRU3037 IC, which was used as a case study, was obtained using datasheet-based information and state-space averaging and AC small-signal methods. In addition to the loop gain analysis, a time domain analysis was carried out and the corresponding step response characteristics were analyzed for both open and closed loop circuits. Future work is concerned with developing different control techniques to obtain more reliable and robust results to minimize the effect of essential and undesirable parameters in switch mode power supply applications.

Author Contributions

The percentages of the authors contributions are presented below. The authors reviewed and approved the final version of the manuscript.

	C.Y.	A.A.
C	50	50
D	50	50
S	50	50
DCP	50	50
DAI	50	50
L	50	50
W	50	50
CR	50	50
SR	50	50

C=Concept, D= design, S= supervision, DCP= data collection and/or processing, DAI= data analysis and/or interpretation, L= literature search, W= writing, CR= critical review, SR= submission and revision.

Conflict of Interest

The authors declared that there is no conflict of interest.

Ethical Consideration

Ethics committee approval was not required for this study because of there was no study on animals or humans.

References

Alavi P, Babaei E, Mohseni P, Marzang V. 2020. Study and analysis of a DC–DC soft-switched buck converter. IET Power Electron, 13(7): 1456-1465.

Beghou L, Popat M, MacDonald S. 2021. PWM control of 3-phase PFC vienna rectifier derived from an average current-based control of single-phase PFC boost converter. In 2021 IEEE IEEE Energy Convers. Congr. Expo. (ECCE), October 10-14, Vancouver, Canada, pp: 3452-3459.

Boukerdja M, Chouder A, Hassaine L, Bouamama BO, Issa W, Louassaa K. 2020. H∞ based control of a DC/DC buck converter feeding a constant power load in uncertain DC microgrid system. ISAT, 105: 278-295.

Bryant B, Kazimierczuk MK. 2006. Voltage loop of boost PWM DC-DC converters with peak current-mode control. IEEE Trans Circuits Syst I, Reg Papers, 53(1): 99-105.

Chadha A, Kazimierczuk MK. 2020. Small-signal modeling of open-loop PWM tapped-inductor buck DC–DC converter in CCM. IEEE Trans Ind Electron, 68(7): 5765-5775.

Herbst G. 2019. A building-block approach to state-space modeling of DC-DC converter systems. J Multidiscip Sci J, 2(3): 247–267.

Hsieh YH, Lee FC. 2022. Improved three-terminal model for PWM converters with current-mode control. In 2022 IEEE IEEE Energy Convers. Congr. Expo. (ECCE), October 9-13, Detroit, USA, pp: 1-8.

Jing T, Maklakov A, Radionov A, Gasiyarov V, Liang Y. 2022. Formulations, solving algorithms, existing problems and

future challenges of pre-programmed PWM techniques for high-power AFE converters: A comprehensive review. Energies, 15(5): 1696.

Kapat S, Krein PT. 2020. A tutorial and review discussion of modulation, control and tuning of high-performance DC-DC converters based on small-signal and large-signal approaches. IEEE Open J Power Electron, 1: 339-371.

Kobaku T, Jeyasenthil R, Sahoo S, Ramchand R, Dragicevic T. 2020. Quantitative feedback design-based robust PID control of voltage mode-controlled DC-DC boost converter. IEEE Trans. Circuits Syst. II: Express Briefs, 68(1): 286-290.

Leoncini M, Melillo P, Bertolini A, Levantino S, Ghioni M. 2022. Integrated loop-gain measurement circuit for DC/DC boost converters with time-based control. In 2022 IEEE 17th Conf. Ph. D Res. Microelectron. Electron. (PRIME), June 12-15, Villasimius, Italy, pp: 253-256.

Lin J, Su M, Sun Y, Li X, Xie S, Zhang G, Blaabjerg F, Feng, J. 2021. Accurate loop gain modeling of digitally controlled buck converters. IEEE Trans Ind Electron, 69(1): 725-739.

Linares-Flores J, Méndez AH, García-Rodríguez C, Sira-Ramírez H. 2013. Robust nonlinear adaptive control of a "boost" converter via algebraic parameter identification. IEEE Trans Ind Electron, 61(8): 4105-4114.

Lu D, Zeng X, Hong Z. 2023. Accurate loop gain model of ripple-based constant on-time controlled buck converters. IEEE Trans Power Electron, 38(6): 7034-7048.

Michal V. 2016. Dynamic duty-cycle limitation of the boost DC/DC converter allowing maximal output power operations. In 2016 IEEE Int. Conf. Appl. Electron, September 6-7, Pilsen, Czech Republic, pp: 177-182.

Naik BB, Mehta AJ. 2017. Sliding mode controller with modified sliding function for DC-DC Buck Converter. ISA T, 70: 279-287.

Polivka WM, Chetty PRK, Middlebrook RD. 1980. State-space average modelling of converters with parasitics and storage-time modulation. In 1980 IEEE Power Electron Spec Conf, June 16-20, Atlanta, USA, pp: 119-143.

Rahimi AM, Emadi A. 2008. An analytical investigation of DC/DC power electronic converters with constant power loads in vehicular power systems. IEEE Trans Veh Technol, 58(6): 2689-2702.

Ravi D, Ghosh A. 2022. Voltage mode control of buck converter using practical PID controller. In 2022 IEEE Int. Conf. Intell. Control. Comput. Smart Power (ICICCSP), July 21-23, Hyderabad, India, pp: 1-6.

Samosir AS, Sutikno T, Mardiyah L. 2023. Simple formula for designing the PID controller of a DC-DC buck converter. Int J Power Electron Drive Syst, 14(1): 327-336.

Sangeetha S, Revathi BS, Balamurugan K, Suresh G. 2023. Performance analysis of buck converter with fractional PID controller using hybrid technique. Robotics Auton Syst, 169: 104515.

Simmons J, Tymerski R. 2021. Design and control of an alternative buck PWM DC-to-DC converter. J Power Energy Eng, 9(6): 43-61.

Singh R, Bose S, Dwivedi P. 2020. Closed loop control of flyback converter with PV as a source. In 2020 IEEE 9th Power India Int. Conf. (PIICON), February 28-March 01, Sonepat, India, pp: 1-6.

Su I, Li D. 2020. Understanding and simulation of loop stability test for DC/DC converters. URL: www.ti.com (accessed date: 28 July 2024).

Suman G, Kumar BP, Kumar MS, Babu BC, Subhashini KR. 2012. Modeling, analysis and design of synchronous buck converter using state space averaging technique for PV energy system. In 2012 IEEE Int Symp on Electronic System Design (ISED), December 19-22, Kolkata, India, pp: 281-285.

Xie H, Guo E. 2019. How the switching frequency affects the performance of a buck converter. Texas Instruments Incorporated: Dallas, TX, USA, pp: 53.

Yasuda T, Itoh JI. 2024. A power balancing control for large power unbalance in a modular multilevel multiport converter with phase-disposition PWM. IEEJ J Industry Appl, 13(1): 41-51.

Zhou S, Zhou G, He M, Mao S, Zhao H, Liu G. 2024. Stability effect of different modulation parameters in voltage-mode PWM control for CCM switching DC-DC converter. IEEE Trans Transport Electr, 10(2): 2408-2422.