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The Electrical Characterization Effect of Insulator Layer between Semiconductor and Metal

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ABSTRACT: Metal-Insulator-semiconductor contacts (MIS) have been studied its importance in electronic and optoelectronic. Their importance comes from its so high dielectric constant, storage layer property and effect of capacitance. For this reason, Si_3N_4 were deposited with PECVD technique on p-type Si about 5 nm thickness layers. The thicknesses of Si_3N_4 were measured with an elipsometre and obtained MIS contact with Al contact. It was researched the insulator layer effect on the Al/p-Si contact. Its electrical characterizations were inquired by use of the forward and reverse bias *I-V*, *C–V* and *G-V* measurements and were seen that the insulator Si_3N_4 layer influenced characterizations of the contact. Effect of the interface states (N_{ss}), the series resistance (R_s) and the other some electrical parameters were investigated by calculating from *I-V* and *C–V* measurements. It was observed that from the *C-V* characterizations at 500 kHz dual, contact behaved similarly memristor structure.

Keywords: Al/Si_3N_4/p-Si, capacitance behavior, metal-insulator-semiconductor structure, Schottky diode

IĞDIR ÜNİVERSİTESİ FBED JIST

Metal ve Yarıiletken Arasındaki Yalıtkan Tabakanın Elektriksel karakterizasyon Etkisi

ÖZET: Metal-yalıtkan-yarıiletken (MIS) aygıtlar elektronik ve optoelektronikteki önemlerinden dolayı çalışılmaktadır. Bu önem aygıtların yüksek dielektrik sabitine, depolama tabakası ve kapasitans özelliklerine sahip olmalarından kaynaklanmaktadır. Bu yüzden Si_3N_4 tabakası p-tipi Si üzerine PECVD tekniği kullanılarak büyütülmüş, kalınlığı elipsometre ile 5 nm olarak ölçülmüştür ve Al kontak sayesinde MIS yapısı elde edilmiştir. Elde edilen Al/p-Si yapısı üzerine Si_3N_4 tabakasının etkisi araştırılmıştır. Bunun için aygıtın elektrik karakterizasyonları ileri ve ters beslem *I-V*, *C–V* ve *G-V* ölçümleriyle yapılmış ve yalıtkan Si_3N_4 tabakanın diyot özelliklerini oldukça etkilediği görülmüştür. Ara yüzey halleri (N_{ss}), seri direnç (R_s) ve diğer bazı elektriksel parametrelerin aygıt üzerine etkileri *I-V* ve *C–V* ölçümlerinden hesaplanarak araştırılmıştır. *C-V* ölçümlerinden aygıtın memristör bir yapı gibi davrandığı tespit edilmiştir.

Anahtar Kelimeler: Al/Si_3N_4/p-Si, kapasitör özelliği, metal-yalıtkan-yarıiletken yapılar, Schottky diyot

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INTRODUCTION

Metal-semiconductor contacts (Schottky diodes) are fundamental and mostly employed in technology e.g. rectifiers, inverters, freewheeling and polarity protection diodes (Sharma et al., 2004; Rajesh and Menon 2007; Güllü and Türüt, 2010; Karataş et al., 2013). From past to present, there has been increasing attention of these contacts because they have used in optic and electronic (Markyart, 2000; Sze and Kwok, 2007; Tatar et al., 2009; Orak et al., 2014). Current conduction mechanism and barrier height forming in these contacts are depend on several parameters such as interfacial layer, series resistances, doping acceptor/donor concentration of atoms, interface states density, the thickness and homogeneity of barrier height and interfacial layer, sample temperature and applied bias voltage. But the performance and quality of these contacts can be changed or improved by using interfacial insulator layers (Bilkan et al., 2015). If an insulator sheet for instance TiO_2, $SrTiO_3$, SiO_2, SnO_2 and Si_3N_4 is inserted between semiconductor and metal, the metal semiconductor structures change a metal–oxide–semiconductor (MOS) structure (Türüt et al., 2015) (≥ 100 Å) or metal–insulator–semiconductor (MIS) (Zeyrek et al., 2006) (≤ 100 Å) based on the thickness of insulator. Presence of some insulator layer induces deviation from the ideal property which could be detected the *C–V* and *G/w–V* measurements of metal semiconductor contacts (Gökçen et al., 2012). The important characteristic of insulator layer at the MIS structure has a dielectric property which is resemble a capacitor. If insulator layer between semiconductor and metal is very thin (˜30 Å), electrical parameters of this structure could be specified by *I-V* and *C-V* characterizations. But the existence of more thickness insulator layer at the interface, *I-V* characteristics cannot be measured (Sönmezoğlu and Akın, 2011).

In the present study, Al/Si_3N_4/p type Si contact has been investigated according to insulator layer effect at room temperature because of understanding performance and quality of this contact.

MATERIALS AND METHODS

p-type Si wafer which was polished and cleaned used for the deposition of the Al/Si_3N_4/p type Si heterojunction has (100) orientation and 7.3 x 10^{15} cm^{-3} carrier concentration according to manufactures specifications. The wafer was degreased consecutively in acetone and isopropyl alcohol with ultrasonic mixer for 5 min. Before ohmic contact, the wafer p-type Si was cut into pieces of 1.0 cm length by 1.0 cm breadth. The degreased wafer was etched with $HF:H_2O$ (1:10) for 30 second to take out the surface damages and undesirable impurities. Aluminum was vaporized (thermal) on another side of the p-type Si for the ohmic contact and the p-Si/Al was puddled at 450 °C for 3 minute in N_2 ambience. The insulator layers have been formed PECVD technique on p-type Si nearly 5 nm thicknesses. (The ratio of Si_3N_4($SiH_4:NH_3$, (185:45 sccm)) The schematic diagram of contact could be seen in Figure 1. The Al contacts have been formed by thermal vapor method as points with diameter of around 1.0 mm on the front surface of the p-Si. The thickness of metal coating was designated with a quartz screen positioned in close intimacy to the Si. The *I–V* and *C-V* measurements of the diode were performed by use of a Keithley 2400 Picoammeter/Voltage Apparatus and HP 4192 A LF Impedance Analyzer.

Figure 1. Schematic diagram of Al/Si_3N_4/p-Si Schottky contact

RESULTS AND DISCUSSION

It has been shown the typical semi-logarithmic *I–V* characteristics of the Al/Si_3N_4/p-Si structure in Figure 2.

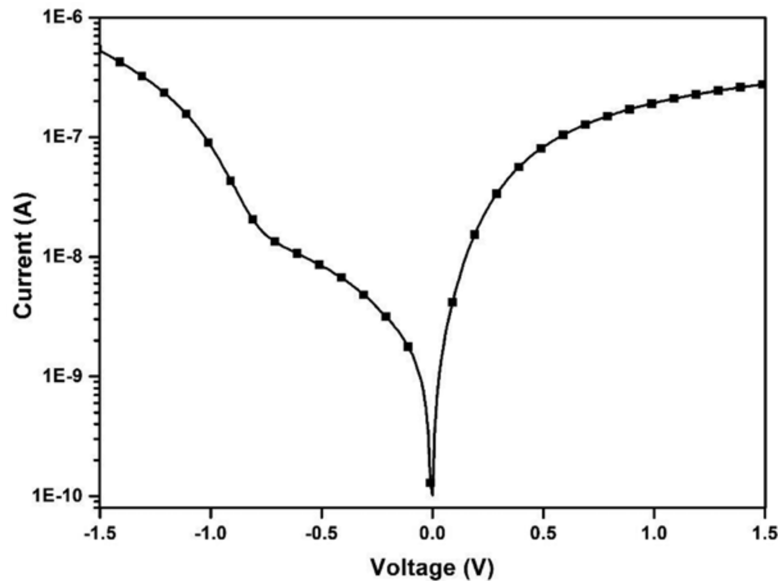

Figure 2. ln$I$-V characteristic of Al/Si_3N_4/p-Si in dark at room temperature

According to this figure, contact has a rectifying behavior under dark at room temperature. Important diode parameters i.e ideality factor and barrier height could be gotten from this graph. The ideality factor (n) could be obtained from the gradient of the linear region of the forward bias I–V plot and barrier height (Φ_b) could be found the current axis intercept of this linear. The Current is given by the equation (El-Nahass et al., 2011);

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{nkT}\right)\right] \quad (1)$$

where I_0 is the saturation current which is obtained from the intercept of ln$I$ vs V plot at $V = 0$, written as

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_b}{KT}\right) \quad (2)$$

where q is the electronic charge, V is the applied voltage, K is Boltzmann's constant, T is the temperature (=300 K), A^* is the effective Richardson constant ($A^* = 32$ A cm^{-2} K^{-2} for p-type Si), A is the area of diode (=7.85 x 10^{-3} cm^2), Φ_b is the Schottky barrier height at zero bias and n is the ideality factor. The ideality factor (for $V \geq 3kT/q$) and barrier height specified from the forward bias ln$I$–V characteristics by use of the Equations (1) and (2)

$$n = \frac{q}{kT}\left(\frac{dV}{dlnI}\right) \quad (3)$$

and

$$\Phi_b = \frac{kT}{q} ln\left(\frac{A^*AT^2}{I_0}\right) \quad (4)$$

In respect of Equations (3) and (4), the worth of the ideality factor (n) and the barrier height (Φ_b) of Al/Si_3N_4/p-Si Contact were accounted as 1.34 and 0.73 eV, respectively. These results have been given in Table 1, also. The worth of ideality factor has higher than from unity which is suggesting Schottky contact is not ideal. If n equals unity, pure thermionic emission occurs but n is usually greater than one. This high ideality factor can be ascribed to several influences i.e tunnelling process (Lee et al., 2010) and irregular scatter of the interfacial charges (Demircioğlu et al., 2011), image-force effect (Sharma and Tewari, 2011), interface states (Orak et al., 2015), barrier inhomogeneity (Roul et al., 2015) and series resistance (Korucu and Duman, 2015). High value of n verify the existence of an insulator sheet between semiconductor and metal, also (Nasim and Bhatt, 2013). In here, beside the insulator layer of Si_3N_4, a little amount of SiO_2 may be formed.

The barrier height (Φ_b) and series resistance (R_s) could be accounted also by Norde method (Güllü et

al., 2012) and the Cheung's functions (Cheung and Cheung, 1986). If the Schottky contact has series resistance, the clear amount current of the contact is because of thermionic emission and could be stated as for Cheung's functions (Karataş et al., 2013);

$$I = I_0 \exp\left(-\frac{q(V - IR_s}{nkT}\right) \quad (5)$$

where IR_s term is the voltage descent owing to series resistance. The worth of the series resistance can be calculated from the below equations:

$$\frac{dV}{d(lnI)} = IR_s + n\frac{kT}{q} \quad (6)$$

$$H(I) = V - n\left(\frac{kT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) \quad (7)$$

where *H(I)* could be written as:

$$H(I) = IR_s + n\Phi_b \quad (8)$$

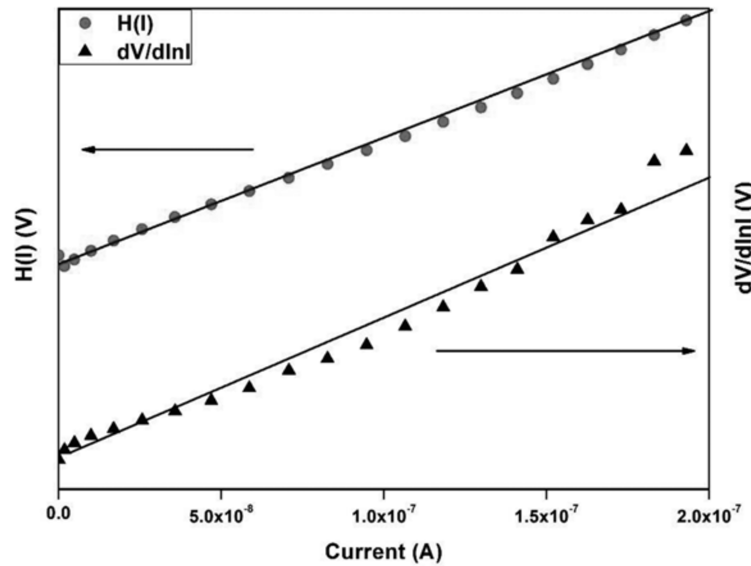

Figure 3. dv/dln*I*-*I* and *H(I)-I* graphs of Al/Si_3N_4/p-Si Schottky contact

Equations (6) and (8) give a straight for the data of decreasing curvature region of the forward bias *I–V* plot. For this reason, the plot of *dV/d(*ln*I)* vs *I* will be linear and obtain R_s as the slope and *nkT/q* as the *y*-axis intercept from Equation (6). Graph of *H(I*) vs *I* according to Equation (8) will be also linear and *y*-axis intercept will equal to $n\Phi_b$. In here, *n* worth is obtained from graphs of *dV/d(*ln*I)* vs *I* and so, Φ_b is accounted easily. The slope of *H(I*) vs *I* also gives a second designation of R_s which could be indicated to control the coherency of Cheung method. The graphs of *dV/d(*ln*I)* vs *I* and *H(I)* vs *I* have been attained the forward bias *I–V* measurement of the Al/Si_3N_4/p-Si contact and given in Figure 3. The values of *n*, Φ_b, R_s (*dV/d(*ln*I)*) and R_s (*H(I)*) have been accounted as 1.07, 0.81 eV, 4.13 KΩ and 4.55 KΩ, respectively. These obtained results have been also given in Table 1 and indicated the accuracy of Cheung's method. There is a small variation between the worth of the ideality factor acquired from the decreasing curvature region of the forward bias *I–V* plot and the linear region of the same characteristics. This variation could be ascribed to the presence of influences i.e. the bias dependency of the Schottky barrier height and the series resistance,

charge of the interface states with bias in this concave region of the *I–V* measurement and according to the voltage descent the interfacial layer (Demircioğlu et al., 2011). It is observed that the worth of *n* attained from the forward bias ln *I–V* plot is agreeing with that of the *dV/d*(ln*I*)*–I* curves (Tatar et al., 2009).

Table 1. The experimental diode parameters calculated from *I-V* measurements for Al/Si_3N_4/p-Si contact.

***n* (*I-V*)** -	***n* Cheung** -	**Φ_b (*I-V*)** (eV)	**Φ_b Cheung** (eV)	**Φ_b Norde** (eV)	**Φ_b (*C-V*)** (eV)	**R_s Cheung** (kΩ (*H*(*I*)))	**R_s Cheung** ((kΩ (*d*ln(*I*))	**R_s Norde** (kΩ)
1.34	1.07	0.73	0.81	0.81	0.69	4.55	4.13	12.1

Norde method can be used as another technique for calculating of the series resistance especially for the high series resistance. The following equation has been identified in the changed Norde method (Karataş et al., 2013):

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q} ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{9}$$

where γ is an integer (γ>*n*). Ideality factor is used from thermoionic emission theory results and *I(V)* is current acquired from the *I–V* curve. Firstly, using plot of the *F(V)* vs *V*

$$\Phi_b = F(V_0) + \left[\frac{V_0}{\gamma} - \frac{kT}{q}\right] \tag{10}$$

Φ_b can be obtained from Equation (10), where $F(V_0)$ is the minimum point of *F(V)* and V_0 is the related voltage.

$$R_s = \frac{\gamma - n}{I} \frac{kT}{q} \tag{11}$$

From the *F(V)–V* plot (shown in Figure 4) by use of $F(V_0)$ = 0.815 V and V_0 = 0.044 V values, Φ_b and R_s of the Al/Si_3N_4/p-Si contact have been calculated as 0.81 eV and 12.1 kΩ, respectively.

The results of Φ_b and R_s obtained from Norde method has been given in Table 1. The barrier height values are same and there is relative difference between series resistance values obtained from Cheung and Norde methods.

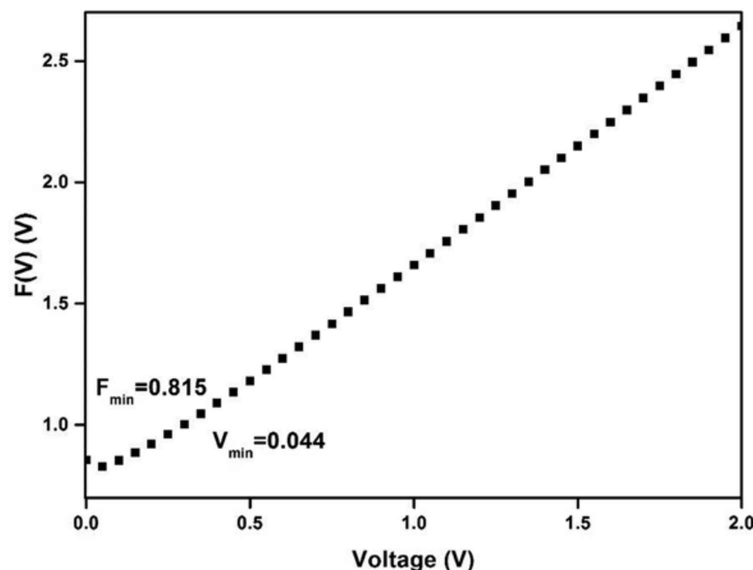

Figure 4. *F(V)* vs *V* graph of Al/Si_3N_4/p-Si contact

ln*I–V* plot which have a non-linearity part at high forward bias voltages shows a continuum of N_{ss} in balance with semiconductor. For diode, the energy density scatter condition of the N_{ss} was designated from the forward bias *I–V* by considering efficient barrier height (Φ_e), ideality factor *n(V)* which is depend on the voltage and R_s. The Φ_e can be written as following equation (Bilkan et al., 2015):

$$\Phi_e = \Phi_b + (1 - 1/n(V))(V - IR_s) \quad (12)$$

Since the ideality factor of a diode become all time greater than one, it was suggested below formula by Card and Rhoderick (Card and Rhoderick, 1971).

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_d} + qN_{ss}(V)\right] \quad (13)$$

where W_d is depletion layer width and δ is the thickness of the insulator sheet at the interface. ε_i and ε_s are permittivity of interfacial layer and the semiconductor, respectively. For diode, proposed the energy density scatter of N_{ss} can be found from the forward bias *I–V* data by using voltage dependent of effective barrier height(Φ_e) and ideality factor (*n(V)*) by which suggested by Card and Rhoderick (Card and Rhoderick, 1971):

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_d})\right] \quad (14)$$

In addition, for p-type semiconductors, the energy of the N_{ss} as regards the upper of the valance band (E_v) at the semiconductor surface can be accounted as

$$E_{ss} - E_v = q(\Phi_e - (V - IR_s)) \quad (15)$$

where the IR_s term is the voltage descent on the R_s. The energy density distribution profile of N_{ss} with (inset of Figure 5) and without R_s that is obtained from the forward-bias *I–V* has been indicated in Figure 5. It could be observed that the N_{ss} worth with series resistance are lower than those obtained without considering the R_s. These results advised that the R_s value should be considered in definition the energy density scatter of N_{ss} (Bilkan et al., 2015).

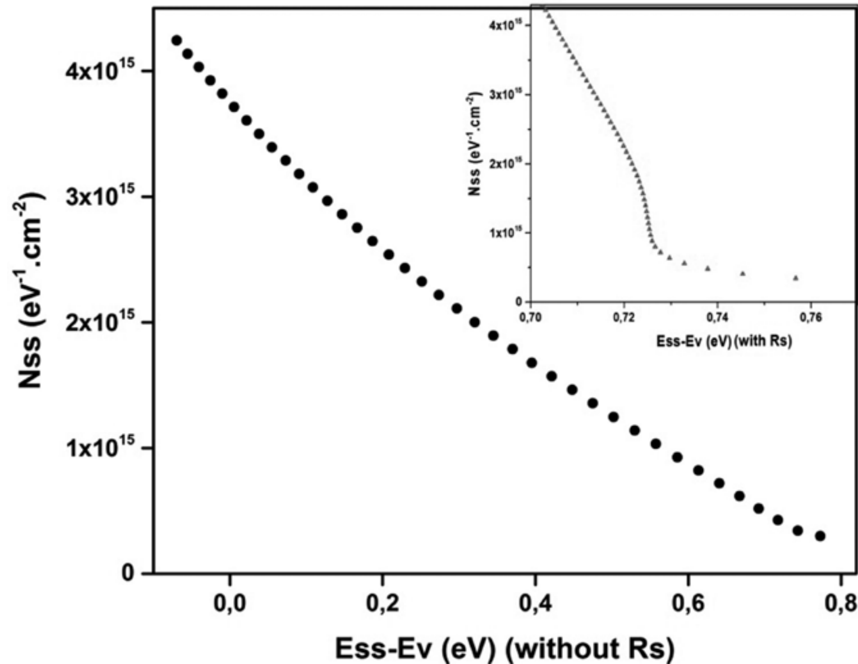

Figure 5. N_{ss}-(E_{ss}-E_v) graphs with R_s and without R_s

C-V and *G–V* graphs could be observed in Figure 6 and 7, respectively for Al/Si_3N_4/p-Si contact. The existence of the capacitance peak in the forward bias on *C–V* graphs was surveyed on MIS contact and attributed to the molecular arrangement of the series resistance and interface states (Bülbül et al., 2006). It has been in Figure 6 that the change in frequency affects the worth and status of *C–V* peaks. Moreover, the capacitance values have increased with the frequency decreasing. The high capacitance values at low frequencies could be ascribed the existence of the interface states at the Al/Si_3N_4/p-Si contact (Ataseven and Tataroğlu, 2013). In other words, charges at the interface states can chase the changing current (ac) signal at low frequencies. However, towards to high frequencies, these charges cannot chase the ac signal and not support to the capacitance (Yahia et al., 2011). But the conductance values have increasing tendency towards to high frequencies. These conclusions could be seen in Figure 6 and 7 for capacitance and conductance, respectively in Al/Si_3N_4/p type Si junction contact. In here, each *C–V* plot for different frequency has three regions (accumulation, depletion and inversion) could be seen in Figure 6, with a thinking voltage-axis change towards the reverse bias because of the interface states which is in balance via semiconductor. Similarly, Figure 7 has been indicated the changing of the conductance in the depletion zone for the same frequency alteration, showing the presence of several time-dependent reactions of interface states (Bülbül and Zeyrek, 2006).

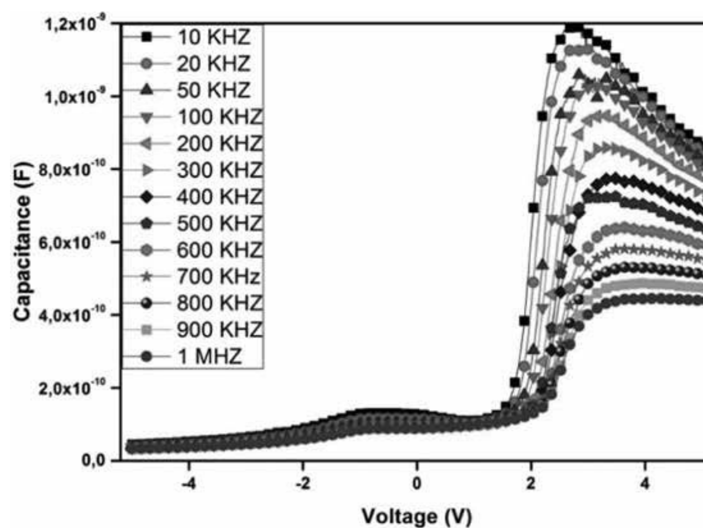

Figure 6. The capacitance-voltage (*C–V*) characteristic depending frequencies for Al/Si_3N_4/p-Si contact

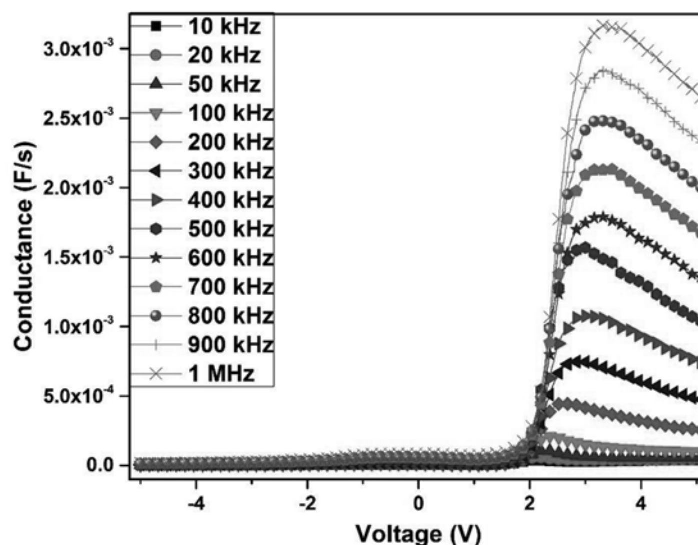

Figure 7. The conductance-voltage (*G–V*) characteristic depending frequencies for Al/Si_3N_4/p-Si contact

The C^{-2}–V graphs of Al/Si_3N_4/p type Si junction contact have been shown for various frequencies in Figure 8. It has been seen from this figure, the C^{-2}–V graph shows a straight in extensive voltage interval and the diffusion potential which is given in Table 2 is attained with extrapolation of straight lines to the voltage axis. It is known that intercept and slope voltage of the C^{-2}–V plot is dependent on the density of interface states and interface insulator sheet (Sztkowski and Sieranski, 1992). The C^{-2}–V graphs point out that the ac signal could not been follow by interface states and inversion layer charge in the depletion region, particularly in the accumulation and strong inversion (Bülbül and Zeyrek, 2006).

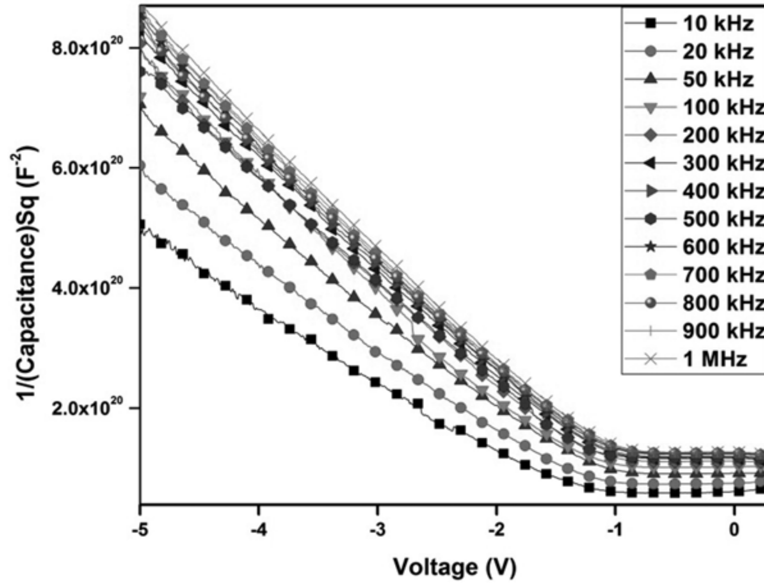

Figure 8. The C^{-2}–V plot of different frequencies Al/Si_3N_4/p type Si contact

The other some important electrical parameters of diode such as, Fermi energy level (E_F), intercept voltage V_i, the width of the depletion region (W_d), the concentration of acceptor atoms (N_a), the image force barrier lowering ($\Delta\Phi_b$) and the values of barrier heights of Φ_b were calculated the capacitance–voltage (C–V) measurements at 10 kHz to 1 MHz frequencies and all of them given in Table 2 for obtaining diode properties.

Table 2. The various parameters of Al/Si_3N_4/p-Si MIS contact obtained from C–V in the different frequencies

f (kHz)	N_A (10^{15} cm^{-3})	V_d (V)	E_F (eV)	$\Delta\Phi_b$ (eV)	Φ_b (eV)	W_d (10^{-5} cm)	E_m (10^4)(V cm^{-1})
10	1.645	0.889	0.178	0.0158	1.051	8.435	2.077
20	1.404	0.944	0.189	0.0157	1.117	9.407	2.035
50	1.259	0.736	0.192	0.0143	0.914	8.807	1.701
100	1.063	0.804	0.196	0.0141	0.986	9.979	1.637
200	1.129	0.714	0.195	0.0139	0.895	9.167	1.586
300	1.075	0.633	0.196	0.0133	0.816	8.805	1.467
400	1.079	0.482	0.196	0.0125	0.666	7.705	1.285
500	1.129	0.623	0.195	0.0134	0.804	8.563	1.485
600	1.056	0.605	0.196	0.0131	0.788	8.728	1.416
700	1.040	0.555	0.197	0.0128	0.739	8.382	1.355
800	1.097	0.578	0.195	0.0131	0.761	8.367	1.412
900	1.040	0.542	0.197	0.0127	0.726	8.284	1.340
1000	1.039	0.508	0.197	0.0125	0.693	8.063	1.292

Capacitance of depletion layer can be written as (Sze, 1981).

$$C^{-2} = \frac{2(V_R + V_i)}{q\varepsilon_s N_a A^2} \quad (16)$$

here, V_R is the reverse bias voltage, N_a is the acceptor concentration of doping element and V_i is the intercept voltage at zero bias and can be acquired by means of extrapolation of the C^{-2}–V plot to the voltage axis. Accounted N_a values have been given in Table 2 for different frequencies. From V_i values, the diffusion potentials (V_d) at zero bias can be found by use of below equation;

$$V_d = V_i + \frac{KT}{q} \quad (17)$$

The depletion layer widths (W_d) of the contact were also accounted from C^{-2}–V plots at for different frequencies below equation;

$$W_d = ((2\varepsilon_s\varepsilon_0 V_d)/qN_a)^{1/2} \quad (18)$$

The Fermi energy level could be calculated as

$$E_F = \frac{KT}{q} Ln\left(\frac{N_v}{N_a}\right) \quad (19)$$

With

$$N_v = 4.82 \text{ x } 10^{15} T^{3/2} \left(\frac{m_h^*}{m_0}\right)^{3/2} \quad (20)$$

where N_v is the efficient density of states in Si valance band and given as 1.04 x 10^{19} cm^{-3}, m_h^*= 0.16 m_0 is the effective mass of holes and m_0 is the rest mass of the electron. $\Delta\Phi_b$ is the image force barrier lowering and is given by

$$\Delta\Phi_b = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right]^{1/2} \quad (21)$$

where E_m is the maximum electric field and calculated with

$$E_m = \left[\frac{2qN_a V_i}{\varepsilon_s\varepsilon_0}\right]^{1/2} \quad (22)$$

After accounting of worth of V_d, E_F and $\Delta\Phi_b$, the values of barrier heights Φ_b (C–V) could be obtained from below relation;

$$\Phi_b(C-V) = V_d + E_F - \Delta\Phi_b \quad (23)$$

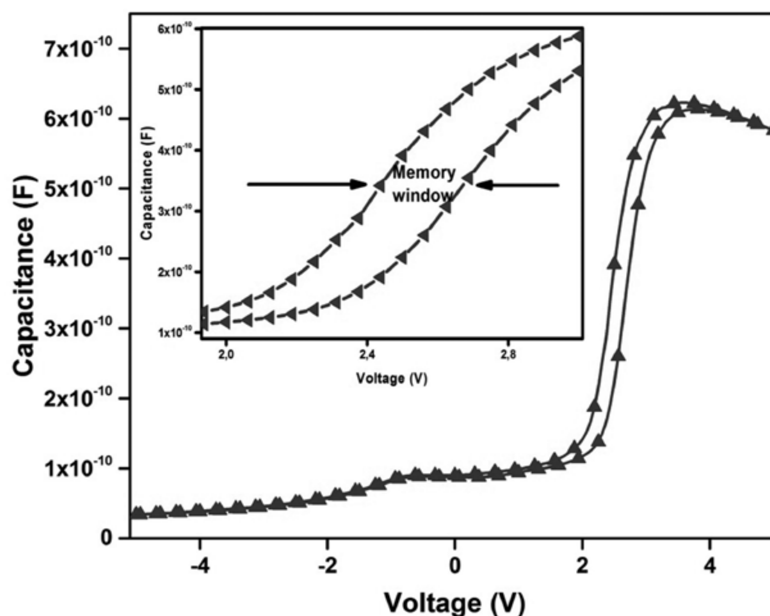

Figure 9. The capacitance-voltage characterization of Al/Si_3N_4/p type Si and Memory window graph at 500 kHz frequency

The issue of memristor is new and general because it has low power and nonvolatile operation, variety of physical mechanisms and potentially high density, placing advanced components of future computing systems (Orak et al., 2015). Si_3N_4 is commonly used memory contacts for memristive characterizations. As can be seen in Figure 9, The Al/Si_3N_4/p type Si has a memory window owing to Si_3N_4 at 500 kHz at 2 V to 3 V bias voltages. There is a near parallel shift in measured *C–V* characteristics. According to this graph, the contact can be used and improved some memory device applications.

CONCLUSION

The Al/Si_3N_4/p-Si contact (MIS) have been investigated its importance in electronic applications, especially capacitance behaviors. For this reason, 5 nm Si_3N_4 layers were doped with PECVD technique on p-type Si and obtained MIS contact with Al contact. It was researched the insulator layer effect on the Al/p-Si contact properties. It was investigated electrical characterizations using the forward and reverse bias *I-V*, *C–V* and *G-V* measurements and were seen that the insulator Si_3N_4 layer influenced characterizations of the contact. Some diode parameters and effect of the interface states (N_{ss}), the series resistance (R_s) were investigated by calculating from *I-V* and *C–V* measurements.

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